Journal of Operation and Automation in Power Engineering
Vol. 9, No. 3, Dec. 2021, Pages: 256 - 265
http://joape.uma.ac.ir

Design and Control of Three-phase Quasi-Z-Source Based Hybrid 2/3 Level Inverter

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Abstract- *Hybrid 2/3 level inverter is a combination of three-level diode clamped inverter and conventional two-level inverter. This structure has the advantages of both two-level and three-level structures. Also, the number of switches is less than three level diode clamped inverter. In this paper, a modified structure for a hybrid 2/3 level inverter, which is based on quasi-Z-source network, is investigated. This structure improves the performance of the 2/3 level inverter and develops the voltage boost capability of the structure. Increasing the output voltage can be achieved by selecting the appropriate short-circuit interval in quasi-Z-source network. In addition, short-circuit intervals in quasi-Z-source networks allow the inverter to operate without any dead time, which results in higher quality for output AC voltage. A modified switching method is presented for the proposed inverter and the related calculations are performed. Also, a simple control scheme is proposed to balance the neutral-point of the structure and to compensate the voltage imbalance of the Quasi network's capacitors. The proposed structure can be used to connect different distributed generation sources to an islanded load or to a low voltage grid. Simulations are carried out in MATLAB/Simulink environment and results depict suitable performance of proposed inverter.*

Keyword: Hybrid 2/3 level inverter, Loss analysis, Quasi-Z-source network, Switching strategy, THD.

1. INTRODUCTION

By developing power semiconductor devices, the operation of power electronic converters is increasing due to their low prices and volume. Voltage source inverters have been used in various industrial applications including locomotives, marine propulsion, reactive power compensation, motor drive in various power ranges, grid-connected applications especially in distribution networks, conversion of photovoltaic and wind renewable energy sources, interruptible power supplies (UPS), HVDC systems and electric vehicle charging stations, etc. [1]. Multi-level inverters have advantages in comparing with two-level inverters such as high output power quality, low THD, high amplitude for fundamental voltage, high efficiency, low switching losses, low dv/dt, low peak inverse voltage (PIV) [2]. Multilevel inverters contain semiconductor switches and capacitive sources that generate output voltage in a staircase manner. Commutation of the switches causes the voltage of the source s to accumulate together so that more voltage levels can be achieved at the inverter output. Nevertheless, the rated voltage of the switches is less than the total voltage of the voltage sources [3].

Although conventional two-level inverters have satisfactory performance in transient and steady state conditions, but in high power applications, there is a possibility of reduced efficiency, high voltage stress and distortion of their waveform, which affects the efficiency of the whole system [4-5]. Multilevel inverters are widely used in many industrial applications. Common structures of multilevel inverters include cascaded H-bridges (CHB), neutral point diode clamped (NPC), and fly capacitors (FC) [6-7]. In conventional voltage source multilevel inverters, the output AC voltage is less than the sum of input DC sources and these structures are only capable of reducing the voltage [8].

Recent advances in impedance source-based converters have led to an increase in the use of these types of inverters in various power electronic applications. The Z-source inverters are a good option for industrial drives and renewable energy sources, but the main disadvantage of the Z-source inverters are the discontinuous input current and the lack of common ground between the input source and inverter terminals.

Received: 30 August. 2020
Revised: 16 Jan. 2021
Accepted: 25 Feb. 2021
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DOI: 10.22098/joape.2021.7681.1548
Research paper

To solve this problem quasi-Z-source inverter has been proposed [9-10].

Among the various structures of multilevel inverters, the three-level neutral-point clamp diode (NPC) inverters have been used extensively in medium voltage and power applications. However, this inverter acts as a buck converter and the output AC voltage is smaller than the input DC voltage. Therefore, a dc-dc boost converter can be used at the input of the inverter to reach the required higher AC output voltage, which increases the cost and complexity of system [11]. In order to convert and increase the DC input voltage to a higher output AC voltage in a single-stage condition in the NPC structure, the use of Z-source network as increasing the DC input voltage has been proposed in Refs. [12-13]. The Z-source inverter has the ability to increase the voltage by using the shoot-through state mode. In addition, in this structure, there is no need for dead time, which leads to improved quality of the output voltage. However, to solve the problem of discontinuous input current in the Z-source network structure, quasi-Z-source NPC inverter topology is investigated in Refs. [14,15]. The quasi-Z-source NPC inverter topology not only has a continuous input current, but also includes a single-stage boost capability as well as a reduction in voltage stress on the switches and good switching frequency performance [15].

The 3-level T-type inverter (3LT2I) is a suitable topology for low voltage applications. This inverter has a simple structure that reduces switching conduction losses in comparing with a conventional 3-level neural point diode clamp inverter (3LNPCI). So, the 3LT2I is a good choice for renewable energy applications that are often connected to a low voltage grid. This inverter also can operate as a buck converter. Therefore, the use of impedance source network to increase the voltage and single-stage conversion of DC to AC voltage in T-type inverter has been suggested in some references [16, 17]. The structures of [16,17] are not applicable to most renewable energy sources such as solar arrays as well as fuel cells due to their discontinuous input current. To solve this problem, three-level T-type inverters based on quasi-Z-source network are presented in Refs. [18-20]. Quasi-Z-source three-level T-type inverter (QZS 3LT2I) which has the advantages of 3LT2I and QZS inverters simultaneously and is considered as a suitable topology.
The number of power semiconductors in an NPC converter is twice the number of power semiconductors in a two-level traditional three-phase inverter. In addition, this topology requires six additional diodes. The voltage stress on the switches of this structure is equal to half the voltage of the DC link, which makes it possible to use this structure in medium voltage applications. The T-type three-level inverter contains 12 semiconductor switches and six diodes of the NPC structure are removed in the T-type structure. However, the main disadvantage of this type of converter is the voltage stress on the switches, which is equal t o the total DC link voltage. In other words, the switches of T-type inverter must withstand twice the blocking voltage compared to switches of NPC inverter. Therefore, the elimination of fast diodes and the addition of switches with blocking voltage and higher cost are the main advantages and disadvantages of the T-type converter structure.

A new type of power electronic converter has been introduced in Ref. [21], which reduces the number of switches and increases the quality of output AC voltage. This structure is called a hybrid 2/3 level converter or 10-switch converter. Structurally, the number of power semiconductors of the hybrid 2/3 level inverter is lower than three-level NPC inverter as well as the T-type inverter. However, a 10-switch inverter cannot produce a full three-level AC voltage and produces a combination of two and three-level AC voltages. In the case of switch reduction, the 2/3 level inverter has two switches less than the T-type inverter and also, unlike NPC, does not require additional diodes. The voltage stress on the switches of auxiliary leg of the 10-switch inverter is equal to half the voltage of the DC link, as in the NPC inverter. For the other 6 switches of this structure, the voltage stress will be equal to the total value of the DC link voltage, which is the same as a conventional two-level and three-level T-type inverter. A hybrid 2/3 level inverter can be a good option for low voltage applications (less than 575 volts) such as integration of photovoltaic arrays to a low voltage grid [22], low voltage AC motor drive [23] and in bipolar hybrid microgrids [24].

In this paper, a single-stage 2/3 level inverter based on double quasi-Z-source networks is proposed. The quasi-Z-source network employed not only results in voltage buck-boost but is also expected to be more reliable. This is attributed to the insertion of shoot-through and will not cause any semiconductor failure. Furthermore, as the shoot-through allows the inverter to be performed without dead-time protection, the quality of the output is better. The output voltages of the inverter can be boosted by accurate insertion of shoot-through states at equal time intervals. To achieve that, this paper proposes a proper PWM switching pattern for the investigated three-phase quasi-Z-source based

hybrid 2/3 level inverter. The performance and the details of switching strategy for the investigated structure is analyzed. In Addition, a simple control scheme is proposed to balance the neutral-point of the structure and to compensate the voltage imbalance of the Quasi network's capacitors. The investigated structure can be a good option for integrating the distributed generation resources such as photovoltaic arrays to a low voltage grid with acceptable injection power quality. To evaluate the efficiency of the proposed structure, the performance of this structure has been compared with three-level quasi-Z-source NPC and T-type inverters.

2. THE PROPOSED INVERTER STRUCTURE

Fig. 1 displays the structure of a hybrid 2/3 level quasi-Z-source inverter. This converter consists of two quasi-Z-source networks, a three-phase bridge including switches S_{x1}-S_{x2} (x = a, b, c), and four auxiliary switches including S_1-S_4. Auxiliary switches S_1, S_2, S_3 and S_4 cause to positive and negative sides of the three-phase bridge to be connected to one of the positive or negative ends of the DC link or to the neutral point 0, so the output voltage can be two-level at some intervals and three-level at other intervals. The quasi-Z-source network has the ability to increase the input voltage and delivers the increased voltage to the two DC branches of the hybrid 2/3 level inverter's input. The quasi-Z-source network consists of four inductors and four capacitors that are located in the inverter's input. The advantage of a quasi-Z-source network is that it receives continuous current from a DC source. Table 1 demonstrates the possible switching modes of the proposed inverter.

3. SWITCHING SCHEME OF THE PROPOSED INVERTER

Considering the quasi-Z-source network in Fig. 1 and assuming that the inductors and capacitors of the impedance network are equal, the circuit analysis is performed in this section. The peak value of the DC link voltage can be considered from the following equation.

$$V_{DC} = V_{oU} + V_{oL} \tag{1}$$

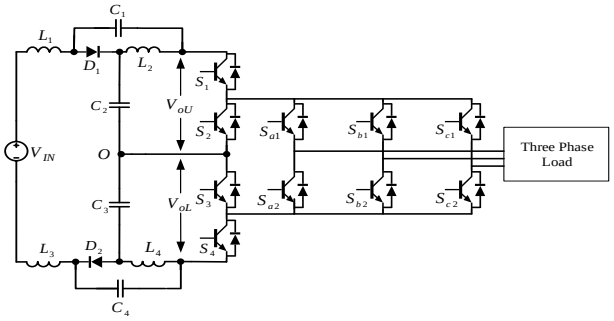

Fig. 1. The structure of hybrid 2/3 level quasi-Z-source inverter

Table 1. Possible switching states for the proposed inverter

S_1	S_2	S_3	S_4	S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	V_o
1	0	1	0	1	0	1	0	1	0	E/2
1	0	0	1	1	1	1	1	1	1	0
0	1	0	1	0	1	0	1	0	1	-E/2

where V_{oU} is the output voltage of upper quasi-Z-source network and V_{oL} is the lower one. It is assumed that $L_1 = L_3$, $L_2 = L_4$ and $C_1 = C_4$, $C_2 = C_3$. Accordingly, $v_{L1} = v_{L3}$, $v_{L2} = v_{L4}$ and $V_{C1} = V_{C4}$, $V_{C2} = V_{C3}$. Considering the above conditions, the voltage of the capacitors can be obtained from following equations:

$$V_{C1} = V_{C4} = \frac{D_S V_{IN}}{2-4D_0}$$
$$V_{C2} = V_{C3} = \frac{V_{IN}(1-D_0)}{2-4D_0} \tag{2}$$

The boost factor of the utilized quasi-Z-source network is obtained from the following equation.

$$B = \frac{V_{DC}}{V_{IN}} = \frac{V_{C1}+V_{C2}+V_{C3}+V_{C4}}{V_{IN}} = \frac{1}{1-2D_0} \tag{3}$$

The effective value of the inverter's output phase voltage can be calculated from the following equation.

$$V_o = M\frac{V_{DC}}{2\sqrt{2}} = M\frac{V_{IN}}{2\sqrt{2}(1-2D_0)} \tag{4}$$

The relationship between the output voltage by input voltage (V_{IN}) and the shoot-through duty cycle (D_0) can be expressed as:

$$V_o = \frac{(1-2D_0)V_{IN}}{2\sqrt{2}(1-2)D_0} \tag{5}$$

The hybrid 2/3 level inverter has three main legs and an auxiliary leg. These three main legs can be switched into two or three levels by PWM switching scheme based on the size of the reference signals and their comparison with each other. The function of the inverter's auxiliary leg is to connect to the positive, negative, or neutral point of the DC side. In case that the inverter is switched in three-level mode, positive output voltage is generated in the range of zero and *E/2*, and negative output voltage is generated in the range of zero and *-E/2*, and in case the inverter is switched in two-level mode, the output voltage is in the range of *E/2* and *-E/2*. Fig. 2 illustrates the single-phase reference voltage as well as the three triangular carrier signals for generating three-level NPC inverter's switching signals. For proper switching of hybrid 2/3 level inverter by PWM switching scheme, two v_{mid1} and v_{mid2} signals are required according to the presented method in Ref. [10]. Two v_{mid1} and v_{mid2} signals are required for inverter operation mode in two or three levels. Fig. 3 displays the single-phase reference voltage of the three triangular carrier signals as well as the intermediate v_{mid1} and v_{mid2} signals to generate the switching signals of the hybrid 2/3 level inverter.

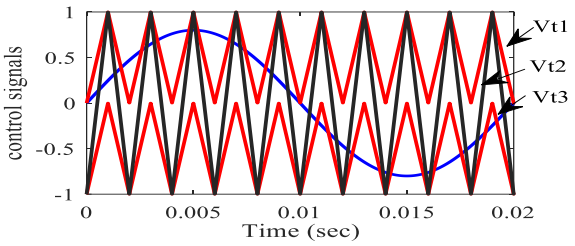

Fig 2. Modulation and carrier signals for PWM switching of three-level inverter

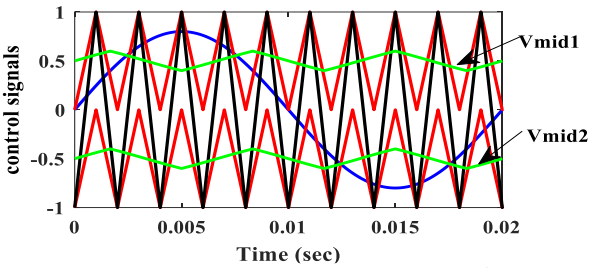

Fig 3. Modulation, carrier and intermediate signals for PWM switching of hybrid 2/3 level inverter

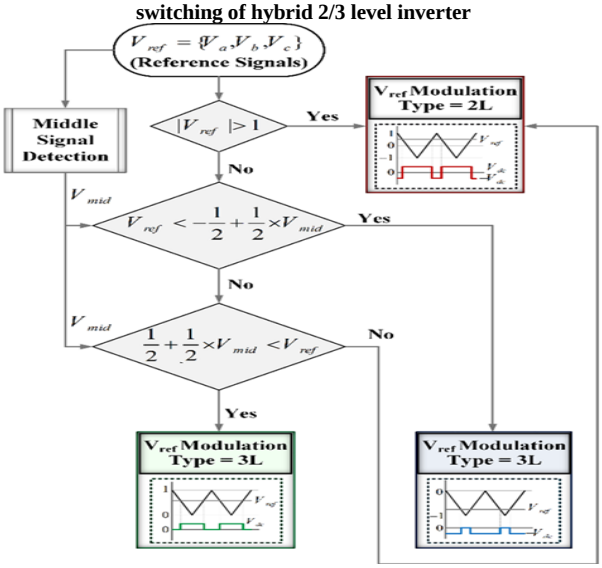

Fig. 4. The modulation scheme for hybrid 2/3 level inverter

The switching logic for a hybrid 2/3 level inverter is as follow:

A. If the modulation signal is larger than the upper intermediate signal vmid1, the modulation signal will be compared with the carrier signal V_{t1} and a three-level positive output voltage should be generated in the zero and *E/2* range.

B. If the modulation signal is smaller than the lower intermediate signal v_{mid2}, the modulation signal will be compared with the carrier signal V_{t3} and the negative three-level output voltage should be generated in the zero and *-E/2* range.

C. If the modulation signal is between the upper intermediate signal v_{mid1} and the lower intermediate signal v_{mid2}, the modulation signal will be compared with the carrier signal V_{t2} and the two-level output voltage should be generated in the *E/2* and *-E/2* range.

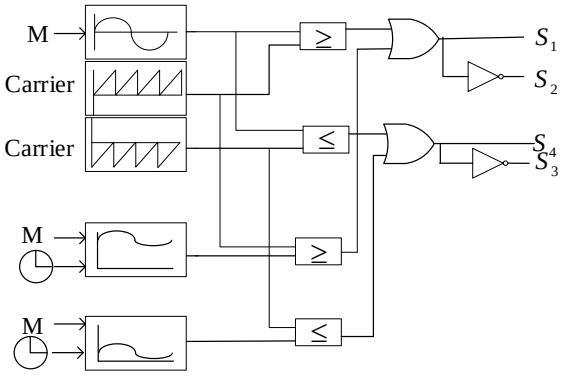

Fig. 5. The logic for shoot-through interval calculation of proposed inverter

D. The mean signal of v_{mid} can be calculated according to Eq. (6).

$$V_{mid} = -\frac{V_{\max} + V_{\min}}{2} \tag{6}$$

As mentioned above, the three-level mode will be established if the condition presented in Eq. (6) is met. And also, the two-level mode will be established if the condition presented in Eq. (7) is realized. In this method, if the amplitude of one of the reference signals is greater than 1, all converter legs will be switched on two levels until the amplitude of all the reference signals is less than one. In the next step, the magnitude of the reference signals is compared with each other and their intermediate signal is determined and applied in Eq. (6) and Eq. (7). If the reference signal satisfies one of the conditions, it will be compared with the positive or negative three-level carrier signal according to the equations shown in the flowchart of Fig. 4.

$$If\ V_{ref} > \frac{1}{2} + \frac{1}{2}V_{mid}\ \ or\ \ V_{ref} < -\frac{1}{2} + \frac{1}{2}V_{mid} \tag{7}$$

$$If\ \frac{1}{2} + \frac{1}{2}V_{mid} < v_{ref} < -\frac{1}{2} + \frac{1}{2}V_{mid} \tag{8}$$

Fig. 5 demonstrates the governing logic of the short circuit interval in the proposed inverter. The modulation, carrier and intermediate signals as well as S_1 to S_4 signals in the switching scheme for the conventional hybrid 2/3 inverter without short circuit intervals are presented in Fig. 6. These signals with considering short circuit intervals are illustrated in Fig. 7 for the proposed hybrid 2/3 level quasi-Z-source inverter. The short-circuit signals are shown in Fig. 7 along with the single-phase modulation signal and the three carrier signals. Also, in this figure, the signals S_1 to S_4 are shown in a way that short circuit intervals are also visible in these figures. As mentioned earlier, during non-shoot-through modes, deformation follows the same pattern observed in conventional carrier-based PWM. From the comparison of Figures (6) and (7) results, the differences of switching signals between two

structures are clearly visible and the short circuit intervals can be seen in Fig. 7. As mentioned earlier, the difference between the positive and negative short-circuit signals is constant. This keeps the short-circuit duty ratio (D_0) constant. The short-circuit duty ratio can be expressed in the maximum constant boost control method according to Eq. (9).

$$D_0 = \frac{T_0}{T} = \frac{2-\sqrt{3}M}{2} \tag{9}$$

4. POWER LOSS CALCULATION OF THE PROPOSED INVERTER

The loss of an inverter is equal to the total power loss of all power semiconductor devices. Losses can be divided into three categories:

A. When the equipment blocks the current (off state), in this case, since the leakage current is a very small amount, losses are negligible and can be ignored.
B. When the equipment is conducting (on state), the loss is called conduction loss.
C. When the equipment is in the switching mode (transition from on state to off state and vice versa), the loss is called switching loss.

Therefore, the loss related to the proposed inverter is considered only conduction and switching loss, each of which is discussed in Ref. [25].

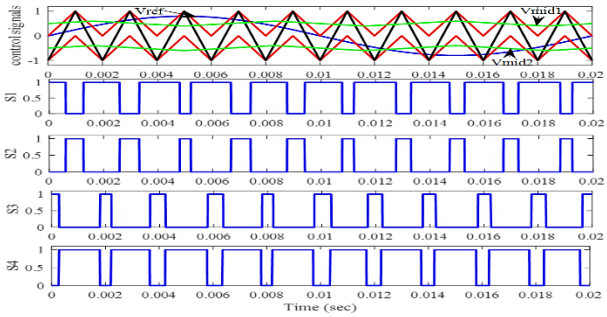

Fig. 6. Modulation, carrier and intermediate signals as well as S_1 to S_4 signals in the switching scheme for the conventional 2/3 inverter without short circuit intervals

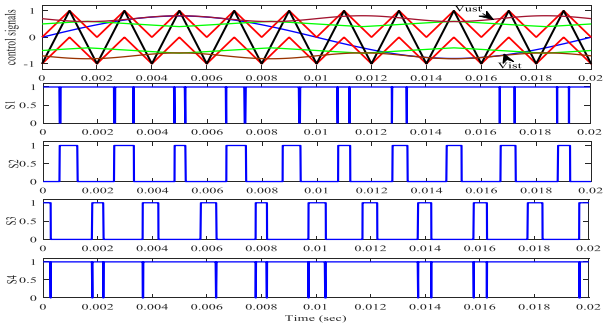

Fig. 7. Modulation, carrier and intermediate signals as well as S_1 to S_4 signals in the switching scheme for the proposed hybrid 2/3 quasi-Z-source inverter considering short circuit intervals

4.1. Conduction loss

The power transistors used in the proposed topology have the ability to conduct bidirectionally and block unilaterally. Conductive losses of transistors and their anti-parallel diodes are [26].

$$P_{c,Transistor}(t) = \left(V_T + R_T i^{\beta}(t)\right) i(t) \tag{10}$$

$$P_{c,Diode}(t) = \left(V_D + R_D i(t)\right) i(t) \tag{11}$$

where $P_{C,Diod\ (t)}$, $P_{C,Transistor\ (t)}$ are related to the conduction losses of the transistor and diode, respectively, V_T and V_D are the voltage drop across the transistor and diode in the on state, R_T and R_D are the resistors of the transistor and diode in the on state and β is a constant value which is a function of the properties of the transistor.

As mentioned, the conductivity of the switches is a function of the instantaneous load current $i_L(t)$. In addition, depending on the level of the inverter's output voltage and the polarity of the load current, a transistor or anti-parallel diode can conduct. At any given time, the number of conducting diodes and transistors are $N_D(t)$ and $N_T(t)$, respectively. Therefore, the average conduction losses can be expressed by Eq. (12) using equations (10) and (11):

$$P_{c,avg} = \frac{1}{\pi}\int_0^{\pi}\Big[\left(N_T(t)V_T + N_D(t)V_D\right)i_L(t) + \left(N_T(t)R_T i_L^{\beta+1}(t)\right) + \left(N_D(t)i_L^2(t)\right)\Big]d(\omega t) \tag{12}$$

4.2. Switching loss

To calculate the switching loss of the proposed inverter, the switching loss of each switch is calculated. Then, to calculate the switching losses of the whole inverter, the loss of each switch is accumulated to each other. To calculate the switching loss of a switch, a linear approximation of voltage and current is used during the switching period (transition from on to off state and vice versa) [27]. Energy losses of turning on can be calculated with Eq. (13).

$$E_{on,j} = \int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}}\left[\left(V_{o,j}\frac{t}{t_{on}}\right)\left(-\frac{I}{t_{on}}(t-t_{on})\right)\right]dt = \frac{1}{6}V_{o,j}.I.t_{on} \tag{13}$$

$$E_{off,j} = \int_0^{t_{off}} v(t)i(t)dt = \int_0^{t_{off}}\left[\left(V_{o,j}\frac{t}{t_{off}}\right)\left(-\frac{I'}{t_{off}}(t-t_{on})\right)\right]dt = \frac{1}{6}V_{o,j}It_{off} \tag{14}$$

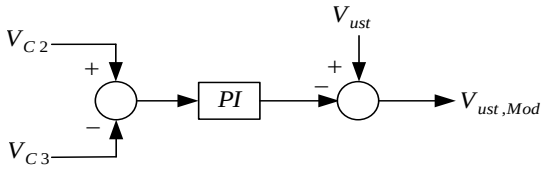

Fig. 8. Control block diagram for neutral point voltage unbalance compensation

In Eq. (13), $E_{on,\,j}$ indicates the energy loss of the switch and the t_{on} is the time the j-th switch takes to turn on. The switch current is denoted by I after switching on, and $V_{o,\,j}$ represents the voltage that the j-th switch should block when it is off. Similarly, the energy losses of the j-th switch during shutdown can be calculated with Eq. (14). In this equation, t_{off} is the time the j-th switch takes to turn off and I is the current before the switch turns off. The switching loss is a function of the number of switch changes as well as the switching technique. In the time interval of 1 second, the j-th switch changes f_j times, which f_j is the switching frequency. Hence, it is assumed that the sum of power switching losses can be expressed as follows.

$$P_s = \sum_{j=1}^{M}\left[\frac{1}{6}V_{o,j}I(t_{on}+t_{off})f_j\right] \quad (15)$$

4.3. Total power loss

The total inverter loss can be calculated using equations (12) and (15). The output power of the inverter can be calculated using equation (17). The inverter efficiency can be calculated using Eq. (18).

$$P_{losses} = P_{c,avg} + P_s \quad (16)$$

$$P_{out} = V_{out} \times I_{out} \quad (17)$$

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \quad (18)$$

5. NEUTRAL POINT BALANCING CONTROL SCHEME

As shown in Fig. 8, a simple solution is proposed to avoid deviation of neutral point and compensate voltage unbalance at upper and lower capacitors (C_2 and C_3) of the quasi-Z-source networks. In this control scheme, voltage difference of C_2 and C_3 is fed to a PI controller. The output of the controller as a corrective signal is subtracted from V_{ust}. This scheme causes to little changes in switching and turn on/off intervals. It leads to neutral point voltage balancing and eliminates voltage unbalance at C_2 and C_3.

6. SIMULATION RESULTS

In this section, the simulation of proposed inverter is investigated. Table 2 shows the proposed inverter simulation values.

Table 2. The simulation parameters of the proposed inverter

Parameters	Values
DC Source Voltage	100V
Quasi Z-Source inductor	1mH
Quasi Z-Source capacitor	1000 μF
Switching Frequency	5kHz
Load resistance	10Ω
Load inductor	7mH
Fundamental Frequency	50Hz
Modulation Index (M)	0.85

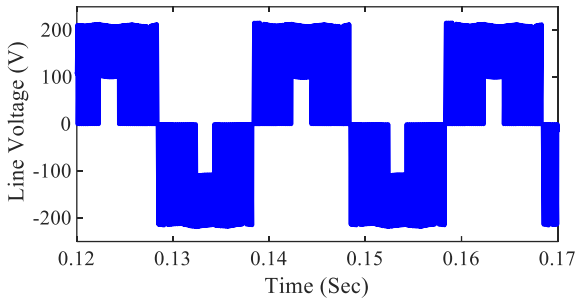

Fig. 9. Line voltage of proposed inverter

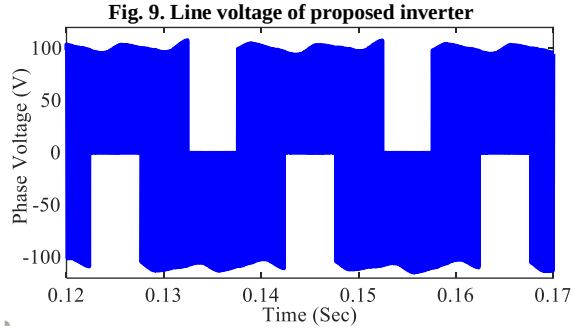

Fig. 10. Phase to neutral point voltage of proposed inverter

Fig. 9 displays the line voltage of proposed inverter. As can be seen in this figure, the output line voltage includes two-level and three-level intervals. The peak voltage of the line voltage indicates that the quasi-Z-source network has increased the input DC voltage of 100 volts to the peak voltage of the line equal to 200 volts. Fig. 10 displays the phase voltage of the proposed inverter. According to Equation (9), for the modulation index of 0.85, the value of the short circuit duty cycle of the proposed structure will be equal to 0.26. Replacing the values mentioned in Equation (3), the boost factor of the proposed structure is nearly equal to 2. In addition, by replacing the values in equation (4), the effective value of the output phase voltage of the proposed inverter is 73 volts and the peak value of the phase voltage relative to the neutral point is about 100 volts. The simulation results in Fig. 10 show the correct operation of the proposed structure and the compatibility of the simulation results with the provided relationships for this structure. As shown in Figures (9) and (10), the peak output voltage is associated with a slight ripple, which is due to the use of the maximum constant boost switching method. If the simple boost method is used to increase the voltage in the quasi-Z-source network, the existing voltage ripple will be lost.

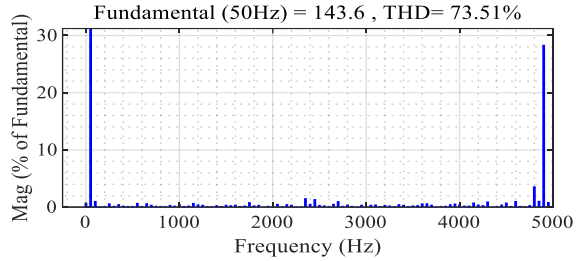

Fig. 11. THD for line voltage

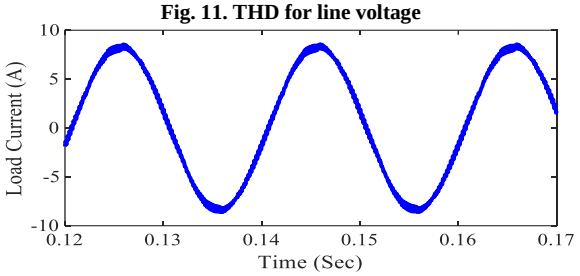

Fig. 12. The output current of proposed inverter for R-L load

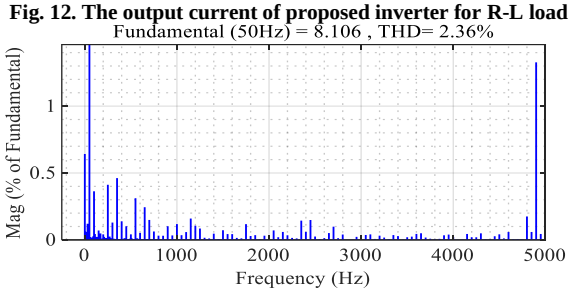

Fig. 13. THD for the output current

Fig. 11 displays THD of the proposed inverter's line voltage. It is worth noting that the THD presented in this figure is displayed in the inverter's output without considering the filter. Fig. 12 demonstrates the output current of the proposed inverter for a R-L output islanded load and also Fig. 13 shows the THD of the inverter's output current. If an L or LC filter is used at the output of the inverter, the THD of the voltage and current will decrease significantly.

Fig. 14 displays the voltage of two capacitors C_2 and C_3 of quasi-Z-source network without applying neutral voltage control scheme. Without this scheme for limiting the neutral point deviation, capacitor voltages are unbalance, where C_2 voltage increases and C_3 voltage decreases inchmeal. This unbalance may cause several drawbacks in structure operation. As demonstrated, voltage deviation increases by time passing. Finally, voltage of a capacitor attenuates and becomes zero in such system and then mismatches occur in the converter operation. Fig. 15 shows the capacitor voltages after using the unbalance compensation controller. As shown, voltages of the capacitors are matched together and there is no unbalance. According to Fig. 15, the energy of the input DC voltage source of 100 volts is transmitted by the quasi-Z-source network to two capacitors C_2 and C_3 with a voltage of about 77 volts.

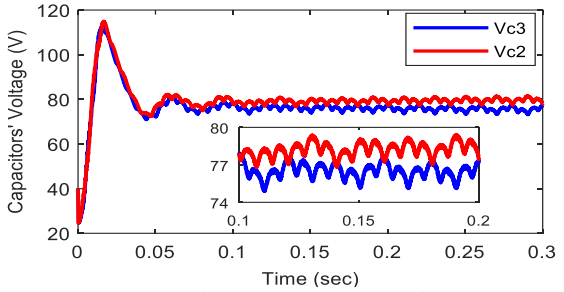

Fig. 14. The voltage of capacitors C_2 and C_3 of quasi-Z-source network without applying neutral voltage control scheme

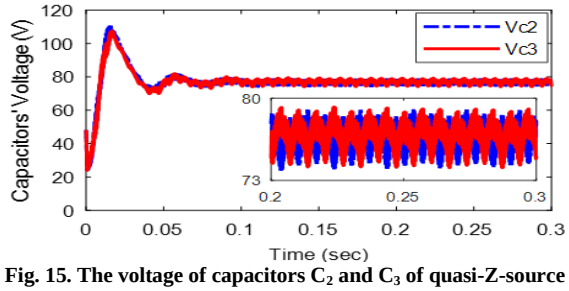

Fig. 15. The voltage of capacitors C_2 and C_3 of quasi-Z-source network considering neutral voltage control scheme

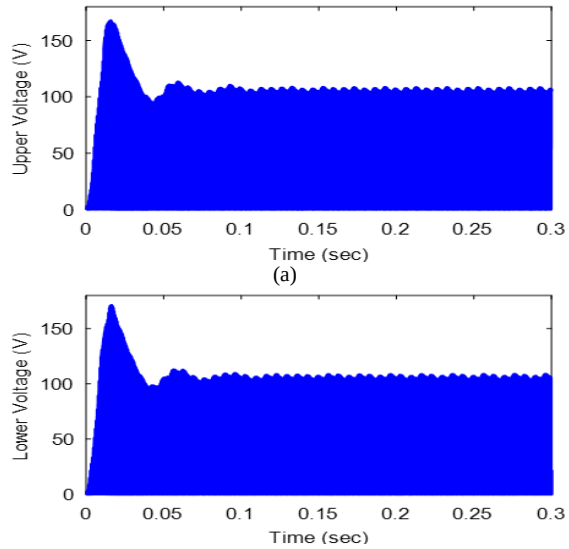

Fig. 16. (a). The voltage of upper DC link (V_{oU}), (b). The voltage of lower DC link (V_{oL})

Fig. 16 (a) and (b) show the output voltage of the two quasi-Z-source networks which are the upper DC link voltage (V_{oU}) and the lower DC link voltage (V_{oL}), respectively. Naturally due to short circuit intervals, these two voltages will be equal to zero in some intervals and are about 100 volts in other intervals. For this reason, these two voltages are visible as solid between zero and 100 volts. In order to certify the performance of the proposed controller, simulation run time has been increased. Fig. 17 shows the result for 3 seconds. As shown, the two voltage signals are matched and balanced. The output signal of the PI controller is shown in Fig. 18. This signal is subtracted from V_{ust}. It causes neutral point voltage balancing and avoids from unbalance in the capacitor voltages.

Table 3. Loss analysis results for proposed inverter

Parameter	Value
Switching Losses (W)	4.5
Conduction Losses (W)	35.9
Total Losses (W)	38.2
Efficiency (%)	97.3
P_{out} (W)	1300

Table 4. The comparison of line voltage THD between three compared structures

Structure	THD
T-Type quasi-Z-source Inverter	76.4%
NPC quasi-Z-source Inverter	42%
2-level quasi-Z-source Inverter	96.1%
2/3-level quasi-Z-source Inverter	73.3%

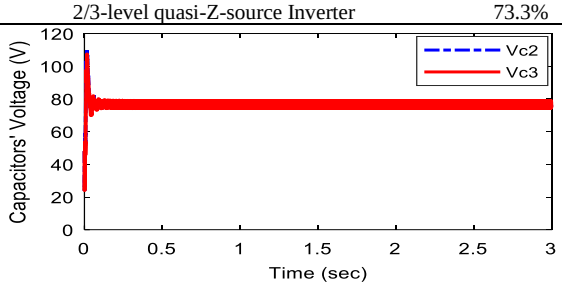

Fig. 17. The voltage of capacitors C_2 and C_3 of quasi-Z-source network in a more time interval

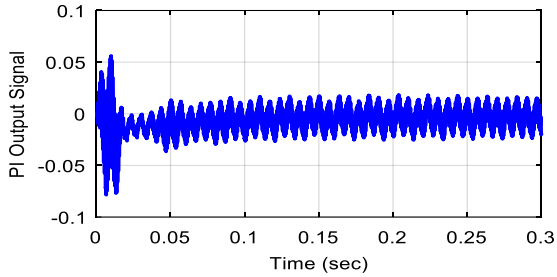

Fig. 18. The output signal of the PI controller in the neutral point balancing control scheme

The results of the proposed structure's loss, switching loss, conduction loss, total loss and efficiency, as well as output power are presented in Table 3, respectively. It should be noted that, the loss and efficiency are not merely calculated based on input/output measured powers. But precise loss calculations are conducted and inverter loss and efficiency are resulted. In the section 4, more explains is presented for power electronic converter loss calculations. A power electronic converter conduction loss can be resulted by Eqns. (10), (11), and (12). Switching loss can be resulted by Eqns. (13), (14), and (15). Total loss and efficiency can be yielded by Eqns. (16) and (18), respectively [25], [26]. For all switches and diodes of the structure, the mentioned equations are exerted in the MATLAB/Simulink. Then, switching and conduction loss of all switches and diodes are extracted and calculated during converter operation.

7. COMPARING THE PROPOSED STRUCTURE WITH SIMILAR STRUCTURES

In addition to presenting the results of the proposed structure, the proposed inverter for the same output load and the same output power have been compared with similar structures including quasi-Z-source based structure of the three-level NPC, the three-level T-Type and conventional two-level inverters. To perform the comparison under fair conditions, all the structures have been examined under the same voltage and output power. Naturally, due to the differences in the structures, their input voltage will be different. But the purpose of this section is to compare these structures for single power supply with the same output power and voltage.

Table 4 displays the result of comparing the THD value of the proposed inverter's line voltage with three similar structures. As shown in the table, the THD of the proposed inverter is lower than the two T-Type quasi-Z-source inverter as well as two-level quasi-Z-source inverter while is higher than the three-level NPC quasi-Z-source inverter. Since the NPC structure produces a pure three-level output voltage, the THD value of the proposed structure with a two- or three-level output voltage is higher than that of the three-level NPC quasi-Z-source inverter. On the other hand, the T-Type structure does not produce pure three-level voltage, and hence the THD of the proposed structure is less than the T-Type structure as well as the two-level structure.

Table 5. Efficiency comparison between 3 compared structures

Structure	Efficiency
T-Type quasi-Z-source Inverter	96.23%
NPC quasi-Z-source Inverter	95.10%
2-level quasi-Z-source Inverter	98.28%
2/3-level quasi-Z-source Inverter	97.38%

Table 6. MBV, TBV and total energy storage in L and C of three-level compared structures

Parameters \ Structures	P_{out} (pu)	QZS-NPC	QZS-T-Type	QZS-Hybrid 2/3 Level
MBV (*100V) Only for Switches	0.5	0.82	1.38	1.54
	0.75	0.96	1.66	1.86
	1.0	1.1	1.96	2.18
MBV (*100V) Switches and Diodes	0.5	0.88	1.38	1.54
	0.75	1	1.66	1.86
	1.0	1.2	1.96	2.18
TBV (*100V) Only for Switches	0.5	9.84	12.5	12.32
	0.75	11.52	14.94	14.88
	1.0	13.2	17.64	17.44
TBV (*100V) Switches and Diodes	0.5	15.2	12.5	12.32
	0.75	17.52	14.94	14.88
	1.0	20.4	17.64	17.44
$\sum_{k=1}^{4}\frac{1}{2}L_k I_k^2$ (J)	0.5	0.14	0.12	0.13
	0.75	0.3	0.28	0.3
	1.0	0.56	0.49	0.55
$\sum_{k=1}^{4}\frac{1}{2}C_k V_k^2$ (J)	0.5	4	3.84	4.04
	0.75	5.2	4.98	5.25
	1.0	6.5	6.28	6.6
$\sum_{k=1}^{4}\frac{1}{2}L_k I_k^2+\sum_{k=1}^{4}\frac{1}{2}C_k V_k^2$ (J)	0.5	4.14	3.96	4.17
	0.75	5.5	5.26	5.55
	1.0	7.06	6.77	7.15

Table 5 compares the proposed structure in terms of efficiency with three similar structures. As shown in the table, the efficiency of the proposed inverter is higher than the three-level NPC quasi-Z-source and the T-Type quasi-Z-source inverters. Note that that the proposed structure has 2 switches less than the two other

mentioned three-level structures, increasing the efficiency of the proposed structure is logical. The efficiency of the proposed structure is about one percent lower in comparing with the two-level structure due to the four more switches.

In order to more evaluations the effectiveness of the studied structure, comparison with similar three-level structures such as QZS-NPC and QZS-T-type is essential. To fair comparison, for three structures the input voltages are equal (i.e. 100 V), modulation index is 0.8. The output power is investigated for three conditions as 0.5 pu, 0.75 pu, and 1 pu. Note that nominal power is 1500 W. The results of this comparison are illustrated in Table 6. The investigation results show that maximum blocking voltage (MBV) by the switches of the QZS-NPC structure is lower than other structures. Also, without considering the blocking voltage of diodes in the Total Blocked Voltage (TBV) calculation, the TBV for the QZS-NPC is lower than other two structures. If blocking voltage of the diodes in the QZS-NPC structure is considered in TBV calculation, this structure will lose the ideal condition. It is noticeable that the QZS-NPC structure due to switch configuration has lower TBV and is suitable for medium voltage and power applications. For the same reasons, the QZS-T-Type structure and quasi-Z-source based hybrid 2/3 level structure are suitable for low voltage applications. For low voltage applications, the conventional price switches abound. And then, MBV and TBV issues are not important. MBV and TBV comparison between QZS-T-Type and QZS-Hybrid 2/3 Level structures shows in QZS-Hybrid 2/3 Level structure MBV is 12% higher and TBV is 1% lower. Therefore, MBV and TBV values are not sensible difference in these two structures. On the other hand, QZS-Hybrid 2/3 Level structure has two switches lower than QZS-T-Type structure and then lower cost. Also, the stored energies in inductances and capacitors of the quasi-Z-source network for three studied three-level structures for same conditions are presented in Table 6. According to results of this table, there is not sensible difference in the structures. In general, the proposed structure has suitable conditions in comparison with the three compared structures. The proposed structure has the ability to increase the input voltage. The output voltage of the proposed structure is two-level in some intervals and three-level in other intervals. The quality of the output voltage of the proposed structure is almost similar to the three-level T-Type quasi-Z-source structure and its efficiency is higher than the three-level T-Type quasi-Z-source inverter.

8. CONCLUSION

In this paper, two quasi-Z-source networks are used at the input of the hybrid 2/3 level inverter to provide the ability to increase the input voltage. The structure of a hybrid 2/3 level quasi-Z-source inverter is introduced and studied with the aim of creating the ability to increase the voltage while reducing the number of switching components compared to three-level structures. Appropriate switching logic is presented for the correct operation of the proposed structure and the resulting relationships are extracted for this structure. Comparing the performance of the proposed structure with conventional two-level and three-level quasi-Z-source inverters indicates the appropriate efficiency of the proposed structure. The THD of the proposed structure has been improved by 22.8% in comparing with the two-level quasi-Z-source inverter and 3.1% compared to a three-level T-type quasi-Z-source inverter. In addition, the efficiency of the proposed structure is improved by 3% compared to three-level NPC quasi-Z-source inverter and by 2% compared to three-level T-Type quasi-Z-source inverter. In general, the proposed structure has advantages of conventional two-level and three-level inverters at the same time and is a suitable option for low voltage applications.

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