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An LCL-Filtered Single-Phase Multilevel Inverter for Grid Integration of PV Systems

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ABSTRACT

Integration of the PV into the electrical grid needs power electronic interface. This power electronic interface should have some key features and should come up with grid codes. One of the important criteria is the quality and harmonic contents of the current being injected to the grid. High-order harmonics of the grid current should be very limited (lower than 0.3% of the fundamental current). Beside the topology of the power electronic interface, the output filter also affects the quality of the grid current. In this paper, a 5-level inverter is presented for grid integration of PV systems along with its output LCL filter design. Analytical calculation of losses for the 5-level inverter and the output LCL filter is presented. It is also compared to the H-bridge inverter in terms of output voltage and current harmonics, and the overall losses. Second-order generalized integral phase locked loop is used to synchronize the system with the grid voltage and the proportional resonant (PR) with harmonic compensation control method is used to control the output current. The proposed system has been simulated in the PSCAD/EMTDC environment to verify its operation and control.

KEYWORDS: LCL filter, Multilevel inverter, PV.

1. INTRODUCTION

PV as a renewable energy is a clean and safe solution to address the increasing demand for the electricity. The available data regarding the installed capacity of grid-integrated PV systems shows an exponential increase for the grid-connected PV systems. The PV panels are always equipped with power electronic converters in order to power conditioning. From the view point of grid connection, the PV systems are grid-connected or stand-alone (off-grid). Each of these categories has their special specifications and requirements. For example, in the case of grid-connected mode, there is essentially no need for energy storage systems (ESS), whereas for the off-grid application installation of an ESS is required to have a sustainable power.

In recent decades, the power converter systems for PV interface have attracted more and more attention. A review on the step-up transformer less converter topologies for grid interface of PV systems has been presented in Ref. [1]. A comprehensive review of the single-phase grid-connected inverters can be found in Ref. [2]. In Refs. [3-4] the optimal design of various transformer less PV inverter topologies has been considered where the economic and reliability are treated as the key factors. Various single-stage converters for off-grid PV lighting systems have been presented in Ref. [5]. These converters are also capable of charging a battery and also implementing the maximum power point tracking (MPPT). One can look at Ref. [6] to have an overview of the MPPT methods. The Z-source and quasi-Z-source inverter based topologies have also been considered as the PV system interface [7-10]. Nonlinear control of a single-phase grid-

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connected PV system has been presented in Ref. [11]. This work uses partial feedback linearization technique which linearizes the system partially. An AC-link converter based power electronic system for stand-alone PV/battery system has been presented in Ref. [12]. In this work, the output of the PV is converted to AC by a current-source type inverter and the AC load and also the battery are connected to the common AC link provided by the inverter at the output of PV. The optimal sizing of the PV system has been presented in Refs. [13-14]. It considers sizing of the battery energy storage and the PV panel so that the technical requirements are met and at the same time system is optimized economically. In Ref. [15] the genetic algorithm has been used in order to optimal design of the multiple inverter based grid-connected PV systems.

The multilevel converter, as a type of power converters, has some advantages over the classic converters. The advantages include improved output waveform quality, lower stresses on the switches and high-power handling capability [16-17]. The multilevel converters have also been applied in PV systems [18-19]. In Refs. [20-21] the diode-clamped multilevel converter has been used for stand-alone PV systems. Ref. [22] presented a diode-clamped based topology for single-phase grid-connected PV system in which the common mode current has been cancelled. Application of the cascaded H-bridge (CHB) multilevel converter for grid connection of the PV panels has been investigated in Refs. [23-27]. In Ref. [28] the application of modular multilevel converter (MMC) for grid-connected PV system has been studied. Other transformer less PV inverters are presented in Refs. [29-33].

In the CHB based PV systems, a PV panel is required for each H-bridge. Adjusting of the DC-link voltages for each H-bridge separately in order to get maximum power point tracking (MPPT) without using the DC-DC converter is a difficult task requiring extra sensors and complicated control algorithms. The NPC multilevel converters also have difficulties with balancing and adjusting the voltages of the DC-link capacitors. In this paper, a 5-level inverter with only one DC source requirement is adopted for the PV-grid interface application. Also, its comprehensive comparison with the three-level H-bridge inverter is presented. In Section 2, the multilevel inverter based PV system is described followed by the control method presented in Section 3. Output LCL filter design is presented in Section 4. Section 5 describes the efficiency analysis of the multilevel inverter based PV system. The simulation results and comparison with the H-bridge inverter are presented in Section 6 to verify the operation and control.

2. SYSTEM DESCRIPTION

Figure (1) shows the grid-connected PV system based on multilevel inverter. It includes a multilevel inverter and an output LCL filter. Although the multilevel inverter can be extended to higher number of voltage levels [34], the 5-level inverter is considered in this paper. The inverter uses 8 power electronic switches (IGBTs in this study) denoted by $S_1 \sim S_8$. The switches $S_1 \sim S_4$ operate in fundamental frequency (low-frequency switches) while the other switches operate with switching frequency (high-frequency switches). The interesting fact is that the high-frequency switches operate at lower voltage and the low-frequency switches operate at higher voltage. The switching combinations of the multilevel inverter are shown in Table 1. There are 10 different switching combinations that produce output voltage of zero. However, in this paper the aim is that the H-bridge ($S_1 \sim S_4$) to operate in fundamental frequency and therefore only two of the switching combinations are used for zero output voltage (S_1, S_4, S_6, S_7 for positive half cycle and S_2, S_3, S_6, S_7 for negative half cycle). For the voltage levels $V_{DC}/2$ and $-V_{DC}/2$ both available combinations should be used in order to balance the capacitors voltage. A proper PWM-based method automatically uses these redundant switching combinations. Therefore, the modulation of the inverter is not of concern. In the PV inverters, the leakage current is an important issue. The current is related to the common-mode voltage (CMV). As far as possible the CMV should be kept constant. For the proposed PV inverter if the aim is to limit the leakage current (keep CMV constant) some of the switching states shown in Table 1 should not be utilized.

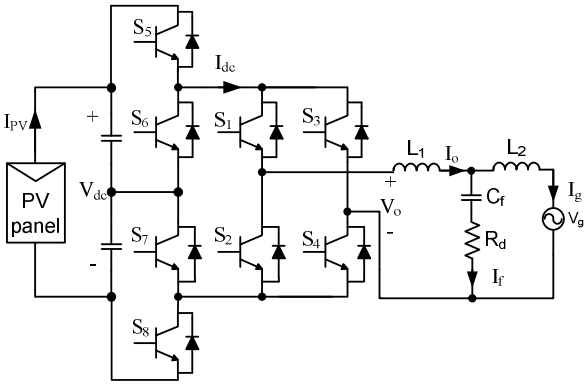


Fig. 1. The multilevel inverter based grid-connected PV system

Table 1. Switching Combinations for the 5-level Inverter.

Combination	ON switches	Output voltage
1	S_1, S_4, S_6, S_7	0
2	S_2, S_3, S_6, S_7	
3	S_1, S_3, S_6, S_7	
4	S_1, S_3, S_5, S_7	
5	S_1, S_3, S_5, S_8	
6	S_1, S_3, S_6, S_8	
7	S_2, S_4, S_6, S_7	
8	S_2, S_4, S_5, S_7	
9	S_2, S_4, S_5, S_8	
10	S_2, S_4, S_6, S_8	
11	S_1, S_4, S_5, S_7	$\frac{V_{DC}}{2}$
12	S_1, S_4, S_6, S_8	
13	S_2, S_3, S_5, S_7	$-\frac{V_{DC}}{2}$
14	S_2, S_3, S_6, S_8	
15	S_1, S_4, S_5, S_8	V_{DC}
16	S_2, S_3, S_5, S_8	$-V_{DC}$

As a result, the output voltage will be a three-level voltage introducing more harmonics at the inverter output. Therefore, the size of filter will also be larger. Comparing the proposed 5-level inverter with other multilevel inverters, the proposed topology uses only one dc source. The number of switches used in the proposed is the same as that of the other topologies; however, extra elements such as clamping diodes (as in diode-clamped topology) and flying capacitors (as in flying-capacitor topologies) are not required. Moreover, half of the switches in the proposed topology operate in fundamental frequency.

3. CONTROL SYSTEM

In the grid-connected PV inverters, the main control aim is to deliver a specific power to the grid. For the active power, this value (active power reference) is usually the result of the MPPT algorithm. The incremental conductance method for MPPT is used in this paper. In the proposed grid-connected PV system there is not any DC-DC converter and therefore MPPT is done by changing the active power reference (rather than changing the DC voltage) value and setting it to its maximum power point. The value of the reactive power reference is usually set to zero in normal operation conditions. The overall control system is shown in Fig. 2. The second-order generalized integrator based phase locked loop (SOGI-PLL) [35], (Fig. 2(a)), is used in order to synchronize the control system with the grid voltage and generate orthogonal signals, v_α and v_β. It has been demonstrated that this PLL method has enhanced performance for single-phase grid-connected applications [36]. As shown in Fig. 2(b), the control objective is to deliver a specified active and reactive power (P_{ref}, Q_{ref}) to the grid. P_{ref} is obtained from the MPPT algorithm and Q_{ref} is usually set to zero in normal operating condition. The active and reactive power controllers are the proportional-integral (PI) type. The outputs of these controllers are mathematically processed to obtain the reference value of the grid current ($i_{g,ref}$).

The proportional-resonant (PR) with harmonic compensation current controller is used. The transfer function of this controller can be written as:

$$G_{PR} = K_p + K_1 \frac{s}{s^2 + \omega_0^2} + K_3 \frac{s}{s^2 + (3\omega_0)^2} + K_5 \frac{s}{s^2 + (5\omega_0)^2} + K_7 \frac{s}{s^2 + (7\omega_0)^2} \quad (1)$$

where, ω_0 is the fundamental angular frequency.

The output of the current controller is the reference voltage (v_{ref}) for inverter modulation. As the figure indicates, the switches S_1 and S_4 are turned on when $v_{ref}>0$ (positive half cycle) and the switches S_2 and S_3 are turned on when $v_{ref}<0$ (negative half cycle).

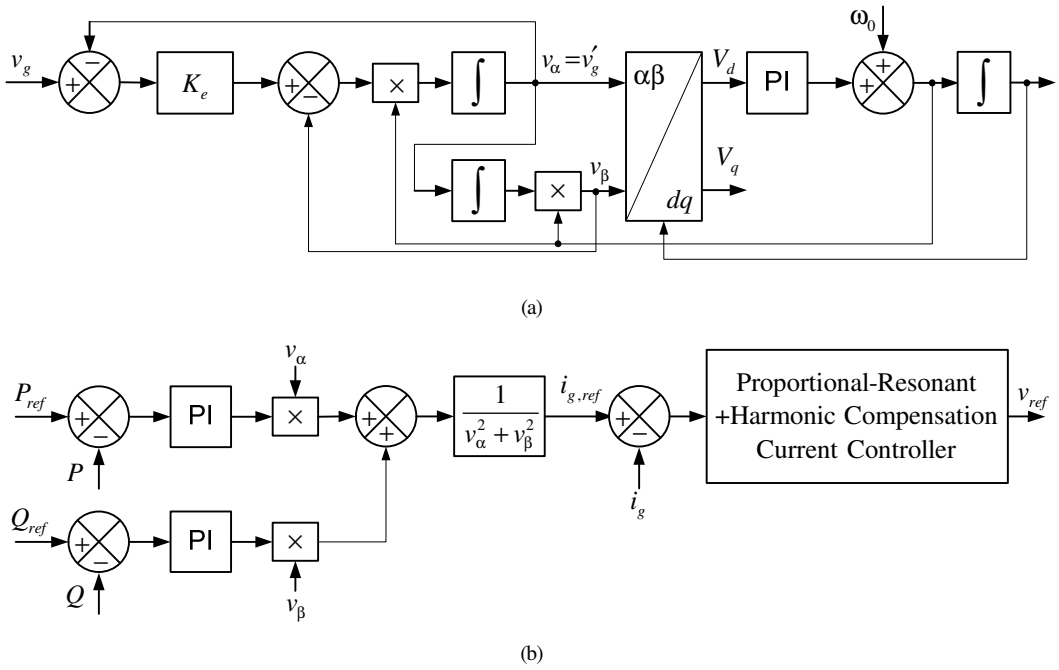


Fig. 2. Control system, (a) SOGI-PLL, (b) Power controllers and PR current controller

To generate the switching signals for the switches S_1 ~ S_8 the absolute value of the reference voltage is compared with two triangular waveforms (varying between 0 and 1) with 180° phase difference. The details are clear in Fig. 3.

Using the mentioned PWM method, the output voltage of the 5-level inverter can be written as Eq. (2) shown in bottom of this page. Where, v_o is the output voltage of the inverter; M is the modulation index; V_{DC} is the DC-link voltage, and J_ν is the Bessel function of first kind. Also, ω_c is the angular frequency of carrier waveforms.

Using (2), the magnitude of the h^{th} output voltage harmonic ($V_{o,h}$) can be obtained as:

$$V_{o,h}\Big|_{h=n\frac{\omega_c}{\omega_0}\pm\nu} = \frac{2V_{DC}}{n\pi} J_\nu(n\pi M) \qquad (3)$$

where, ω_s is the effective angular frequency of switching which is the double of the angular frequency of the carrier waveforms (ω_s = 2 ω_c) for the 5-level inverter studies in this paper.

4. THE OUTPUT LCL FILTER DESIGN

In order to design LCL filter for a grid-connected inverter special criteria and constraints should be taken into account.

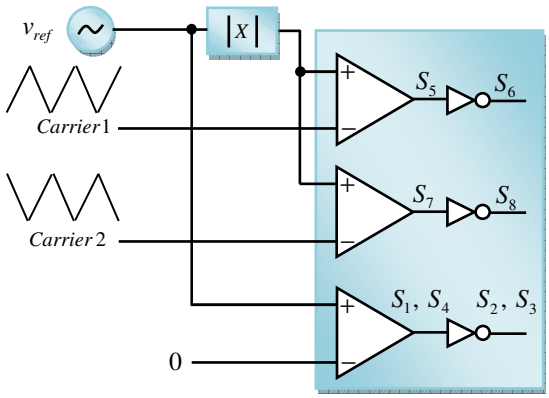


Fig. 3. The PWM implementation of the 5-level inverter

The most common criteria and constraints are [37-39]:

- The upper limit for the filter capacitor ($C_{f,\,max}$) is 5% of its base value which is defined as:

$$v_o(t) = MV_{DC}\sin(\omega_0 t) + \sum_{n=2,4,\cdots}^{\infty}\sum_{\nu=1,3,\cdots}^{\infty}\left\{\frac{2V_{DC}}{n\pi}J_\nu(n\pi M)\left[\sin(n\omega_c t + \nu\omega_0 t) - \sin(n\omega_c t - \nu\omega_0 t)\right]\right\} \qquad (2)$$

$$C_{f,\max} = \frac{0.05 P_n}{\omega_0 V_g^{\,2}} \tag{4}$$

where, P_n is the rated power and V_g is the RMS grid voltage.

Considering Eq. (4):

$$C_f \le C_{f,\max} \tag{5}$$

- The value of the inverter side inductor (L_1) should be chosen in a way that its current ripple remains in a specific limit, e.g.:

$$0.15 \le \frac{\Delta I_o}{I_n} \le 0.4 \tag{6}$$

where, ΔI_o is the peak-to-peak ripple current and I_n is the magnitude of the rated grid current.

The current ripple for the 5-level inverter can be obtained as:

$$\Delta I_o = \frac{V_{DC}}{16 L_1 f_c} \tag{7}$$

where, f_c is the frequency of the carrier waveforms.

Using Eqs. (6) and (7), the following constraint is obtained for the inverter side inductor:

$$\frac{V_{DC}}{6.4 f_c I_n} \le L_1 \le \frac{V_{DC}}{2.4 f_c I_n} \tag{8}$$

- The value of the grid side inductor is dominated by the attenuation of the grid current high-frequency components. The level of attenuation level depends on the standards and short circuit ratio of the grid. For example, if ratio of the grid short circuit current to its rated current is lower than 20, the current harmonics in order of higher than 35th should be limited to 0.3% of the rated fundamental current.

The transfer function of the grid current to inverter output voltage can be obtained as:

$$G_{i_g v_o}(s) = \left.\frac{i_g(s)}{v_o(s)}\right|_{v_g(s)=0} = \frac{R_d C_f s + 1}{L_1 L_2 C_f s^3 + R_d C_f (L_1 + L_2) s^2 + (L_1 + L_2) s} \tag{9}$$

Using this transfer function and considering the magnitude of inverter output voltage harmonic contents, Eq. (3), the amplitude of the current harmonics ($I_{g,h}$) can be obtained as Eq. (10) shown at the bottom of this page.

where, $\omega_h = n\omega_c \pm \nu\omega_0$ is the angular frequency of the h[th] harmonic.

For the 5-level inverter used in this paper, the dominant voltage harmonics appear around the double of the carrier frequency. Therefore, the dominant current harmonics will also appear in the same frequency range. As a consequence, it is enough to check several odd-order harmonics around the mentioned frequency to find an acceptable range for grid side inductor. In other words, the value of L_2 should be chosen so that the following constraint is met:

$$\max_{\substack{\nu=1,3,5 \\ \omega_h = 2\omega_c \pm \nu\omega_0}} \left\{ \frac{I_{g,h}}{I_n} \right\} \le 0.3\% \tag{11}$$

- Using Eqs. (10) and (11), the value of L_2 should satisfy the relation Eq. (12) indicated at the bottom of this page. The resonance frequency of the filter (ω_r) should be in the following range:

$$10\omega_0 < \omega_r = \sqrt{\frac{L_1 + L_2}{C_f L_1 L_2}} < \frac{1}{2}\omega_s \tag{13}$$

- The value of $L_1 + L_2$ should be lower than 10%.

For the 220V, 2kW, 5-level inverter with $V_{DC} = 320V$, $f_c = 5kHz$, and $f_0 = 50Hz$ the value of filter components are obtained as:

Using Eq. (4), the maximum value of the filter capacitor is:

$$C_{f,\max} = \frac{0.05 \times 2000}{2\pi \times 50 \times 220^2} = 6.58\mu F \tag{14}$$

Considering Eq. (8), the constraint for inverter side inductor is obtained as Eq. (15).

$$I_{g,h} = \left| G_{i_g v_o}(j\omega_h) \right| \times V_{o,h} = \frac{2 V_{DC} J_\nu(n\pi M) \times \sqrt{1 + (\omega_h R_d C_f)^2}}{n\pi \sqrt{\left[\omega_h (L_1 + L_2) - \omega_h^3 L_1 L_2 C_f \right]^2 + \left[\omega_h^2 R_d C_f (L_1 + L_2) \right]^2}} \tag{10}$$

$$\max_{\substack{\nu=1,3,5 \\ \omega_h = 2\omega_c \pm \nu\omega_0}} \left\{ \frac{\sqrt{1 + (\omega_h R_d C_f)^2}}{I_n \sqrt{\left[\omega_h (L_1 + L_2) - \omega_h^3 L_1 L_2 C_f \right]^2 + \left[\omega_h^2 R_d C_f (L_1 + L_2) \right]^2}} \times \frac{2 V_{DC} J_\nu(2\pi M)}{2\pi} \right\} \le 0.3\% \tag{12}$$

$$\frac{320}{6.4\times5000\times12.86} \le L_1 \le \frac{320}{2.4\times5000\times12.86} \qquad (15)$$
$$0.778mH \le L_1 \le 2.074mH$$

Considering 25% ripple for the current, the value of the L_1 is obtained to be 1.25mH. For the capacitor $C_f = 4.7\mu F$ is considered. Also, for L_2 the value of 3 mH is considered. The value of R_d is chosen to be 10 Ω. With these values of the filter components the resonance frequency of the filter is 2471 Hz which is in the range stated by Eq. (13). Also, L_1+L_2=5.5% which is lower than the maximum limit of 10%. Also, the value of grid current harmonics obtained analytically using Eq. (10) will be shown in the Section 6 indicating that the value of grid side current harmonics is lower than 0.3% of the fundamental current.

5. EFFICIENCY ANALYSIS

In order to calculate the efficiency of the whole system, the efficiency of individual components should be considered. The efficiency of the whole system in terms of the efficiency of the components can be written as follows:

$$\eta_t = \eta_i \eta_f \qquad (16)$$

where, η_t, η_i, and η_f are the total efficiency, efficiency of the inverter, and efficiency of the filter, respectively.

5.1. Calculation of the inverter losses

For calculating the efficiency, the power losses are calculated. Generally, two kinds of losses are associated with power electronic devices; conduction losses and switching losses. The conduction loss of a typical device (P_c) can be estimated as follows [40]:

$$P_c = \frac{1}{T}\int_0^T f(\mathrm{t})\left(V_{on} + r_{on} i(\mathrm{t})^{\beta}\right) i(\mathrm{t}) dt \qquad (17)$$

where, T is the fundamental period, $f(t)$ is the switching function of the device; its value is 1 if the device in current path otherwise, its value is 0. V_{on} and r_{on} are the on-state forward voltage drop and the resistance of the device, respectively, which can be obtained from the device datasheet. β is a constant related to the device type. Also, $i(t)$ is the current through the device.

In order to calculate the switching losses of a converter, usually the lost energy during the turn-on and turn-off processes are considered. The energy lost during turn-on ($E_{sw,\ on}$) and turn-off ($E_{sw,\ off}$) process for a typical device can be estimated as follows, respectively [41]:

$$E_{sw,on} = \frac{1}{6} V_{sw} I_{sw} t_{on} \qquad (18)$$

$$E_{sw,off} = \frac{1}{2} V_{sw} I_{sw} t_{off} \qquad (19)$$

The Eqs. (17) - (19) can be used for power loss calculation in inverter by extending them to all of the devices.

The inverter has two parts; the H-bridge part including the switches S_1 ~ S_4 and the other part including the switches S_5 ~ S_8. The H-bridge part operates in fundamental frequency and also it operates under zero voltage condition since the zero voltage can be obtained by turning on the switches S_6 and S_7. Therefore, the H-bridge part has no switching power losses. The conduction power loss of the H-bridge can be written as follows:

$$P_{c,H} = \frac{1}{\pi}\left[\int_0^{\phi} 2\left[V_{on,D} + r_{on,D} i(\mathrm{t})^{\beta_D}\right] i(\mathrm{t}) d(\omega t) + \int_{\phi}^{\pi} 2\left[V_{on,T} + r_{on,T} i(\mathrm{t})^{\beta_T}\right] i(\mathrm{t}) d(\omega t)\right] \qquad (20)$$

where, ϕ is the displacement angle between the output voltage and current. It should be considered that the switches S_5 and S_8 have the same operational conditions, therefore, their losses are the same and it is enough to calculate the losses of one of them. The same case is valid for the two switches S_6 and S_7. Consequently, the losses of the two switches S_5 and S_6 are calculated and the result is doubled. The conduction power loss of the switches S_5 ~ S_8 ($P_{c,\,58}$) can be written as follows:

$$P_{c,58} = \frac{1}{T}\left[\int_0^T 2 f_{D5}(\mathrm{t})\left[V_{on,D} + r_{on,D} i_{dc}(\mathrm{t})^{\beta_D}\right] i_{dc}(\mathrm{t}) dt + \int_0^T 2 f_{T5}(\mathrm{t})\left[V_{on,T} + r_{on,T} i_{dc}(\mathrm{t})^{\beta_T}\right] i_{dc}(\mathrm{t}) dt + \int_0^T 2 f_{D6}(\mathrm{t})\left[V_{on,D} + r_{on,D} i_{dc}(\mathrm{t})^{\beta_D}\right] i_{dc}(\mathrm{t}) dt + \int_0^T 2 f_{T6}(\mathrm{t})\left[V_{on,T} + r_{on,T} i_{dc}(\mathrm{t})^{\beta_T}\right] i_{dc}(\mathrm{t}) dt\right] \qquad (21)$$

where, f_{Di} and f_{Ti} is the switching function of the diode and transistor of the i^{th} switch.

Also, from the view point of the switching losses, the switches S_5 and S_8 have the same conditions. The same is true for the switches S_6 and

S_7. Therefore, extending Eqs. (18) and (19) to the switches S_5 and S_6, the switching losses of the switches $S_5 \sim S_8$ ($P_{sw,58}$) can be obtained as follows:

$$P_{sw,58} = \frac{2}{T}\left\{\frac{1}{6}V_{DC}\sum_{i=1}^{N}\left[t_{on}i_{dc}(\mathrm{t_i}) + 3t_{off}i_{dc}(\mathrm{t_i})\right]\right\} \quad (22)$$

where, N is the number of switching during a period.

5.2. Calculation of the filter losses

In order to damp the possible oscillations around the resonance frequency of the filter, the two passive and active damping schemes can be used. In the active damping, a control loop is added to the control system by feeding back the capacitor current. This solution is lossless; however, it contributes to more complicated control system. In the passive damping scheme, a resistor is inserted in the filter circuit (usually in series with the capacitor). Although this solution contributes to the power losses, it provides a simple and popular way to damp the oscillations. In this paper, the passive damping is used by inserting a resistor in series with the capacitor. The value of the resistor should be selected in a way that the damping is effective, the losses remain within a reasonable margin, and also the impedance of the parallel branch (including capacitor and resistor) around the switching frequency is not too high.

The losses of the filter can be written as:

$$P_d = R_d\left(I_{f,1}^2 + \sum_{h=2}^{\infty} I_{f,h}^2\right) \quad (23)$$

in which, $I_{f,1}$ is the RMS value of the fundamental component of current passing through the parallel branch. $I_{f,h}$ also denotes the RMS value of h^{th} harmonic of the parallel branch current. They could be estimated as:

$$I_{f,1} = \frac{V_{g,rms}}{\sqrt{R_d^2 + \left(\frac{1}{\omega_0 C_f}\right)^2}} \quad (24)$$

$$I_{f,h} = \frac{\omega_h L_2 \times V_{o,h,rms}}{\sqrt{\left[R_d(L_1+L_2)\omega_h\right]^2 + \left[\frac{L_1+L_2}{C_f} - L_1L_2\omega_h^2\right]^2}} \quad (25)$$

6. SIMULATION RESULTS AND COMPARISON

In this section, the simulation results of a 2 kW, 220 V, 50Hz system carried out using PSCAD/EMTDC software are presented. The value of L_1, C_f, L_2 and R_d is 1.25 mH, 3 mH, 4.7 μF, and 10Ω, respectively. For the active and reactive power controllers the parameters $K_P = 0.02$ and $K_I = 50$ are used. Also, for the PR current controller the parameters $K_P = 10$ and $K_R = 2000$ are considered. The control parameters are obtained on the trial-error basis. Beside the 5-level inverter, an H-bridge inverter with the same data and the filter value is simulated and analyzed for comparison purpose.

Figure 4 shows the active and reactive power delivered to the grid. For t<0.5 s, the reference active power is 2 kW. At t = 0.5 s the reference active power decreases to 1.5 kW. The reference value for reactive power is zero. The figure indicates that the control system tracks the reference values of active and reactive power.

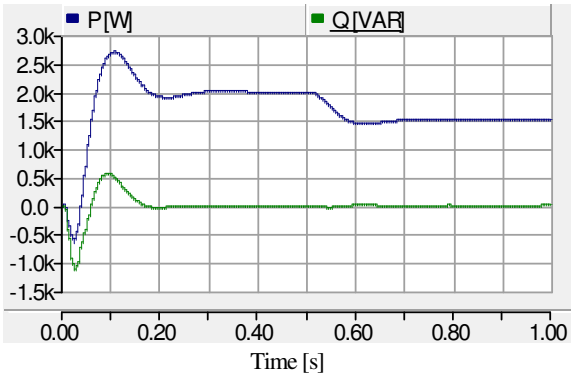


Fig. 4. Active and reactive power delivered to the grid

Figure 5 shows the 5-level output voltage of the inverter. The analytical based output voltage harmonics around the even multiplier of the carrier frequency is shown in Fig. 6(a) and Fig. 6(b), for the 5-level inverter and the H-bridge inverter, respectively. As the figure shows, the magnitude of the voltage harmonics of the 5-level inverter is almost half of that of the H-bridge inverter. This is because of the fact that in the 5-level inverter the switching is accomplished with the step voltage of 160 V, whereas, in the H-bridge inverter the switching voltage step is 320 V.

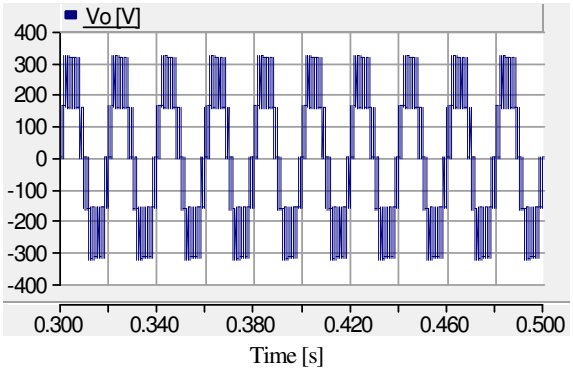
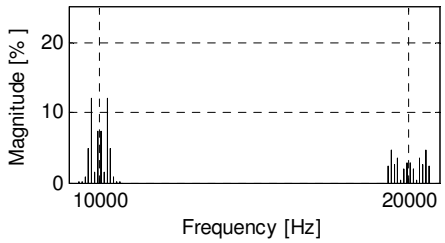
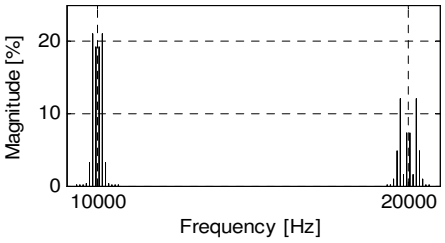


Fig. 5. Output voltage of the 5-level inverter



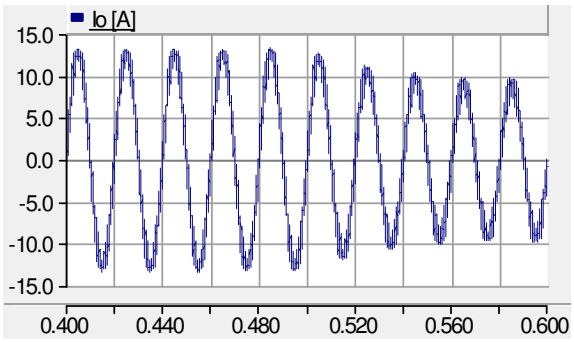
(a)



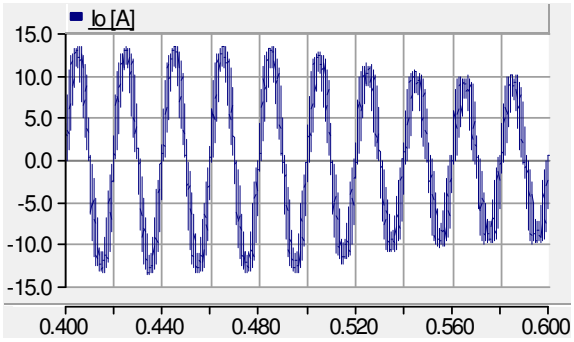
(b)

Fig. 6. Output voltage harmonics (a) 5-level inverter, (b) H-bridge inverter

The output current of the inverter for the 5-level inverter and the H-bridge inverter are shown in Fig. 7(a) and Fig. 7(b), respectively. Clearly, the ripple and harmonics of the output current of the H-bridge inverter are considerably higher than that of the 5-level inverter. The grid current for the 5-level inverter and H-bridge inverter is shown in Fig. 8(a) and Fig. 8(b), respectively. As the figure indicates, the disturbance of the grid current in the case of the 5-level inverter is lower than that of the H-bridge inverter. The change in the magnitude of the current is because of the change in the values of active power delivered to the grid. The harmonic contents of the grid current around the even multiples of the carrier frequency is shown in Fig. 9(a) and Fig. 9(b), for the 5-level inverter and the H-bridge inverter, respectively. As the figure indicates, for the 5-level inverter the magnitudes of the current harmonics are much lower than that of the H-bridge inverter. Moreover, the magnitude of the current harmonics of the 5-level inverter is lower than 0.3% of the fundamental current which is an upper limit for high-order harmonic currents.

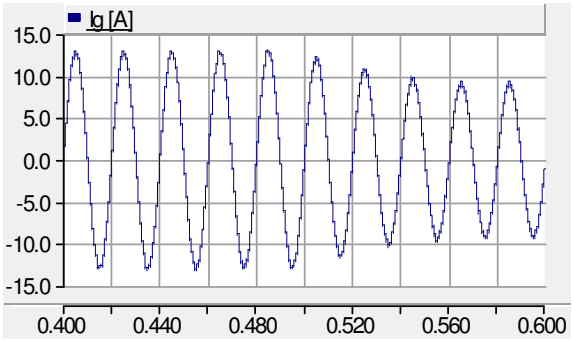


(a)

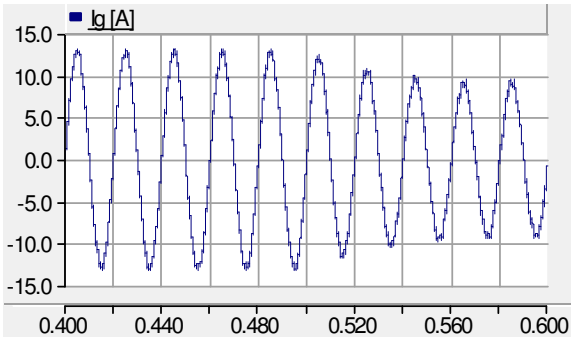


(b)

Fig. 7. Output current, (a) 5-level inverter, (b) H-bridge inverter



(a)



(b)

Fig. 8. Grid current, (a) 5-level inverter, (b) H-bridge inverter

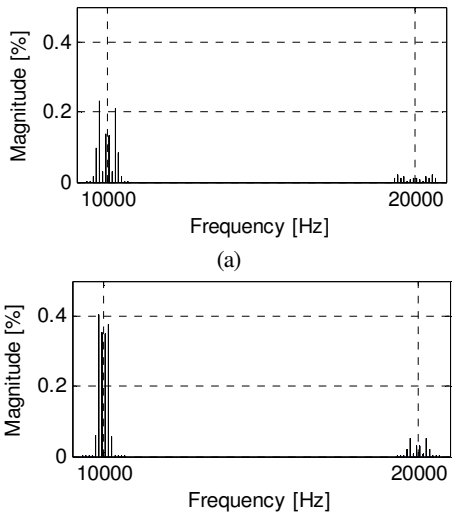


Fig. 9. Grid current harmonics, (a) 5-level inverter, (b) H-bridge inverter

Current through the filter capacitor for the 5-level inverter and the H-bridge inverter is shown in Fig. 10(a) and Fig. 10(b), respectively. As the figure indicates, the current through the filter capacitor for the 5-level inverter is almost half of that of the H-bridge inverter. Considering that the damping resistance is in the same branch, it can be expected that the power losses of filter in the 5-level inverter would be much lower than that of the H-bridge inverter.

The DC-link voltage (PV voltage) is shown in Fig. 11.

The efficiency analysis method given in section 5 is used to estimate the power losses and efficiency of the system. For calculation of losses data given in Section 4 is used. Also, the following data is used:

$$V_{on,T}=1.2V,\ V_{on,D}=0.5V,\ r_{on,T}=0.1\Omega,\ r_{on,D}=0.06\Omega$$

$$\beta_T=0.55,\ \beta_D=0.7,\ t_{on}=70ns,\ t_{off}=200ns$$

Table 2 summarizes the results of the power loss calculations and harmonics analysis for the two 5-level and H-bridge inverter. As the table indicates, the switching power loss of the H-bridge inverter is higher since the switches operate with full DC-link voltage (320 V); however, the PWM switches of the 5-level inverter operate at half of the DC-link voltage (160 V). The conduction power loss of the 5-level inverter is higher than that of the H-bridge inverter. This is because of the fact that in the 5-level inverter there are two extra devices in current path in any instant of time.

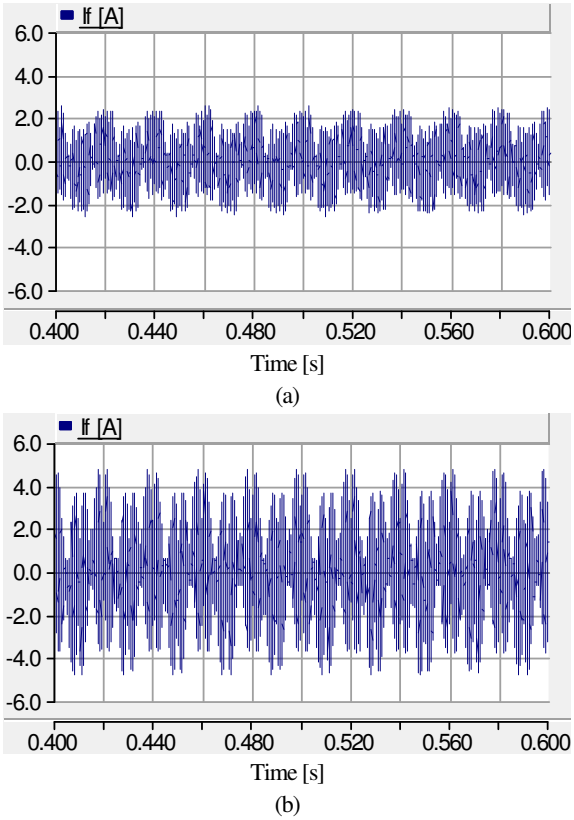


Fig. 10. Current through the filter capacitor, (a) 5-level inverter, (b) H-bridge inverter

As expected, the filter power loss of the H-bridge inverter is considerably higher than that of the 5-level inverter due to higher current through the parallel branch of the filter.

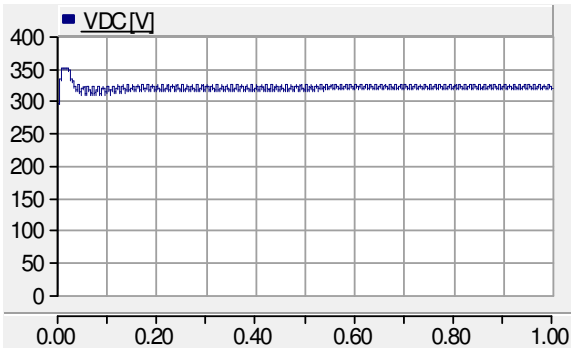


Fig. 11. DC-link voltage

From total efficiency point of view, the H-bridge inverter is slightly better than the 5-level inverter. However, the output current ripples, total harmonic distortion (THD) of the grid current, and the magnitude of grid current dominant harmonic in 5-level inverter is considerably lower than that of the H-bridge inverter. It should be noted that the number

of power-electronic switches used in the proposed topology is twice of that of the H-bridge topology.

There different types of filter for grid-connected PV systems. However, the most common types of filters for grid-connected inverters are the L and the LCL types. In the L type filter, only an inductance inserted between the inverter and the grid. This is the simplest and cheapest filter; however, its performance from the view point of harmonics may not be satisfactory. The type of the filter does not affect the switching and conduction losses of the inverter, considerably. However, the type of filter directly influences the harmonics and THD of the grid current. For example, for the proposed 5-level inverter with L type filter (4.25mH) the grid current THD is %2.35 (instead of %1.42 for LCL filter) and the magnitude of the grid current dominant harmonic is about %1.15 (instead of %0.22 for LCL filter).

Table 2. Comparison of the 5-level and the H-bridge inverters under rated power delivery

	H-bridge inverter	5-level inverter
Switching losses [W]	6.5	3.2
Conduction losses [W]	25.4	47.9
Filter losses [W]	20.3	6.2
Total losses [W]	52.2	57.3
Efficiency [%]	97.39	97.13
Output current ripple [%]	52.8	25.3
THD of grid current	2.76	1.42
Magnitude of grid current dominant harmonic [%]	0.37	0.22

7. CONCLUSIONS

In this paper, the comparison of a multilevel inverter and a three-level H-bridge inverter has been presented for grid integration of PV system. The output LCL filter design as well as the harmonic analysis of the output voltage and current has been presented for the multilevel inverter.

Also, the analytical efficiency analysis has been provided. The two inverters (multilevel and H-bridge) have been compared from different points of view such as losses and efficiency, output current ripple, and grid current THD and harmonics. As the results showed, the multilevel inverter has much lower harmonics and current ripple. However, the efficiency of the H-bridge inverter is slightly higher than that of the multilevel inverter. The simulation results verified the performance of the adopted control scheme, SOGI PLL, PI power controller and proportional-resonant plus harmonic compensation current controller.

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