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Two Inputs Five-Level Quasi-Z-Source Inverter

A. Baghbany Oskouei[1], *M. R. Banaei*[1,*], *M. Sabahi*[2]

[1]*Department of Electrical Engineering, Azarbaijan Shahid Madani University, Tabriz, Iran.*
[2]*Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran*.

Abstract- *This paper combines quasi-Z-source into a typical five-level inverter, which includes two dc voltage sources, two quasi-Z-sources and five switching devices. In this structure, the output voltage amplitude is not limited to dc voltage source and it can be increased by quasi-Z-source. Besides, due to nature of Z-source families, this new structure is reliable and higher efficiency. Also, in this inverter, two quasi-Z-networks can be controlled independently. This paper also proposes new switching algorithms for proposed five-level dual quasi-Z-Source inverter based on pulse width modulation (PWM) and selective harmonic elimination method (SHEM) algorithms. The performance of proposed inverter and switching algorithm are validated with simulation results using MATLAB/SIMULINK software and experimental results based PCI-1716 data acquisition system.*

Keyword: Two inputs five-level inverter, quasi-Z-source, PWM, SHEM, shoot-through implementation.

1. INTRODUCTION

Recently, industry has begun to demand higher power equipments. Controlled high power ac drives are usually connected to the medium voltage networks. Meanwhile, direct connection of a single switching device to medium voltage grid is very hard. Then, multilevel inverter as a solution has been proposed, in recent years [1-3]. The three common topologies for multilevel inverter are as: diode clamped, flying capacitor, and cascaded H-bridge inverters. The total switching device power (TSDP) is used for comparison of rating of converters, where it is calculated as:

$$TSDP = \sum_{j=1}^{N} Cj \,.\, Vsj \,.\, Isj \qquad (1)$$

Where, N is the number of switching devices, V_{sj} and I_{sj} are voltage and current stress of device, respectively. C_j is cost factor and defined 1 for semiconductor device, and 0.5 for diode.

The modulation methods for multilevel inverters can be classified based on switching frequency: methods with high switching frequency and methods with low switching frequency. Methods with high switching frequency do many switchings in one period of the fundamental output voltage, and methods with low switching frequency perform very low commutations of switching devices during one cycle of the output voltages. A very popular method is carrier based pulse width modulation (PWM), and another interesting one is the space vector modulation (SVM). Representatives of low switching frequency family are selective harmonic elimination method (SHEM) and space vector control (SVC). Selective harmonic elimination method is based on solving a series of trigonometric equations result from the Fourier expansion of the inverter output voltage [4-8].

Growing environmental concerns and attempts to decrease dependency on fossil fuel sources are bringing renewable energy resources to the tendency of the electrical power sector [9]. In the conventional renewable energy system configurations, a dc-dc converter is used, where these systems are connected to the dc-link through this dc-dc converter. The main purpose of using this converter is voltage increase and production of a control freedom to maximum power point tracking (MPPT) [10]. Later, Z-source as a novel dc-dc converter was proposed in 2002 [11]. This type of converter, addition to capability of voltage boosting, creates a large degree of freedom, utilizing Z-impedance network between the dc source and inverter circuitry. The Z-source inverter, as well as delivered quasi-Z-source inverters, has one state to short circuit any leg of inverter, named as shoot-through state, and uses it for boosting output voltage [12-14]. So, reliability of the system is greatly improved. Also, Due to lack of dead

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∗Corresponding author:
E-mail: m.banaei@azaruniv.edu (M. R. Banaei)

time in this configuration, inverter output distortion is reduced [5], [15].The quasi-Z-source inverter is a kind of improved Z-source topology. Such Z-source inverter, in addition to all the advantages of Z-source inverter, has some unique merits, such as lower component rating, constant input current, and less switch pulse. Also, in this improved Z-source topology, the voltage of one capacitor of the quasi-Z- network is greatly reduced, compared to conventional Z-source [16-17].

In 2008, literature [16] proposed four structures as quasi-Z-source inverters, which a kind of improved Z-source topology. This new converter, not only inherits all the advantages of Z-source inverter, but also has some unique merits, such as lower component rating, constant input current, less switch pulse and also the voltage of one capacitor at the Z-source network is greatly reduced. Then, a new Z-source based inverter was presented in Ref. [18]. Use of Z-source in multilevel structure was reported in [5]; which suggested a new inverter topology based on mixture of cascaded basic units and one H-bridge. Then, in Ref. [19] was presented a new topology of cascaded transformer-based multilevel inverter using Z-source. Combination of quasi-Z-source into five-level inverter using coupled inductors was proposed in Refs. [12], [20] and [21] are the other literatures using SVM and SVC algorithms for switching of multilevel Z-source based inverters.

This paper, at first, presents a five-level inverter with one main H-bridge inverter, one auxiliary switching device, and two dc sources proposed in Ref. [22]. The main goal of this inverter is to reduce the number of switching devices. Then, a Z-source based inverter is suggested, which it combines quasi-Z-source into later five-level inverter. Pulse width modulation (PWM) and selective harmonic elimination method (SHEM), as selected switching algorithms, are used to switch of it. Besides, it is explained how these algorithms cause boosting of output voltage in the new structure. Theoretical analysis, simulation and experimental results are presented to show the validity of the proposed inverter with new control strategies.

2. QUASI-Z-SOURCE INVERTER

The quasi-Z-source inverter is shown in Fig. 1. This structure compared to the Z-source inverter, has merits as lower dc voltage on capacitor C_2 and continuous input current [16]. This member of Z-source family operates in two modes: shoot-through and non shoot-through state. In the non shoot-through state mode, only one switching device in each phase arm conducts. During this mode, the inverter is controlled such a standard inverter. The shoot-through state mode occurs when both switching devices in at least one arm of inverter are turned on. When a shoot-through state is ordered, the related switching devices are turned on to initiate inductive boosting of the quasi-Z-source impedance network, and when the inverter is ordered to enter to non shoot-through state mode, this stored inductive energy, together with energy from the dc source, is released to the load, resulting boosting of the inverter [23].

With the analysis of circuit output voltage of quasi-Z-network, v_i is obtained as:

$$v_i = \left(\frac{1}{1-2\frac{T_{st}}{T}} \right) V_{dc} \tag{2}$$

$$B = \frac{1}{1-2\frac{T_{st}}{T}} \tag{3}$$

Where T, T_{st} and B are period of switching, total shoot-through state period, and boost factor, respectively.

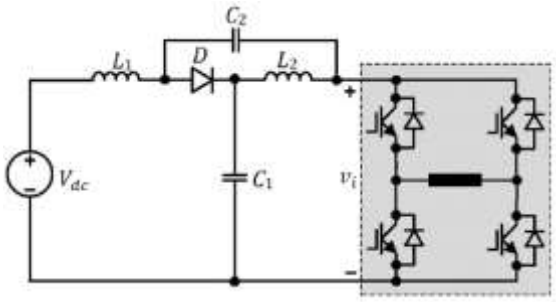


Fig. 1. Quasi-Z-source inverter structure.

During the non shoot-through state mode the input voltage appears across the capacitor and no voltage appears across the inductor (just a pure dc current flow through the inductors). During non shoot-through state mode, the inductor voltage is same as capacitor voltage and inductor current increases linearly. The job of the inductor is to limit the current ripple during the shoot-through state mode.

Inductors value may be calculated as:

$$L_1 = \frac{V_{dc}T}{\Delta I_{L1}} \left(\frac{1+D}{1-2D} \right) D \tag{4}$$

$$L_2 = \frac{V_{dc}T}{\Delta I_{L2}} \left(\frac{1-D}{1-2D} \right) D \tag{5}$$

Where ΔI_{L1} and ΔI_{L2} are the assumed current ripple of inductor L_1 and L_2, respectively.

The capacitor absorbs the current ripple and achieves quite a stable voltage. The inductor is charged by the capacitor during the shoot-through state mode. The capacitors value may be calculated as:

$$C_1 = \frac{I_{L2}T}{\Delta V_{C1}} D \quad (6)$$

$$C_2 = \frac{I_{L1}T}{\Delta V_{C2}} D \quad (7)$$

where I_{L1} and I_{L2} are the average current of inductor L_1 and L_2 and ΔV_{C1} and ΔV_{C2} are the assumed voltage ripple of capacitor C_1 and C_2, respectively.

3. PRESENTED FIVE-LEVEL INVERTER

The main goal of this inverter is to reduce the number of switching devices without changing the staircase nature of the output voltage. So, the same number of dc sources is used in this topology as conventional cascaded H-bridge inverter. The presented five-level inverter is shown in Fig. 2 [22]. From this figure, it is observed that this inverter has a main H-bridge inverter (S_2-S_5), and one auxiliary switch S_1. It is evident that the number of dc voltage sources is two, where it is equal to conventional five-level cascaded H-bridge inverter, and the number of switching devices is five, where conventional five-level cascaded H-bridge has eight switching devices.

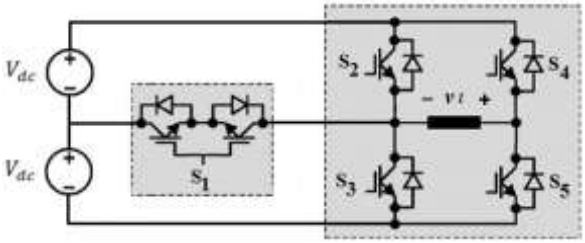


Fig. 2. Presented five-level inverter.

In this inverter, the switching devices in one arm must not turn on simultaneously. For instance, S_3 must be turn off, if S_2 is turned on. But, it does not mean that the switching devices in one arm are complementary, necessarily, because there are some instants that both of them are turned off.

Table 1. Switching states and load voltage of the presented five-level inverter

S_1	S_2	S_3	S_4	S_5	v_l
0	0	1	1	0	$+2V_{dc}$
1	0	0	1	0	$+V_{dc}$
0	1	0	1	0	0
0	0	1	0	1	0
1	0	0	0	1	$-V_{dc}$
0	1	0	0	1	$-2V_{dc}$

It occurs when S_1 is ON, and just for first arm (S_2, S_3). The load voltage of the inverter can be summarized in Table 1. For convenience, the number "1" is used to denote the ON state of switching device and "0" is used to denote the OFF state. As observed, this inverter can produce five voltage levels at its load terminal. From Table 1, it should be pointed out that the switching state of S_4/S_5 must be 1/0, if $v_l \geq 0$, and it must be 0/1 if $v_l \leq 0$. This means S_4 and S_5 are switched at the fundamental frequency and the switching losses of them are minimum. Also, Table 1 shows that the switching states of other switching devices repeat in $v_l \geq 0$ and $v_l \leq 0$. Then switching pattern in this inverter is very simple.

The modulation methods which used in this five-level inverter can be pulse width modulation (PWM) and selective harmonic elimination method (SHEM). In this paper these two modulation methods are introduced and they are analyzed in detail for this inverter.

3.1. PWM

From the above analysis, the switching state of S_4/S_5 is decided by the sign of v_l^* (the reference of v_l): S_4/S_5 is 1/0 if $v_l^* \geq 0$ and S_4/S_5 is 0/1 if $v_l^* \leq 0$. This is very easy to implement. The switching state of the other switching devices is based on a comparison of a sinusoidal reference waveform with triangular carriers. Modulation waveforms to switching of the other switching devices of the inverter are shown in Fig. 3.

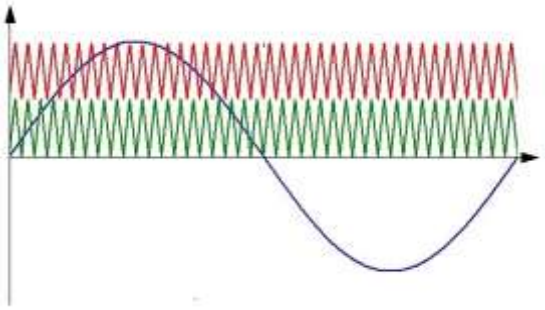


Fig. 3. Modulation waveforms to switching (PWM).

There is one sinusoidal reference signal and two triangular carriers. Each carrier is related to each positive level. It is known, there are two positive levels, $+2V_{dc}$ and $+V_{dc}$. $+2V_{dc}$ is related to upper carrier and $+V_{dc}$ is related to lower one. The gate signal for S_1 is generated by comparing two carrier signals with reference signal, as if modulus of reference signal is between two carriers, S_1 is ON. Also, the gate signals for S_2 and S_3 are generated by comparing reference signal with lower carrier in positive levels. In negative levels, they are obtained by comparing reference signal with upper carrier.

This switching condition is summarized as below:

if $r \geq 0$ then $S_4=1$ else $S_5=1$;

if $C_1 < |r| < C_2$ then $S_1=1$;

if [0<r<C_1 or -r>C_2] then S_2=1;

if [0<-r<C_1 or r>C_2] then S_3=1;

where C1 and C_2 are lower and upper carriers, respectively, and, r is sinusoidal reference signal.

3.2. SHEM

In this algorithm, the control of the five-level inverter is to choose two switching angles to generate quarter wave, symmetric, stepped load voltage waveform [8], [24-25]. Fig. 4 shows such waveform with five level and two switching angles, Θ_1 and Θ_2. The Fourier series expansion of the five-level stepped waveform using fundamental frequency in Fig. 4 is given by:

$$V_l(\omega t) = \sum_{n=1,3,\ldots}^{\infty} \frac{4V_{dc}}{n\pi}[\cos(n\theta_1) + \cos(n\theta_2)]*\sin(n\omega t) \quad (8)$$

In order to control the fundamental load voltage and eliminate one harmonic, two equations are needed. Therefore, presented five-level inverter can provide control of the fundamental component and the ability to eliminate or control the amplitude of one harmonic. The preferred harmonic to eliminate is biggest one. Then third harmonic is selected to eliminate, (n=3).

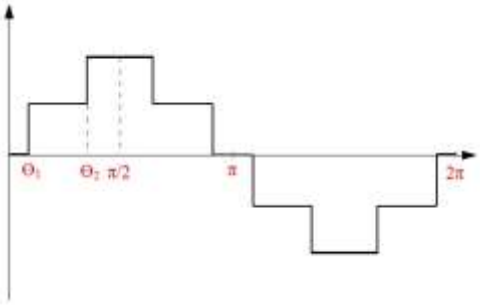


Fig. 4. Symmetric and stepped load voltage of five-level inverter.

Two switching angles can be found by solving below equations:

$$\begin{cases} \cos(\theta_1) + \cos(\theta_2) = \dfrac{V_1\pi}{4V_{dc}} \\ \cos(3\theta_1) + \cos(3\theta_2) = 0 \end{cases} \quad (9)$$

where V_1 is desired fundamental voltage.

4. PROPOSED FIVE-LEVEL DUAL QUASI-Z-SOURCE INVERTER

Fig. 5 shows the proposed inverter, which combines quasi-Z-source into the later five-level inverter. In this topology, reliability of the system is improved, significantly, because the short circuit across any arm of the inverter is allowed. Use of quasi-Z-networks causes boosting capacity of dc sources. This inverter can operate in two modes, too, shoot-through and non shoot-through states. When a shoot-through state is commanded, the related shoot-through switching devices are turned on to initiate inductive boosting of the quasi-Z-network. The related switching devices are the switches that provide short circuit for each quasi-Z-network. These switching devices are S_1 and S_2 for quasi-Z-network1 and S_1 and S_3 for quasi-Z-network2. As observed, there is no addition switching device to provide shoot-through state and it causes more usage from inverter instruments and does not impose excess cost.

Also, in this topology, the two dc voltage sources and quasi-Z-networks are independent, completely. The operation of quasi-Z-networks from view point of shoot-through state time is independent from each other, consequently. This means the boost factor of two quasi-Z-networks can be unequal and the system can operate as two independent systems. Because of represented reasons and presence of two number of dc sources, it is possible to use of this topology in hybrid renewable energy systems.

Comparing proposed dual input structure with inverter proposed in Ref. [20], it is obtained that there are five switching devices in this inverter, whereas proposed inverter of [20] with five levels in output voltage has eight switching devices. Therefore, the number of switching devices in proposed structure is reduced comparing to suggested inverter of [20].

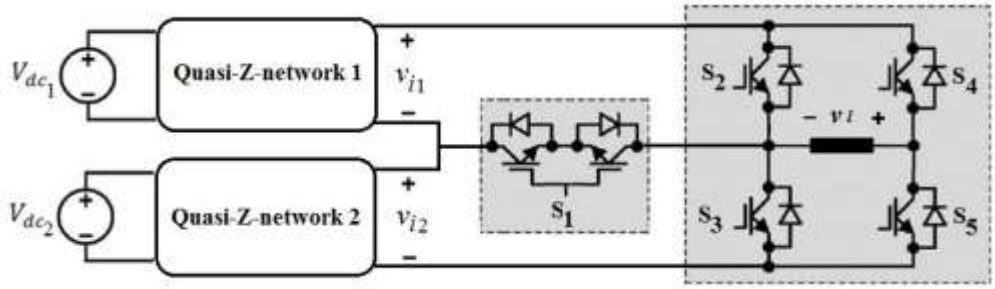


Fig. 5. Proposed five-level dual quasi-Z-source inverter.

Although, the dc voltage source numbers of two structures are equal. According to Fig. 5, the voltage levels of v_l can be summarized in Table 2.

Table 2. Switching states and load voltage of the proposed quasi-Z-source inverter.

ON switches	vl
S3, S4	+vi1+ vi2
S1, S4	+vi1
S2, S4	0
S3, S5	0
S1, S5	-vi2
S2, S5	-vi1-vi2

As observed in Table 2, the load voltage of the proposed inverter can have five levels, which it depends on the output voltages of both quasi-Z-networks, where if they are unequal the load voltage does not have symmetric levels. So, it is necessary to equalize the output voltage of quasi-Z-networks. This equalization is accomplished with control of shoot-through state time in quasi-Z-networks. It means even with unequal dc sources, it is possible to achieve symmetric five-level voltage. Then, $v_{i1}= v_{i2}= v_i$, and the voltage level of proposed inverter become as Table 3.

Table 3. Switching states and load voltage of the proposed quasi-Z-network inverter with equal output voltage of quasi-Z-networks.

ON switches	vl
S3, S4	+ 2vi
S1, S4	+vi
S2, S4	0
S3, S5	0
S1, S5	-vi
S2, S5	-2vi

When voltage boosting in each quasi-Z-network is not required, the shoot-through state is not inserted and the switching method is implemented as switching methods mentioned in section 3. But, when voltage boosting is required, the shoot-through state in each quasi-Z-network should occur in adequate time. When shoot-through state implementation of each quasi-Z-network with related switching device does not affect in load voltage, this adequate time is provided. It means that the condition of v_l=0 is adequate time for shoot-through implementation for both quasi-Z-networks, when it is possible to insert shoot-through state in two quasi-Z-network, synchronously. Also, there is other allowed time for shoot-through state of each quasi-Z-network, which it is when foreside switching devices of each network does not play role in load voltage. It is v_l=-v_i for quasi-Z-network1, and v_l=+v_i for quasi-Z-network2. This allowed shoot-through state time in two quasi-Z-networks is summarized in Table 4.

Table. 4. Allowed shoot-through state time in two quasi-Z-networks

v_l	ON switches	Allowed shoot-through state in	
		quasi-Z-network 1	quasi-Z-network 2
0	S_2, S_4 or S_3, S_5	*	*
+v_i	S_1, S_4	-	*
-v_i	S_1, S_5	*	-

4.1. PWM

The dual quasi-Z-source inverter can boost its output voltage by using two dual quasi-Z-networks and accurate designed PWM. Based on illustrated cases, the allowed time for shoot-through implementation is such Fig. 6. So, continuous allowed time (t_{ca}) for each quasi-Z-network in one cycle is:

$$t_{ca1} = \frac{[(\pi+\theta)-\pi]+[2\pi-(2\pi-\theta)]}{2\pi f} = \frac{\theta}{\pi f} \quad (10)$$

$$t_{ca2} = \frac{\theta+[\pi-(\pi-\theta)]}{2\pi f} = \frac{\theta}{\pi f} \quad (11)$$

where t_{ca1} and t_{ca2} are the continuous allowed shoot-through time for quasi-Z-network1 and quasi-Z-network2. From these relations, it can be observed that the continuous allowed times for both quasi-Z-network are equal.

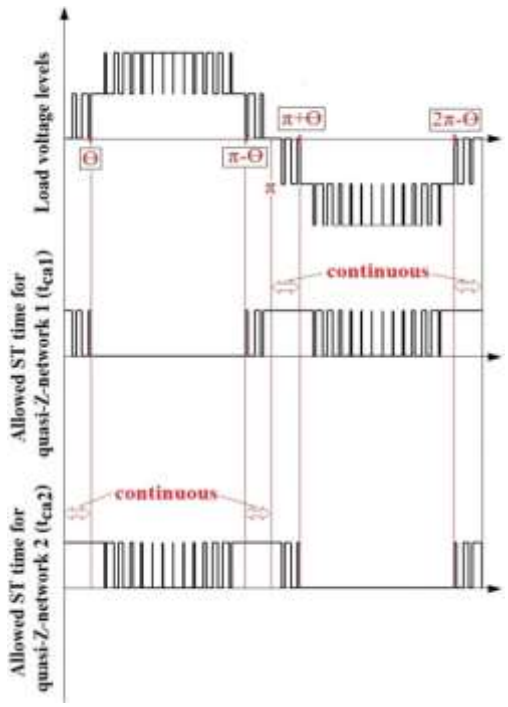


Fig. 6. Allowed time for shoot-through implementation in PWM.

Then, considering symmetric nature of PWM in this inverter, it can be result discontinuous allowed times for both quasi-Z-networks are equal, too.Based on the continuous and discontinuous allowed time for shoot-through implementation, the duty ratio of it can be divided to two sections, continuous D_1 and discontinuous D_2, where, these duties are duty cycles of shoot-through pulses for each section. Then, D_1T is shoot-through state time for the continuous section, exactly, Because of continuous nature of this section. But, D_2T is different from shoot-through state time for discontinuous section, because of quasi-pulse nature of discontinuous section. Then, it is convenient and accurate to deal the continuous section, and based on this principle, it is preferred to use this section. But, if this section cannot satisfy requirement boost, it is necessary to use the discontinuous section. Based on represented subjects, the PWM algorithm for each quasi-Z-network in proposed inverter is summarized in flowchart of Fig. 7. In Fig. 7, D_0 is initial duty cycle for the discontinuous allowed time, ΔD is increment value of duty cycle and v_i^* is reference of v_i.

4.2. SHEM

In this modulation scheme, two switching angles participate.

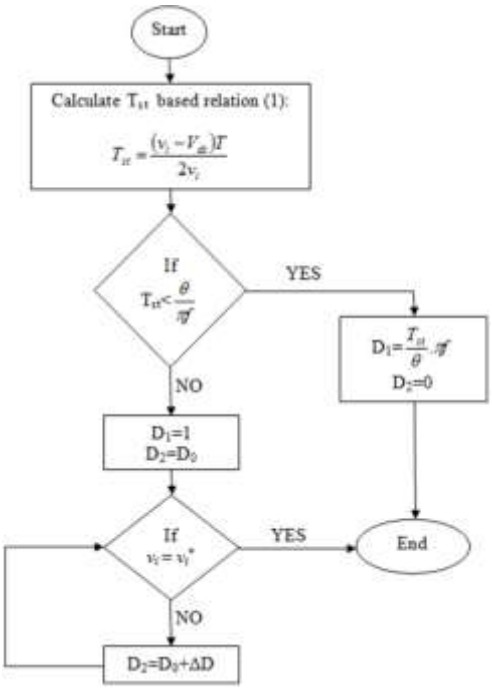


Fig. 7. PWM algorithm flowchart for each quasi-Z-network in proposed inverter.

Also, because of stepped nature of load voltage in this algorithm, the allowed time for shoot-through implementation is continuous, wholly, unlike PWM. Where, it is shown in Fig. 8. From Fig. 8, the allowed time for each quasi-Z-network in one cycle is:

$$t_{ca1}=\frac{\theta_1+\left[(\pi+\theta_2)-(\pi-\theta_1)\right]+\left[2\pi-(2\pi-\theta_2)\right]}{2\pi f}=\frac{(\theta_1+\theta_2)}{\pi f} \tag{12}$$

$$t_{ca2}=\frac{\theta_2+\left[(\pi+\theta_1)-(\pi-\theta_2)\right]+\left[2\pi-(2\pi-\theta_1)\right]}{2\pi f}=\frac{(\theta_1+\theta_2)}{\pi f} \tag{13}$$

It is observed that the allowed time for both quasi-Z-network are equal. Because of continuous nature of the allowed time in SHEM, this algorithm does not have complexity of PWM, and it is more accurate than later algorithm. The SHEM algorithm for each quasi-Z-networks is summarized in flowchart of Fig. 9. Where D is duty cycle shoot-through pulses.

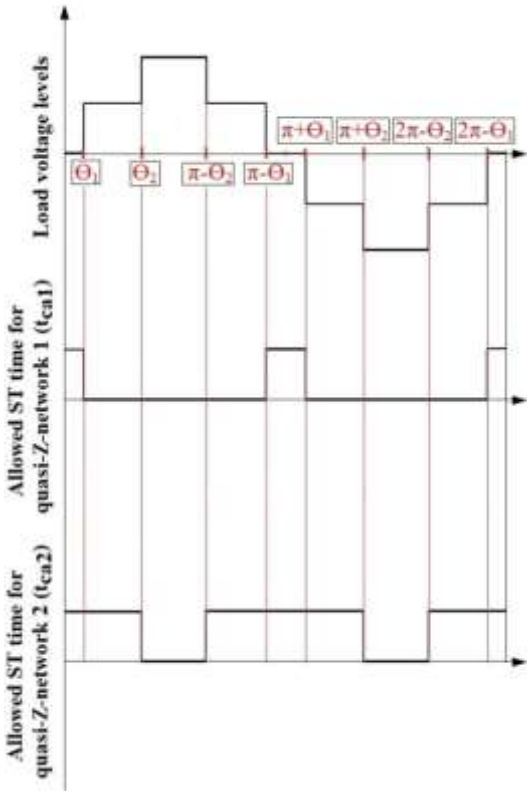


Fig. 8. Allowed time for shoot-through implementation in SHEM.

5. RESULTS

5.1. Simulation results

Simulations have been performed to prove the capabilities of proposed inverter. The system parameters are listed in Table 5. For better comparison, the modulation indices are set to 1.

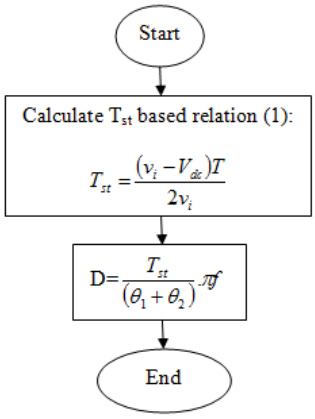


Fig. 9. SHEM algorithm flowchart for each quasi-Z-network in proposed inverter.

Table 5. System parameters

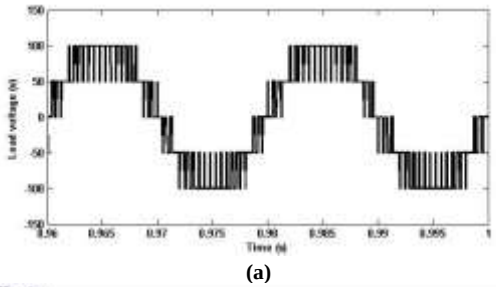
L_1=L_2	8 mH
C_1=C_2	4700 µF
Nominal frequency	50 Hz
Switching frequency	500 Hz
Load resistance	10 Ω
Load inductance	mH

5.1.1. Presented five-level inverter

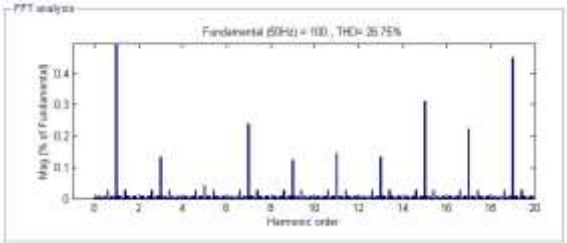
In these simulations, the dc source voltage is considered 50V, and two switching algorithms are used to switch of the inverter.

5.1.1.1. PWM

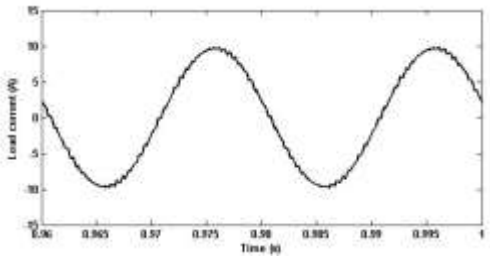
Fig. 10(a)-(b) present the load voltage of the inverter and harmonic spectrum of it. It can be observed that the load voltage has five levels, as expected, and the levels of it are 0,±50V, and ±100V. Also, load current of the inverter is displayed in Fig. 10(c).



(a)



(b)

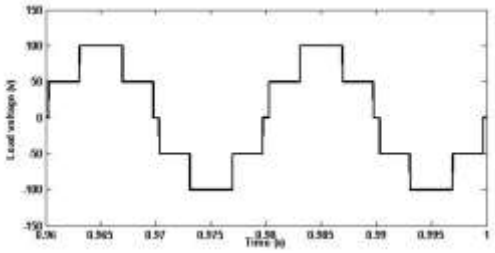


(c)

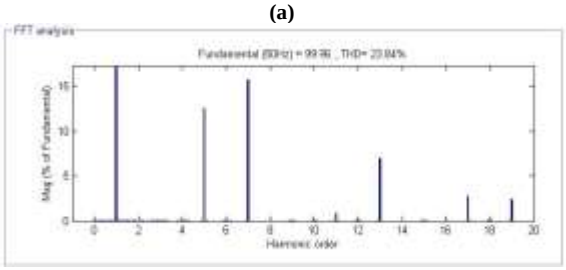
Fig. 10. Presented five-level inverter (PWM): (a) load voltage; (b) harmonic spectrum of load voltage; (c) load current.

5.1.1.2. SHEM

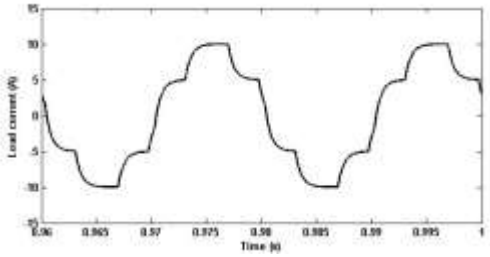
The load voltage of the five-level inverter and harmonic spectrum of it are displayed in Fig. 11(a)-(b). This inverter is switched by SHEM and as showed, it has quarter wave, symmetric, and stepped load voltage. Also, it is shown that the value of third harmonic is almost zero, which it shows the correct operation of the inverter in SHEM algorithm. Fig. 11(c) displays the load current of the inverter, when SHEM implementing.



(a)



(b)



(c)

Fig. 11. Presented five-level inverter (SHEM): (a) load voltage; (b) harmonic spectrum of load voltage; (c) load current.

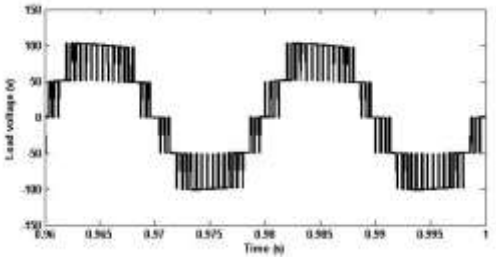
5.1.2. Proposed five-level dual quasi-Z-source inverter

In this section, the dc voltage sources are lower than 50V, and the goal of the inverter is increase of the dc level until attaint 50V in output of each quasi-Z-network. Then in this simulation, V_{dc1} and V_{dc2} are considered 40V and 34V, respectively.

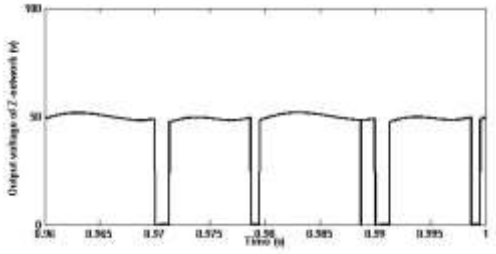
5.1.2.1. PWM

As known, V_{dc2} is 34V. Then, the boost factor is 1.47 and T_{st} is obtained equal to 0.00318s. But in this network $T_{st} > \frac{\theta}{\pi f}$.

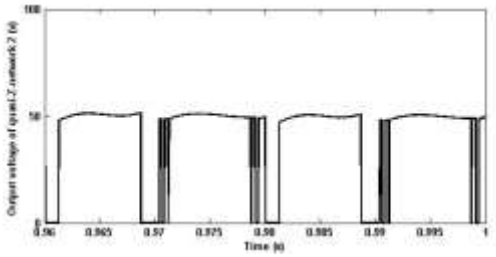
Then based on the algorithm flowchart, D_1 is set to 1 and D_2 is specified based on iteration scheme, where it is obtained equal 0.05. So, it means the continuous time for shoot-through implementation cannot satisfy requirement boost, and it is necessary to use discontinuous section in quasi-Z-network2. Fig. 12(a) presents the load voltage and Figs. 12(b) and 12(c) present the output voltage of quasi-Z-networks, v_{i1} and v_{i2}, which they are obtained about 50V. Also, harmonic spectrum of load voltage and the load current of the inverter are shown in Fig. 12(d) and 12(e), respectively. As observed, the output voltages of quasi-Z-networks have a slope due to nature of capacitor and inductor. So, it is evident that the slope of quasi-Z-networks voltages is appeared in load voltage of the inverter.



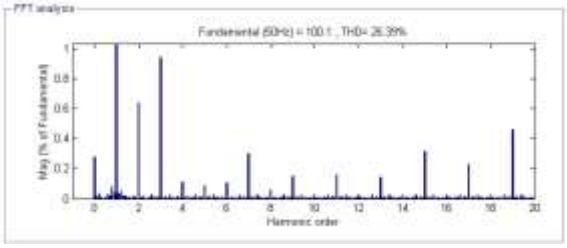
(a)



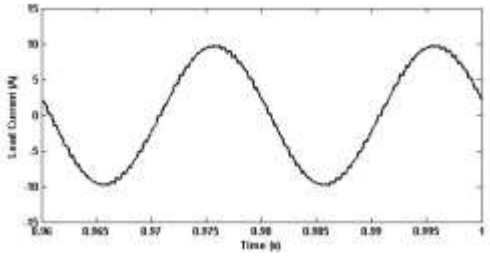
(b)



(c)



(d)



(e)

Fig. 12. Proposed five-level dual quasi-Z-source inverter (PWM): (a) load voltage; (b) output voltage of quasi-Z-network1; (c) output voltage of quasi-Z-network2; (d) harmonic spectrum of load voltage; (e) load current.

Comparing Figs. 10(d) and 12(d), it is result that this phenomenon does not affect on the harmonic spectrum and THD, significantly. It is evident from Fig. 12 that the shoot-through state of quasi-Z-network1 is inserted in two times in each cycle. It means that this quasi-Z-network uses just continuous time of allowed shoot-through, which is confirmed from above calculations. Also, the shoot-through state of quasi-Z-network2 is inserted in more times in each cycle. It is because of dealing with the discontinuous time in addition to the continuous time, based on represented calculations.

5.1.2.2. SHEM

As informed, the boost factor and T_{st} for quasi-Z-network1 are calculated as 1.25 and 0.002s, respectively. The switching angles in this modulation index are $\Theta_1=0.0278\pi$, and $\Theta_2=0.305\pi$. Based on flowchart of Fig. 9, D is obtained as D=0.3.

Besides, the boost factor and T_{st} for quasi-Z-network2 are calculated as 1.47 and 0.00318s, respectively. Then, D is obtained as D=0.48 for quasi-Z-network2.

The load voltage and output voltage of quasi-Z-network are displayed in Figs. 13(a), 13(b), and 13(c). As observed in these figures, v_{i1} and v_{i2} are obtained about 50V. This is demonstrated the correct operation of this shoot-through implementation algorithm. Fig. 13(d) shows harmonic spectrum of load voltage, where the third harmonic is almost eliminated based on the algorithm. Also, comparing Figs. 11(d) and 13(d), it is result that this phenomenon does not affect on the harmonic spectrum and THD, significantly in this switching algorithm similar to PWM. The load current waveform of this inverter is shown in Fig. 13(e).

5.1.3. Comparison

In order to compare proposed inverter with inverter of [20], both structures were simulated with similar parameters. Based on simulation results and above analyses, some comparisons between these inverters based their presented switching algorithms is summarized in Table 6. This table shows the difference of the inverters based their switching algorithms.

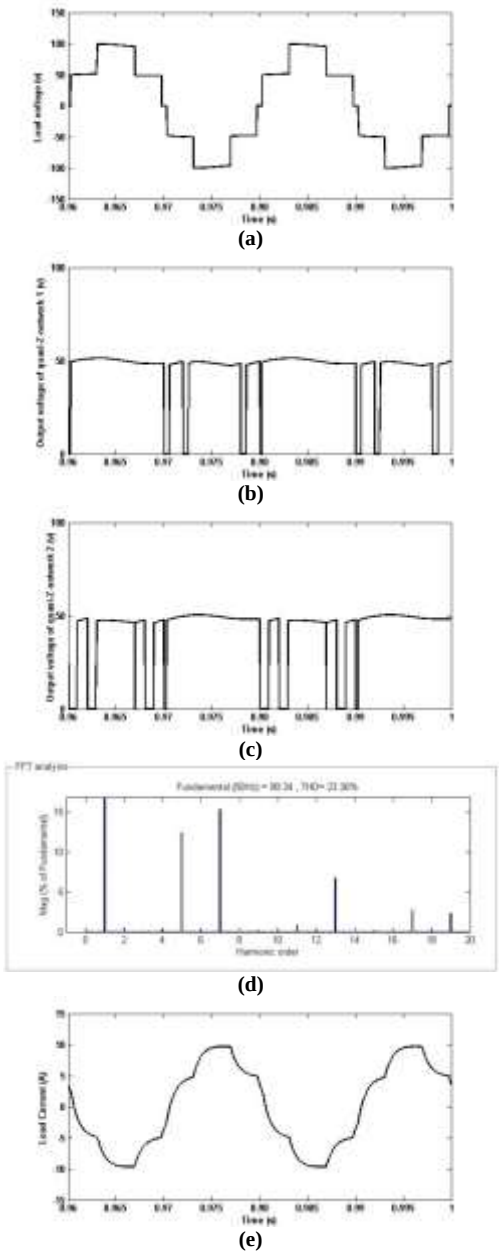


Fig. 13. Proposed five-level dual quasi-Z-source inverter (SHEM): (a) load voltage; (b) output voltage of quasi-Z-network1; (c) output voltage of quasi-Z-network2; (d) harmonic spectrum of load voltage; (e) load current.

5.2. Experimental results

A proposed five-level dual quasi-Z-source inverter was built using IRFP450 MOSFETS as the switching devices and MUR860G as fast diodes in the quasi-Z-source topologies. The dc voltage sources with amplitude 10V were used to individually supply of each quasi-Z-network. The capacitors and inductors of quasi-Z-networks are 4700 μF and 8mH, respectively. Where, they are similar to simulation parameters as Table 5. The switching signals were produced with PCI-1716 DAQ for *B*=1.25, and interfaced to the inverter power switches through driver TLP250. The load of this experimental is RL, where R=10Ω and L=8mH. Fig. 14 shows photograph of the prototype.

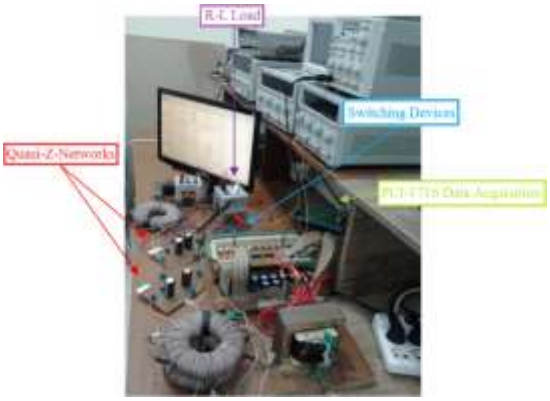


Fig. 14. Photograph of experimental prototype.

Figure 15 and 16 show the load voltage, output voltage of quasi-Z-network1, output voltage of quasi-Z-network2, and the load current which is voltage of the load resistance (10 Ω), in proposed PWM and SHEM algorithms, respectively. Based on the calculations of B=1.25 in section 5.1.2, T_{st} and duty cycles of shoot-through pulses are obtained for each switching algorithms. The related figures show such boosts in output of quasi-Z-networks.

Table 6. Comparison between proposed inverter and inverter of [20]

Inverter / Comparison	Proposed five-level dual quasi-Z-source inverter		Cascaded H-Bridge five-level trans-Z-Source Inverter [20]	
	PWM	SHEM	SVPWM	Extended SVM
Switching frequency	High	Low	High	High
Base of ST implementation algorithm	Calculation-Empirical	Calculation	Calculation	Empirical
Efficiency	83%	81%	83%	86%
TSDP	6218		6920	

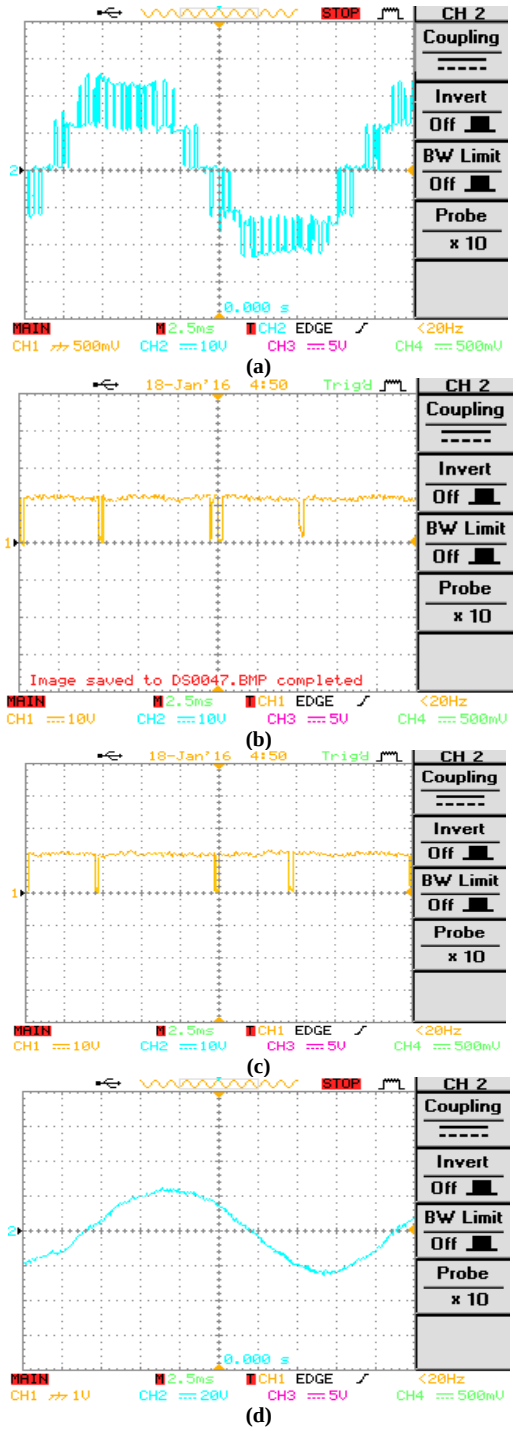


Fig. 15. Experimental results of proposed PWM algorithm: (a) load voltage; (b) output voltage of quasi-Z-network1; (c) output voltage of quasi-Z-network2; (d) load current (voltage of the load resistance).

6. CONCLUSIONS

This study proposed five-level dual quasi-Z-source inverter. This inverter can boost input dc voltage sources independently using quasi-Z-networks. Presence of two dc voltage sources in proposed structure due to two quasi-Z-networks which can be controlled independently causes possibility of use it in hybrid systems, such as PV/wind.

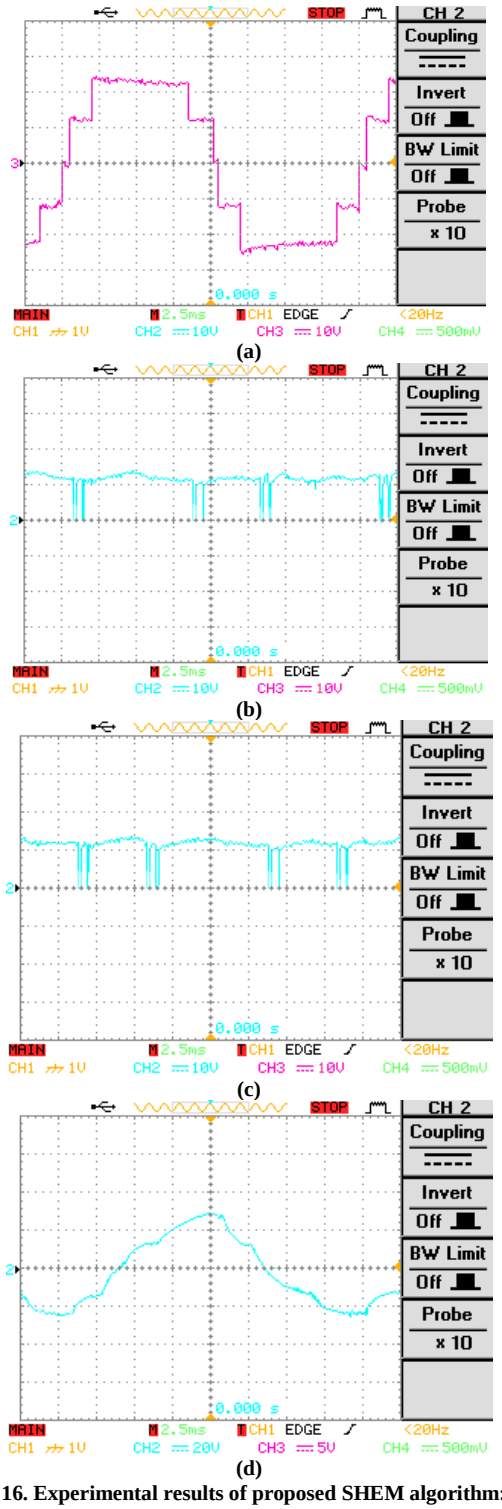


Fig. 16. Experimental results of proposed SHEM algorithm: (a) load voltage; (b) output voltage of quasi-Z-network1; (c) output voltage of quasi-Z-network2; (d) load current (voltage of the load resistance).

The represented inverter with suggested algorithms can generate a wide range of load voltage, where presence of these quasi-Z-networks does not affect in operation of switching algorithms. Comparison of two proposed switching algorithms, it is result that although PWM is convenient and simple one for modulation, but in shoot-through implementation, SHEM does not have

complexity of PWM and it is more accurate. The simulation and experimental results verified the ability of proposed inverter in voltage boosting and generation of desired output voltage waveform. Based the results, the load voltage conforms the represented calculations of suggested algorithms.

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