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A Developed Structure of Step-Up DC/DC Converter by Using Coupled Inductor and Active-Clamped Circuit

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Abstract- *In this paper, a new structure of step-up dc-dc converter by using coupled inductor and active-clamped circuit is proposed. The proposed converter generates high voltage gain in comparison with the conventional dc-dc converters. Due to using active-clamped circuit in the proposed topology, the voltage stress on main switch is reduced. In addition, the zero voltage switching (ZVS) in ON-state of main switch is obtained. In this paper, the performance of the proposed structure is investigated in continuous current mode (CCM) and discontinuous current mode (DCM). Moreover, the voltage gains in CCM and DCM operations are calculated. To prove the correctness operation and also the given equations, the simulation results in PSCAD/EMTDC software are used.*

Keyword: Coupled-inductor, Step-up converter, Active-clamped circuit, Zero voltage switching

1. INTRODUCTION

In recent years, due to quick increasing in energy consumption, the distributed generation (DG) systems such as fuel cell, photovoltaic and wind energy have been noticed [1-2]. Produced voltage through fuel cell and photovoltaic is DC and has a low magnitude. So, a step-up DC-DC converter is used as an interface device between source and inverter to transform voltage from a low level to a high level. This converter must include high voltage gain, high efficiency and small volume [3]. The conventional step-up converters produce a high voltage gain with a very large duty cycle [4-7]. Operating with high duty cycle may cause reverse recovery and electromagnetic interface problems [8]. Moreover, in practice, the voltage gain is restricted due to existence of power switch, rectifier diode and equivalent series resistor of inductors and capacitors. The voltage gain can be improved by using the dc-dc converters with capacitive or inductive switching construction [9]. Additionally, a small resonant inductor is added into the switched-capacitor circuit to solve the diode reverse recovery problem and reduced the large pulsed current across the switches when being turned ON [10-11]. Also an inactive chopper circuit with low losses which is a combination of diode and capacitor is used to cut the voltage spike in OFF-state of switch and then recover energy of the leakage inductor [3]. Moreover, several step-up inductor-based converters and converters with inactive low loss chopper circuit can be used [12-15]. In these structures, the switches operate in hard switching condition. In some of these converters, the high voltage gain is produced by regulating the conversion ratio Nevertheless, the main switch may face with short-term transient voltage (voltage spike) and the transformer leakage inductance causes high power losses. To increase the efficiency and to reach a high voltage gain, new step-up converters have been introduced in [16-17]. In these converters the switch faces high charge current and transmission losses. In DC-DC converters coupling inductor is used to get high voltage gain, but it must be noted that the leakage inductance causes a short-term transient voltage through main switch and impresses conversion ratio [13, 18, 19]. Moreover, voltage multiplier cell could be used to increase the voltage gain [15]. Also, the voltage gain can be increased by utilizing several coupling inductors [20-22]. In [23] a high step-up dc-dc converter has been presented. In the proposed structure in order to have a high voltage gain a diode and a capacitor has been used in the input. In the proposed structure a passive clamp circuit has been used to provide zero voltage switching (ZVS) condition.

In this paper, a new structure for active clamp coupled-inductor-based converter is proposed. The Proposed structure has a high voltage gain and low ripple of input current. At the following, first the operation of the proposed converter in different operating modes in continuous current mode (CCM) and discontinuous current mode (DCM) is given. Then, the voltage gain of the converter is calculated.

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Finally, the correctness operation of the proposed converter is reconfirmed by the simulation results in PSCAD/EMTDC software.

2. PROPOSED CONVERTER

Figure 1 shows the configuration of proposed converter including input DC voltage source (V_i), main switch (S), clamp circuit which is consisted of an auxiliary switch (S_c) and a capacitor (C_c), coupling inductors N_S and N_p, capacitors C_2 and C_3, diodes D_2 and D_3, output diode (D_o) and output capacitor (C_o). The coupling inductor is used as a transformer in converter. Equivalent circuit of coupling inductors contains magnetizing inductor L_m, leakage inductor L_K and an ideal transformer. Parasitic capacitor is used to Zero Voltage Switching (ZVS). The Energy of the leakage inductance of the coupling inductor is returned to the capacitor C_o and then, the voltage stress decreases through the switch (S), so, a switch with low ON-state resistor ($R_{DS,on}$) could be used.

The converter operates in a way that when the main switch is in ON-state the magnetizing inductance L_m is charged by V_i. So, the magnetizing current increases linearly and at the same time the energy is transferred to the switched-capacitors C_2 and C_3 through the coupling inductors. When the switch is off the stored energy in the magnetizing inductor L_m is released through the secondary side of coupling inductor to charge the capacitors C_2 and C_3 in parallel state. The current of secondary winding is limited by leakage inductance.

The following assumptions are considered to simplify the analysis of the proposed converter:

1) The capacitors C_2, C_3 and C_o have enough large magnitude. As a result, the voltages V_{c2}, V_{c3} and V_o is considered constant.
2) The switches are considered but the parasitic capacitor of switch is considered.
3) The conversion ratio of the coupling inductor is assumed as follows:

$$n = \frac{N_s}{N_p} \tag{1}$$

At the following subsections, the operation of the proposed converter is considered in CCM and DCM.

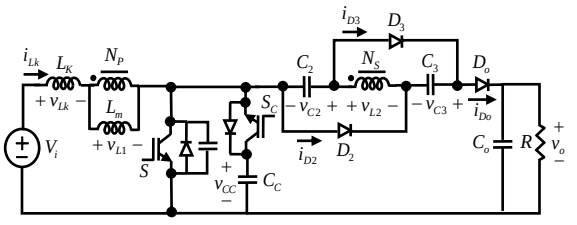


Fig. 1. Proposed dc/dc converter.

2.1. Operation in CCM

In CCM operation, there are eight operating modes at every switching period. Fig. 2 shows the typical waveforms of converter in CCM operation and Fig. 3 shows the equivalent circuit of converter in different operating modes in CCM operation.

A. Subinterval ($t_0 - t_1$)

In this operating mode, the main switch S is in ON-state and the clamp switch S_c and output diode D_o are in OFF-state. The magnetizing inductor and leakage inductors are going to be charged through the input voltage source. So, the magnetic current increases linearly. The voltage equation of leakage and magnetizing inductors in the primary side is as $V_i = V_{Lk} + V_{Lm}$. The Secondary side current (i_s) increases with respect to the leakage inductor and energy is transferred to capacitors C_2 and C_3 through the coupling inductor at the same time. The output capacitor C_o is discharged by the load R. Therefore, the currents I_{Lm} and I_{LK} are obtained as follows:

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_i - V_{L1}}{L_m}(t - t_0) \tag{2}$$

$$i_{Lk}(t) \approx i_{LK}(t_0) + \frac{V_i - \frac{V_{c2}}{n}}{L_{LK}}(t - t_0) \tag{3}$$

B. Subinterval ($t_1 - t_2$)

The main switch (S) turns OFF at moment t_1, then the capacitor C_s begins to resonant with leakage inductance L_K. Since C_s is small and L_K is relatively large, the voltage V_{ds} on main switch S rises almost at a constant of zero. Turn-off losses of main switch are reduced due to the existence of C_s.

$$V_{ds} \approx \frac{i_{Lk}(t_1)}{C_s}(t - t_1) \tag{4}$$

C. Subinterval ($t_2 - t_3$)

According to Fig. 2 at t_2, the switching voltage of main switch reaches the clamp capacitor voltage, and the antiparallel of clamp switch S_c is forced to conduct. Then, V_{ds} is clamped to V_{Cc} by the antiparallel diode of clamp switch S_c.

Since clamp capacitor C_c is much large than C_s, so C_s can be neglected and almost all the current flow through the C_c. After t_2, the leakage inductance L_k is discharged by the voltage of $[V_i - (V_{c2}/n)] - V_{Cc}$ that is shown in Fig. 2. In comparison with $-V_{Cc}$, the voltage of $V_i - (V_{c2}/n)$

is much smaller and it can be neglected to simplify the expression. In this short subinterval, the current through L_{Lk} decreases almost linearly, as well as the current through secondary winding.

Considering the above-mentioned discussion, the followed equations can be written:

$$i_{Lk}(t) = i_{LK}(t_2) + \frac{V_i - \frac{V_{c2}}{n} - V_{Cc}}{L_K}(t - t_2) \quad (5)$$

$$i_{Lk}(t) \approx i_{Lk}(t_2) - \frac{V_{Cc}}{L_K}(t - t_2) \quad (6)$$

According to Fig. 2, in the third operating mode ($t_2 < t < t_3$), the waveform of the current through the leakage inductor has a steep slope which can cause a voltage spike across the inductor in a short time interval. However, in this operating mode, despite the steep slope of the current waveform, the absolute value of the current difference is low, which limits the voltage across the inductor. In addition, according to Eq. (6), the voltage across the leakage inductor is limited to V_{Cc}, which is a constant value and it can not be considered as a spike.

D. Subinterval ($t_3 - t_4$)

At moment t_3 the voltage across the output diode D_o falls to zero, then the stored energy is transferred to the load.

L_m is discharged and during this time interval the leakage inductance L_K is begins to resonate with capacitor C_c and capacitors C_2 and C_3. In this time interval, the resonance is relatively large and the leakage inductance current decreases linearly. For the operating mode, the following equations can be written:

$$i_{Lm}(t) = i_{Lm}(t_3) + \frac{V_o - V_{Cc} - V_{C3} - V_{C2}}{nL_m}(t - t_3) \quad (7)$$

$$i_{LK}(t) \approx i_{LK}(t_3) + \frac{V_i - V_{Cc} - \left(\frac{V_o - V_{c3} - V_{c2}}{n}\right)}{L_K}(t - t_3) \quad (8)$$

E. Subinterval ($t_4 - t_5$)

Turn-On signal is applied to clamp switch S_c at t_4. S_c is turned on when its body diode is conducting thus the ZVS turn-on condition is achieved. The Equivalent circuit in this subinterval is similar to that of subinterval ($t_3 - t_4$).

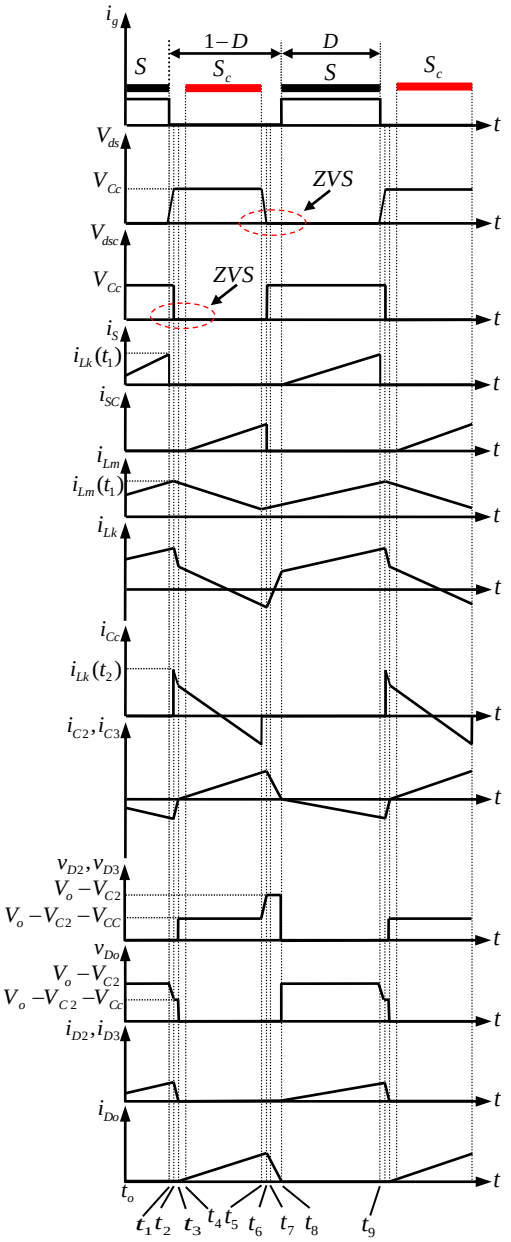
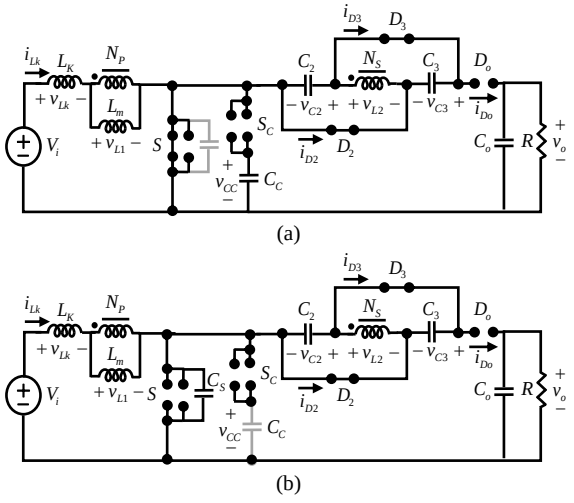


Fig. 2. Typical waveforms of the proposed converter in CCM operation.



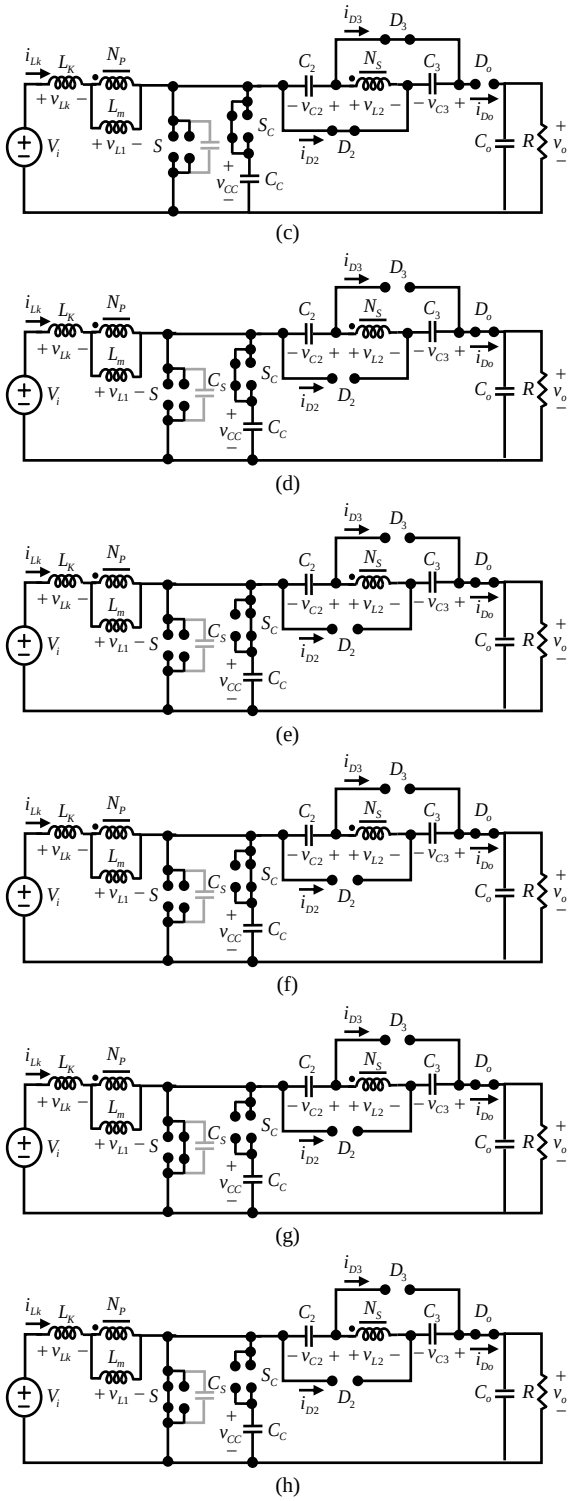


Fig. 3. The equivalent circuit of the proposed converter in different operating modes in CCM operation, (a) subinterval (t_0-t_1), (b) subinterval (t_1-t_2), (c)subinterval (t_2-t_3), (d) subinterval (t_3-t_4), (e) subinterval (t_4-t_5), (f) subinterval (t_5-t_6), (g) subinterval (t_6-t_7), (h) subinterval (t_7-t_8).

F. Subinterval (t_5-t_6)

The clamp switch S_c is turned OFF at t_6. After that, the leakage inductance, and capacitors C_c, C_2 and C_3 stop resonating and a new resonance is formed by leakage inductance and capacitor C_s. According to Fig. 2 because C_c is small and L_k is relatively large, the voltage on the main switch (V_{ds}) decreases almost at a constant slope while the voltage across clamp switch S_c increases from zero at the same rate. Thus, the turn-OFF losses of the main switch are reduced due to the existence of C_s. For this operating mode, the following equation is valid:

$$V_{ds} \approx V_{Cc} + \frac{i_{LK}(t_5)}{C_s}(t-t_5) \tag{9}$$

G. Subinterval (t_6-t_7)

The voltage of capacitor C_s falls to zero at t_6, and then the antiparallel diode of main switch S begins to conduct. C_s and L_K stop resonating. The increasing rate of the current through L_K is controlled by the output voltage. For this operating mode, the following equation can be obtained:

$$\begin{aligned} i_{LK}(t) &= \frac{V_o - V_{c3} - V_{c2} - V_i}{nL_{LK}}(t-t_6) \\ &\approx \frac{V_o}{nL_K}(t-t_6) \end{aligned} \tag{10}$$

H. Subinterval (t_7-t_8)

The turn-on signal is applied to main switch (S) when its antiparallel diode is in the ON-state. The main switch turns on with ZVS. The equivalent circuit in this operating mode is similar to that of subinterval (t_6-t_7). At t_8, the voltages of diode D_2 and D_3 drop to zero. After that L_m is charged by the input voltage and the energy is transferred to C_2 and C_3 by the coupled inductor again.

2.2. Operation in DCM

To simplify the analysis of DCM operation, the leakage inductor (L_K) of the coupled inductor is neglected and it is assumed that there is no clamped circuit in converter's circuit.

Figure 4 shows the typical waveforms when the proposed converter operates in DCM, and Fig. 5 shows the equivalent circuit of the converter in different operating modes.

A. Subinterval (t_0-t_1)

During this time interval, S is turned on. The equivalent circuit of converter is shown in Fig. 5(a). The inductor L_m stores the energy from input source. Thus, its current increases linearly. Also, the energy of input source is transferred to the secondary side of the coupled inductor, which is connected to capacitors C_2 and C_3 in parallel to provide their energies. During this time interval, the output capacitor (C_o) provides the energy of load

lonely. This operating mode ends when switch (S) is turned off at $t = t_1$.

B. Subinterval $(t_1 - t_2)$

During this time interval, S is turned off. The equivalent is shown in Fig. 5(b). The secondary side of the coupled inductor is connected to capacitors C_2 and C_3 in series. The energy of inductor L_m is transferred to load and output capacitor by the secondary side of the coupled inductor. Also both the capacitors C_2 and C_3 is connected in series with the secondary side of the coupled inductor to provide the energy of load and capacitor C_o. This operating mode ends when the energy stored in L_m is depleted at $t = t_2$.

C. Subinterval $(t_2 - t_3)$

During this time interval, S remains turned off. The equivalent circuit is shown in Fig. 5(c). Since the energy stored in L_m is depleted, the energy stored in C_o is discharged to load R. This mode ends when S is turned on at $t = t_3$.

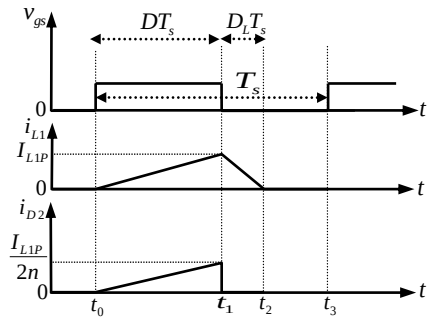
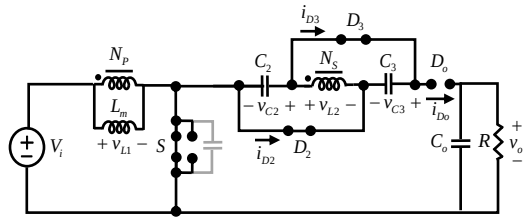
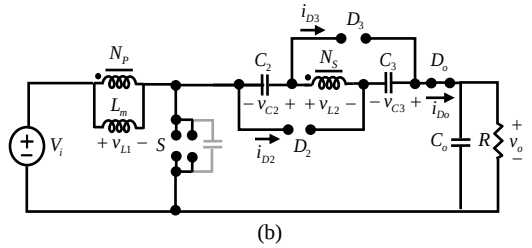


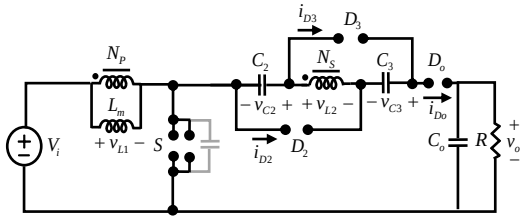
Fig. 4. Typical waveforms of the proposed converter at DCM operation.



(a)



(b)



(c)

Fig. 5. Equivalent circuit of proposed converter for different types of operation mode, (a) subinterval1 $(t_0 - t_1)$ **, (b) subinterval2** $(t_1 - t_2)$ **, (c) subinterval3** $(t_2 - t_3)$.

3. VOLTAGE GAIN CALCULATION

3.1. CCM operation

In Figure 2 at subinterval ($t_1 - t_4$) and ($t_5 - t_8$), the operation is very quick. So, these operating modes can be neglected in voltage gain calculations. The ideal current of leakage inductor is considered linear and constant and the resonance is relatively large at switching period. There are two kinds of separate operation at total switching period. The main switch is off at subinterval ($t_1 - t_5$) and clamp switch is on. The current of D_o, D_2 and D_3 diodes are equal to output current (I_o). The current peak of output diode is:

$$I_{Do-peak} = \frac{2I_o}{1-D} \tag{11}$$

For fifth operating mode the following equations can be written:

$$V_{LK-t_{1-5}} = L_K \frac{nI_{Do-peak} f_s}{1-D} \tag{12}$$

$$V_{LK-t_{1-5}} = \frac{2nL_K I_o f_s}{(1-D)^2} \tag{13}$$

$$V_o = V_{Cc} + V_{c2} + V_{c3} + V_{L2}^{t_{1-5}} \tag{14}$$

$$V_{L2}^{V} = nV_{Lm-discharge} \tag{15}$$

$$V_{L1-discharge}^{t_{1-5}} = V_{Cc} - V_i - V_{LK-t_{1-5}} \tag{16}$$

By applying voltage balance law for inductor L_m we have:

$$\int_0^{T_{on}} V_i dt + \int_{T_{on}}^{T_{off}} (V_i - V_{Cc}) dt = 0 \tag{17}$$

From above equation, the following equation is obtained:

$$DT_s V_i + (1-D)(V_i - V_{Cc}) T_S = 0 \tag{18}$$

Where D denotes duty cycle.

Simplifying Eq. (18):

$$V_{Cc} = \frac{1}{1-D} V_i \tag{19}$$

The main switch is in ON-state at subinterval ($t_5 - t_9$) and clamp switch is in off-state. The current peak of diodes D_1 and D_2, The voltages of leakage inductor and capacitors are achieved as below:

$$I_{D2-peak} = \frac{2I_o}{D} \quad (20)$$

$$V_{LK-t_{5-9}} = L_K \frac{nI_{D2-peak} f_s}{D} \quad (21)$$

$$V_{LK-t_{5-9}} = \frac{2nL_K I_o f_s}{D^2} \quad (22)$$

$$V_{C3-t_{5-9}} = n\left(V_i - V_{LK-t_{5-9}}\right) \quad (23)$$

$$V_{C2-t_{5-9}} = n\left(V_i - V_{LK-t_{5-9}}\right) \quad (24)$$

By substituting Eqs. (17), (19), (23) and (24) into Eq. (15), the voltage gain is obtained as below by considering leakage inductor:

$$V_o = \frac{1}{1-D}V_i + n\left(V_i - \frac{2nL_K f_s I_o}{D^2}\right) + n\left(V_i - \frac{2nL_K f_s I_o}{D^2}\right) + n\left(\frac{1}{1-D}V_i - V_i - \frac{2nL_K f_s I_o}{(1-D)^2}\right) \quad (25)$$

The output current is:

$$I_o = \frac{V_o}{R} \quad (26)$$

The following equation is refined:

$$k_m = \frac{L_{LK} f_s}{R} \quad (27)$$

where f_s is frequency.

By substituting Eq. (27) in Eq. (25) the voltage gain is obtained as below:

$$M_{CCM} = \frac{V_o}{V_i} = \frac{1+n(2-D)}{1-D}\left[\frac{1}{1+\frac{4n^2K_m}{D^2}+\frac{2n^2K_m}{(1-D)^2}}\right] \quad (28)$$

Assuming $k_m = 0$ the voltage gain will be:

$$M_{CCM} = \frac{V_o}{V_i} = \frac{1+2n-nD}{1-D} \quad (29)$$

Considering Eq. (29) the duty cycle is obtained as follows:

$$D = \frac{V_o - (1+2n)V_i}{V_o - nV_i} \quad (30)$$

Substituting Eq. (30) in Eq. (19) yields:

$$V_{Cc} = \frac{V_o - nV_i}{1+n} \quad (31)$$

If conversion ratio of the coupling inductor is considered zero, so the voltage gain will be same with the conventional boost converter. The voltage gain increases by increasing conversion ratio of coupling inductor and decreases when coupling inductance increases. Assuming $k_m = 1$, voltage gain is:

$$M_{CCM} = \frac{V_o}{V_i} = \frac{1+n(2-D)}{1-D}\left[\frac{1}{1+\frac{4n^2}{D^2}+\frac{2n^2}{(1-D)^2}}\right] \quad (32)$$

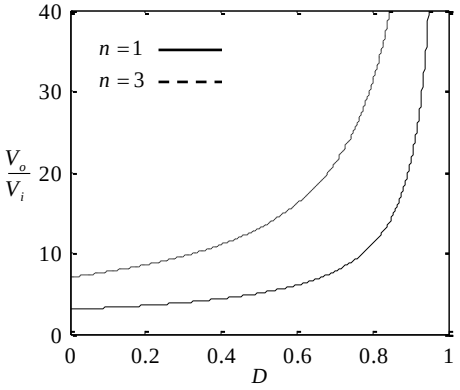


Fig. 6. Variations of voltage gain versus duty cycle under CCM operation with $n=1$, $n=3$ and $k_m=0$.

The variations of voltage gain (V_o / V_i) versus duty cycle (D) for different values of conversion ratio is illustrated in Fig. 6. As shown in this figure by increasing the conversion ratio, the voltage gain increase.

3.2. DCM Operation

For DCM operation, the following equations are valid for subinterval (t_0-t_1):

$$v_{L1} = V_{in} \quad (33)$$

$$v_{L2} = nV_{in} \quad (34)$$

$$V_{C2} = V_{C3} = -v_{L2} \quad (35)$$

$$V_{C2} = V_{C3} = -nV_{in} \quad (36)$$

The peak value of the magnetizing-inductor current is calculated as:

$$I_{LmP} = \frac{V_i}{L_m} DT_s \quad (37)$$

In interval $[t_1 - t_2]$, the following equation can be expressed based on Fig. 5(b):

$$v_{L1} = \frac{V_i - V_o + V_{C2} + V_{C3}}{1-n} \quad (38)$$

Substituting (36) into (38):

$$v_{L1} = \frac{(1-2n)V_i - V_o}{1-n} \quad (39)$$

In time interval $(t_2 - t_3)$, the following equation can be derived from Fig. 5(c):

$$v_{L1} = v_{L2} = 0 \quad (40)$$

By applying the voltage-second balance principle to the coupled inductor, the following equation is obtained:

$$\frac{1}{T}\int_{0}^{DT_S} v_{L1}\,dt+\int_{DT_S}^{(D+D_L)T_S} v_{L1}\,dt+\int_{(D+D_L)T_S}^{T_S} v_{L1}\,dt=0 \qquad (41)$$

Substituting Eqs. (33), (38), and (40) into Eq. (41), the voltage gain is calculated as follows:

$$V_o=\frac{[1-(2-D)n-D_L(1-2n)]}{1-D-D_L}V_i \qquad (42)$$

According to Eq. (42), the duty cycle D_L as defined in Fig. 4 can be derived as below:

$$D_L=\frac{V_i[1-(2-D)n]-(1-D)V_o}{(1-2n)V_i-V_o} \qquad (43)$$

From Fig. 5, the energy stored on capacitor C_2 is fully released to capacitor C_o. Also, the average current I_{Do} is equal to I_{D2}. Thus, the average current of I_{Co} is computed as:

$$I_{Co}=I_{Do}-I_o=I_{D2}-I_o=\frac{1}{2}DT_s\frac{I_{LmP}}{2n} \qquad (44)$$

Because I_{Co} is equal to zero under the steady state, substituting Eqs. (37) and (26) into Eq. (44), the voltage gain in DCM is given by

$$M_{DCM}=\frac{V_o}{V_i}=\frac{D^2T_s^2R}{4nL_1} \qquad (45)$$

4. VOLTAGE STRESS CALCULATION

According to the description of operating modes, the voltage stress on active switch S and diodes D_2, D_3 and D_o is given as:

$$V_{ds}=\frac{1}{1-D}V_i=\frac{V_o-nV_i}{1+n} \qquad (46)$$

$$V_{D2}=V_{D3}=\frac{nV_i}{1-D}=\frac{n(V_o-nV_{i)}}{1+n} \qquad (47)$$

$$V_{Do}=\frac{(1+n)V_i}{1-D}=\frac{V_o-nV_i}{1+n} \qquad (48)$$

Equations (46) - (48) mean that, under the same voltage ratio, the voltage stresses can be adjusted by the turn ratio of the coupled inductor.

5. PERFORMANCE COMPARISON

In this section, to show the performance of the proposed topology, the proposed converter is compared with the presented converters in [24-26] from different point of view. Table 1 summarize the results of this comparison.

The variations of voltage gain versus duty cycle for the proposed converter and converters in [24-26], for $n=2$ have been illustrated in Fig. 7. According to Fig. 7 it can be noticed that for a specific duty cycle the voltage gain of the proposed converter is higher than the ones presented in [24-26].

As it can be seen for duty cycles less than 0.8 the differences between the voltage gains of the proposed converter and the presented ones in [24-26] are higher than the cases in which the duty cycle is larger than 0.8.

Table 1. Comparison between the proposed converter with the presented converters in [24-26]

Topology	[24]	[25]	[26]	The Proposed Converter
Active Switch	2	1	1	2
Diodes	2	4	2	3
Voltage gain	$\frac{1+n}{1-D}$	$\frac{n}{1-D}$	$\frac{2+n-D}{1-D}$	$\frac{1+2n-nD}{1-D}$
Voltage stress of active switch	$\frac{V_o}{n+1}$	$\frac{V_o}{n}$	$\frac{V_o}{2+n-D}$	$\frac{V_o}{1+2n-nD}$
Voltage stress of output diodes	V_o	V_o	$\frac{V_o(1+2nD)}{(2+n-D)}$	$\frac{V_o(1+n)}{(1+2n-nD)}$

For example, for $D=0.4$ the voltage gain of the proposed converter is 7 and the voltage gains of the presented converters in [24-26] are 5, 3.33, and 6, respectively. As it is obvious the voltage gain of the proposed converter is higher than the others.

Since the proposed converter is a high voltage converter, thus the higher voltage gain can be considered as a privilege in comparison to the other converters presented in [24-26].

The variations of the normalized voltage of a switch versus the voltage gain has been shown in Fig. 8. According to Fig. 8, it can be seen that for any duty cycle the voltage stress of the main switch of the proposed converter is lower than the voltage stresses of the main switches of the presented converters in [24-26]. According to Fig. 8, the voltage stresses of the switches in [24] and [25] are independent of the voltage gain. In each one the converters the voltage stress is a function of the conversion ratio.

For instance, for $n=2$ the voltage stresses in [24] and [25] are 0.5 and 0.33, respectively. In [26] the voltage stress of a switch is related to the voltage gain of the converter. In other words, by increasing the voltage gain of the converter the voltage stress of a switch also rises. The voltage stress of the main switch of the proposed converter is similarly dependent on the voltage gain. The variations of the voltage stress of the main switch in the proposed converter is like the one in [26]. However, for a same duty cycle the voltage stress of the main switch in the proposed converter is lower than the one in [26].

In addition to this advantage, according to Fig. 7, the duty cycle of the proposed converter for a same voltage gain is lower in comparison to the one in [26]. The lower duty cycle results in a lower conduction loss.

The comparison of the output diode voltage stresses between the proposed converter and the converters in [24] and [26] is shown in Fig. 9. In the proposed converter and the converter in [26] the voltage stress of the output diode is determined by the duty cycle and the turns ratio of the coupled inductor. For the proposed converter the voltage stress of the output diode is lower than output voltage. In the converter in [24] and [25] this parameter is equal with output voltage. For the converter in [26] the voltage stress of the output diode for low duty cycle is lower than the proposed converter and the converter in [24] and [25].

6. SOFT SWITCHING CONDITION

The turn-off losses of both the main and clamp switches are reduced due to the parallel capacitor. The ZVS turn-on condition of the clamp switch can be realized by applying the turn-off signal to the clamp switch when its antiparallel diode is in the ON state. In order to provide ZVS condition for the main switch at turn-on instance, the anti-parallel diode of the main switch must be conducting before. Thus, the voltage across the main switch would be zero and it can be turned on under ZVS condition. According to Fig. 1 it can be seen that the voltage across D_S is the reverse of the voltage across C_S, which prevents D_S from turning on. In order for D_S to turn on, the voltage across C_S must be zero before the beginning of the operational mode. In this operational mode. C_S resonates with L_{Lk}, In order for the C_S to be discharged faster than L_{Lk} the energy stored in C_S must be less than the energy stored in L_{Lk}. The energy stored in C_S is as follows:

$$W_{Cs} = \frac{1}{2} C_S V_{Cs}^{\,2} \tag{49}$$

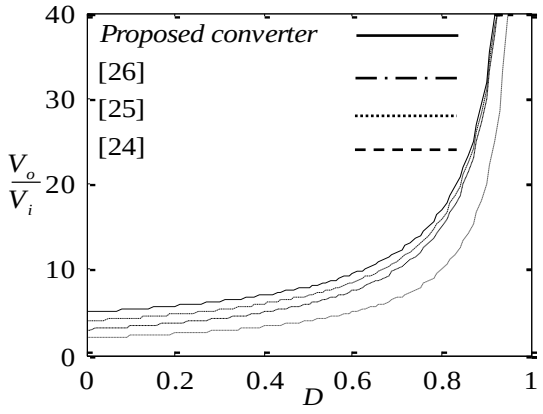


Fig. 7. Variations of voltage gain versus duty cycle for proposed converter and converters in [24], [25] and [26] at CCM operation for $n = 2$.

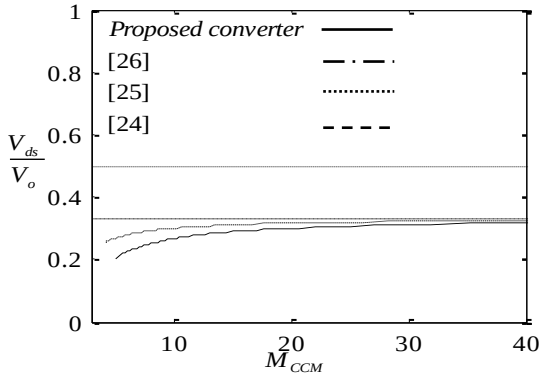


Fig. 8. Normalized switch voltage stress versus voltage gain.

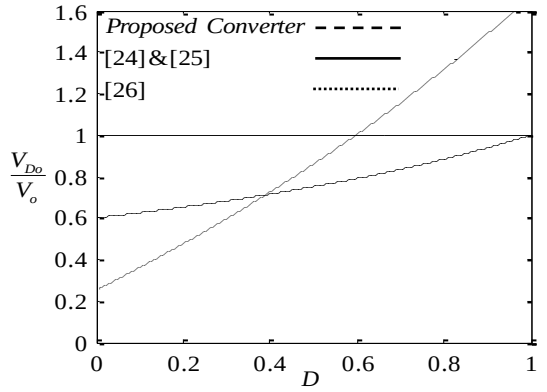


Fig. 9. Normalized output diode voltage stress versus voltage gain.

7. SOFT SWITCHING CONDITION

The turn-off losses of both the main and clamp switches are reduced due to the parallel capacitor. The ZVS turn-on condition of the clamp switch can be realized by applying the turn-off signal to the clamp switch when its antiparallel diode is in the ON state. In order to provide ZVS condition for the main switch at turn-on instance, the anti-parallel diode of the main switch must be conducting before. Thus, the voltage across the main switch would be zero and it can be turned on under ZVS condition. According to Fig. 1 it can be seen that the voltage across D_S is the reverse of the voltage across C_S, which prevents D_S from turning on. In order for D_S to turn on, the voltage across C_S must be zero before the beginning of the operational mode. In this operational mode. C_S resonates with L_{Lk}, In order for the C_S to be discharged faster than L_{Lk} the energy stored in C_S must be less than the energy stored in L_{Lk}. The energy stored in C_S is as follows:

$$W_{Cs} = \frac{1}{2} C_S V_{Cs}^{\,2} \tag{49}$$

where V_{Cs} is the average voltage across C_S.

According to Fig.1 the voltage across C_S is:

$$v_{Cs} = V_i - v_{L1} - v_{Lk} \tag{50}$$

By calculating the average values of each parameter in equation (6) and according to the zero value of the average voltage across an inductor during one switching period, the average value of the voltage across C_S will be as follows:

$$V_{Cs} = V_i \quad (51)$$

By applying (51) in (49):

$$W_{Cs} = \frac{1}{2} C_S V_i^2 \quad (52)$$

The energy stored in L_{Lk} is:

$$W_{Lk} = \frac{1}{2} L_K I_{Lk}^{\ 2} \quad (53)$$

where I_{Lk} is the average value of the current through L_{Lk}.

According to the equivalent circuit of the converter and the current balance through a capacitor, the average value of the current through L_{Lk} is:

$$I_{Lk} = (n-1) I_o \quad (54)$$

By applying Eq. (54) in Eq. (53), the following equation can be rewritten:

$$W_{Lk} = \frac{1}{2} L_K (n-1)^2 I_o^{\ 2} \quad (55)$$

Anti-parallel diode D_S would be forward biased if the following condition met:

$$W_{Lk} \geq W_{Cs} \quad (56)$$

By applying W_{Lk} and W_{Cs} from Eqs. (52) and (55), respectively, in Eq. (56) it can be concluded that:

$$L_K (n-1)^2 I_o^{\ 2} \geq C_S V_i^2 \quad (57)$$

8. SIMULATION RESULTS

To prove the correctness operation of the proposed converter, the simulation results in CCM operation by using PSCAD/EMTDC software are used. In simulation, the input dc voltage and the maximum output rated power are considered 25V and 500W. For high confidence and to produce desired DC voltage, the output capacitance is considered 200 µf. The other parameters of the converter are presented in Table 2. The converter output voltage is 373V with respect to Eq. (32). The waveforms of voltage and current of different components of the proposed converter are shown in Figs. 10, 11 and 12. The Main switch voltage V_{ds}, clamp capacitor voltage V_{Cc} and clamp capacitor current I_{Cc} are shown in Fig. 10. As shown in this figure the main voltage switch is equal the clamp capacitor voltage when the main switch is off. So, voltage spike on the main switch is eliminated As a result, the voltage stress on the main switch decreases and a switch with low ON-state resistance could be chosen.

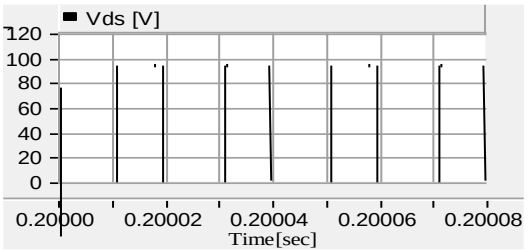
Converter desired output voltage is 373V with respect to Eq. (32) and the simulation results reconfigures this issue as shown in Fig.10 (a).

The waveform of the voltage across S and the currents through S and S_c are presented in Fig. 12. According to Fig. 12, the validity of the theoretical analyses are confirmed by the simulation results.

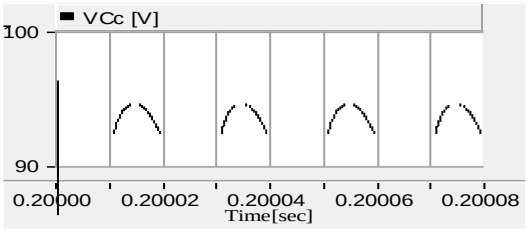
Figure 13 illustrates the proposed converter efficiency curve, which shows that the maximum efficiency is 97.8% at a light-load (50W) operation, and the full load efficiency is about 90.2%.

Table 2. Used parameters in simulation.

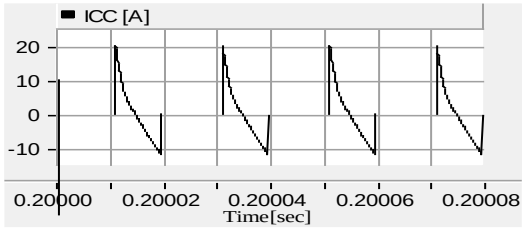
Sign	Parameter	Value
f_s	Switching frequency	$50kHz$
C_2	Capacitor with 200V	$22\mu F$
C_3	Capacitor with 200V	$22\mu F$
C_o	Output capacitor with 450V	$180\mu F$
L_m	Magnetizing inductance	$48\mu F$
L_K	Leakage inductance	$0.25\mu F$
N_p / N_s	Conversion ratio of coupling inductor	1:4
D	Duty Cycle	54.5%



(a)

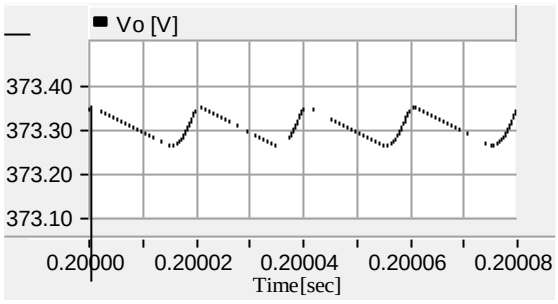


(b)

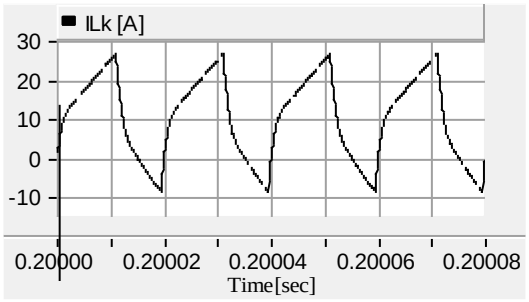


(c)

Fig. 10. Operation of clamp circuit, (a) Main switch voltage gain (V_{ds}), (b) clamp capacitor voltage (V_{cc}), (c) clamp capacitor current (I_{cc}).



(a)



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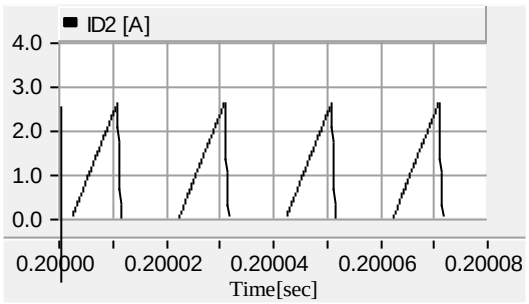

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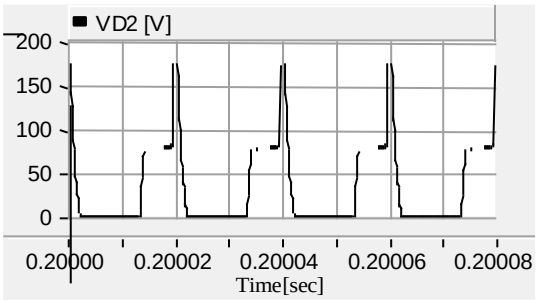
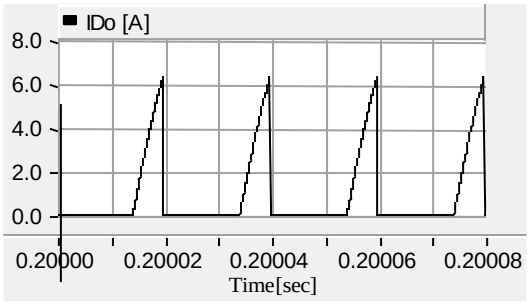
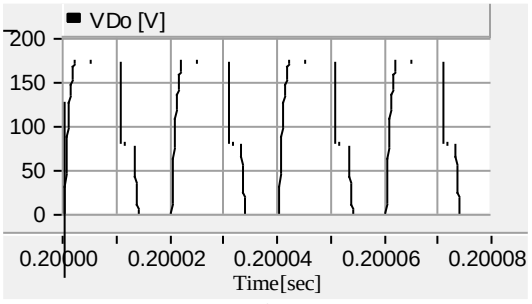


(d)

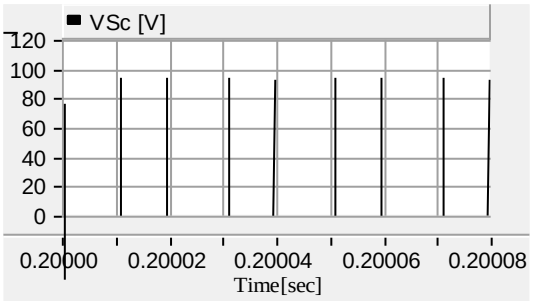


(e)

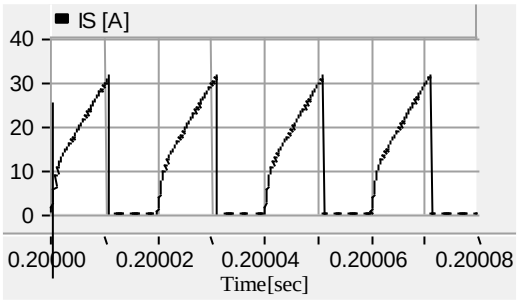


(f)

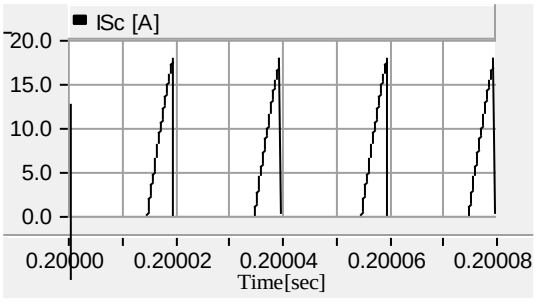
Fig. 11. (a) Output voltage (V_o), (b) leakage inductance current(I_{LK}), (c) diode current (I_{D2}) , (d) diode voltage (V_{D2}), (e) output diode current(I_{Do}), (f) output diode voltage (V_{Do}).



(a)



(b)



(c)

Fig. 12. (a) Clamped switch voltage (V_{Sc}), (b) Main switch current (I_S), (c) Clamped switch current (I_{Sc}) .

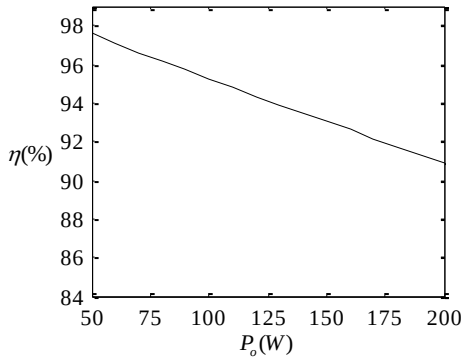


Fig. 13. Efficiency of the proposed converter versus output power.

9. CONCLUSION

This paper proposes a new structure for step-up DC-DC converter. The proposed converter is based on coupled inductor and active-clamped circuits. In the proposed converter, the voltage stress and ON-state resistance are reduced due to using active-clamped circuits. Moreover, the main switch act in ZVS in turn-on condition. Elimination of voltage spike of main switch is another advantage of the proposed converter. The proposed converter produce high voltage gain in comparison with the conventional topologies. In this paper, all equations of the components are calculated in different operating modes in both CCM and DCM operations. Moreover, the voltage gain equation is extracted for both CCM and DCM operations. The accuracy of the proposed converter is reconfirmed by simulation results in PSCAD/EMTDC software.

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