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An Interleaved Configuration of Modified KY Converter with High Conversion Ratio for Renewable Energy Applications; Design, Analysis and Implementation

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Abstract- *In this paper, a new high efficiency, high step-up, non-isolated, interleaved DC-DC converter for renewable energy applications is presented. In the suggested topology, two modified step-up KY converters are interleaved to obtain a high conversion ratio without the use of coupled inductors. In comparison with the conventional interleaved DC-DC converters such as boost, buck-boost, SEPIC, ZETA and CUK, the presented converter has higher voltage gain that is obtained with a suitable duty cycle. Despite the high voltage gain of the proposed converter, the voltage stress of the power switches and diodes is low. Therefore, switches with low conduction losses can be applied to improve the converter efficiency. Moreover, due to utilization of interleaving techniques, the input current ripple is low which makes the suggested converter a good candidate for renewable energy applications such as PV power system. Operation principle and steady-state analysis of the proposed converter in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are discussed in detail. Also, theoretical efficiency of the proposed converter is calculated. Finally, in order to evaluate the proposed converter operation by a renewable energy source such as a PV, the simulation results are presented. Moreover, a 220W prototype of the presented DC-DC converter is designed and implemented in the laboratory to verify its performance.*

Keyword: DC-DC converter, KY converter, Interleaved, High voltage gain, Low voltage stress.

1. INTRODUCTION

Renewable energy sources such as photovoltaic (PV), wind power and fuel cell (FC) are being extensively used for power generation due to the shortage of fossil fuels and environmental pollution concerns. PV power system is one of the most available and popular renewable energy sources, which are used in industrial applications. PV has important advantages such as accessibility, noise-free operation, lack of actuators and mechanical, environmentally friendly and non-contamination. Generally, the output voltage of the PV panel is not large enough for connecting to the utility grid also, their output voltage is variable, which depends on radiation and temperature. Some methods have been proposed to increase PV voltage level such as the series connection of panels. However, due to shading and panel mismatch, maximum power point tracking (MPPT) is not achieved which reduces the system efficiency. To solve these problems, a step-up DC-DC converter is required [1-3]. Fig. 1 shows the general structure of the PV power system, which includes a DC-DC converter to step up the PV generated voltage, and an inverter to deliver power to the grid [2]. Moreover, in order to track the maximum power point in PV systems, the input current of the DC-DC converter should be continuous with low ripple [4].

Several DC-DC converters with high voltage gain have been introduced in the literature survey for PV power application. Due to operational limitations and parasitic elements, the voltage gain of conventional boost, buck-boost, SEPIC, ZETA and CUK can't be too high. Moreover, in these converters, the voltage stress of switches and diodes are equal to the output voltage which increases the switches costs for applications with high output voltage [5, 6]. High voltage gain can be achieved by using coupled inductors in DC-DC converters [7-10]. These types of converters can provide a high voltage gain by using a proper turn ratio of the coupled inductor. However, in these converters, the efficiency is reduced due to losses associated with leakage inductance and high switching frequency in the transformer. Also, using a higher turn ratio to achieve a higher voltage gain causes higher EMI noise and power losses.

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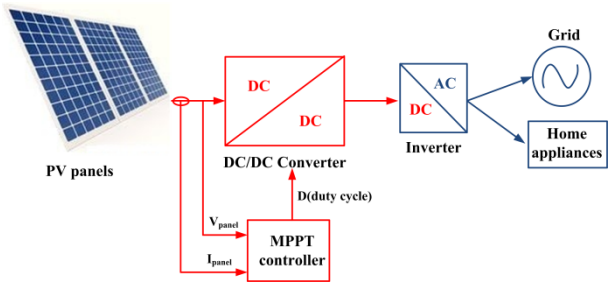


Fig. 1. General structure of a photovoltaic power system.

Furthermore, in these converters, the input current ripple is high, especially when the turn ratio of the coupled inductor is increased [11, 12].

Among various types of high step-up DC-DC converters, non-isolated converters have received significant attention due to their relatively lower size, losses, and cost [13-16]. In [17-23] voltage-boosting converters are proposed, named KY converters. In these converters, the voltage of switches is lower than the output voltage and the output voltage ripple is low. Also, these converters are very suitable for supplying power to devices that must operate under low-noise conditions. Besides, unlike the conventional boost converter, KY converter offers very fast transient load response, similar to the buck converter behavior. Also, the output current is non-pulsating in these converters. However, the voltage gain of these converters is still low which can be enhanced.

Recently, some novel structures of high step-up interleaved DC-DC converters are presented in [24-29]. This paper proposes a new high step-up interleaved DC-DC converter that is composed of two modified KY converters, in order to increase conversion voltage gain. The voltage conversion ratio of the proposed converter is higher than the interleaved configuration of conventional DC-DC converters such as boost, ZETA, CUK and SEPIC converters. The overall features of the proposed interleaved DC-DC converter are; high voltage conversion ratio, high conversion efficiency, low voltage stress of semiconductors, low ripple in the input current, low conduction and switching losses.

The remainder of this paper is organized as follows. Configuration and operation principle of the proposed converter are studied in Section 2. Steady state analysis of the converter operations in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are given in Section 3. In Section 4, design guidelines of the proposed converter are presented. Section 5 is devoted to calculation of theoretical efficiency for the suggested converter. In Section 6, comparison of the proposed converter with some similar step-up DC-DC converters is performed. Section 7 presents simulation results of the proposed converter operation by a PV source and the experimental measurement results of laboratory prototype of the proposed converter in CCM and DCM operation. As a final point, Section 8 concludes the paper.

2. CONFIGURATION AND OPERATION PRINCIPLE OF PROPOSED DC-DC CONVERTER

Fig. 2(a) indicates a step up non-isolated interleaved double dual boost converter that is presented in [29]. The voltage gain of this converter is not high enough and equals to $(1+D)/(1-D)$. Moreover, configuration of modified step-up KY converter is shown in Fig. 2(a). In this converter, the voltage of switches is lower than the output voltage, and the output voltage ripple is low. Also, the output current is non-pulsating in this converter. According to this figure, the voltage gain of this converter is obtained as follows:

$$M = \frac{1+D}{1-D} \tag{1}$$

It is obvious that the voltage gain of this converter is not high enough for some practical applications. The configuration of proposed DC-DC converter is obtained by interleaving two modified step-up KY converters to achieve a high voltage gain. As shown in Fig. 2(b), the proposed converter, named as interleaved modified KY converter, consists of two power switches S_1 and S_2 along with anti diodes, four diodes D_1, D_2, D_3 and D_4, four capacitors C_1, C_2, C_3 and C_4 which are large enough to keep the voltage across itself constant, four inductors L_1, L_2, L_3 and L_4, and two output capacitors C_{O1} and C_{O2}. In the equivalent circuit, the input and output voltages are indicated by V_{in} and V_O, and the input and output currents are represented by I_{in} and I_O, respectively. The switching frequency and switching period are represented by f_S and T_S, and duty cycle is denoted by D. The voltages across capacitors C_1, C_2, C_3, C_4, C_{O1} and C_{O2} are signified by V_{C1}, V_{C2}, V_{C3}, V_{C4}, V_{CO1} and V_{CO2}, the voltages across diodes D_1, D_2, D_3 and D_4 are indicated by V_{D1}, V_{D2}, V_{D3} and V_{D4}, and the voltage across inductors L_1, L_2, L_3 and L_4 are denoted by V_{L1}, V_{L2}, V_{L3} and V_{L4}, respectively.

The suggested DC-DC converter can be operated in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) which are analyzed in the following. In order to simplify the analysis, the following assumptions are considered:

1) The value of input voltage, V_{in}, is constant.

2) All capacitors are large enough as the voltages across

them are constant in one switching period.

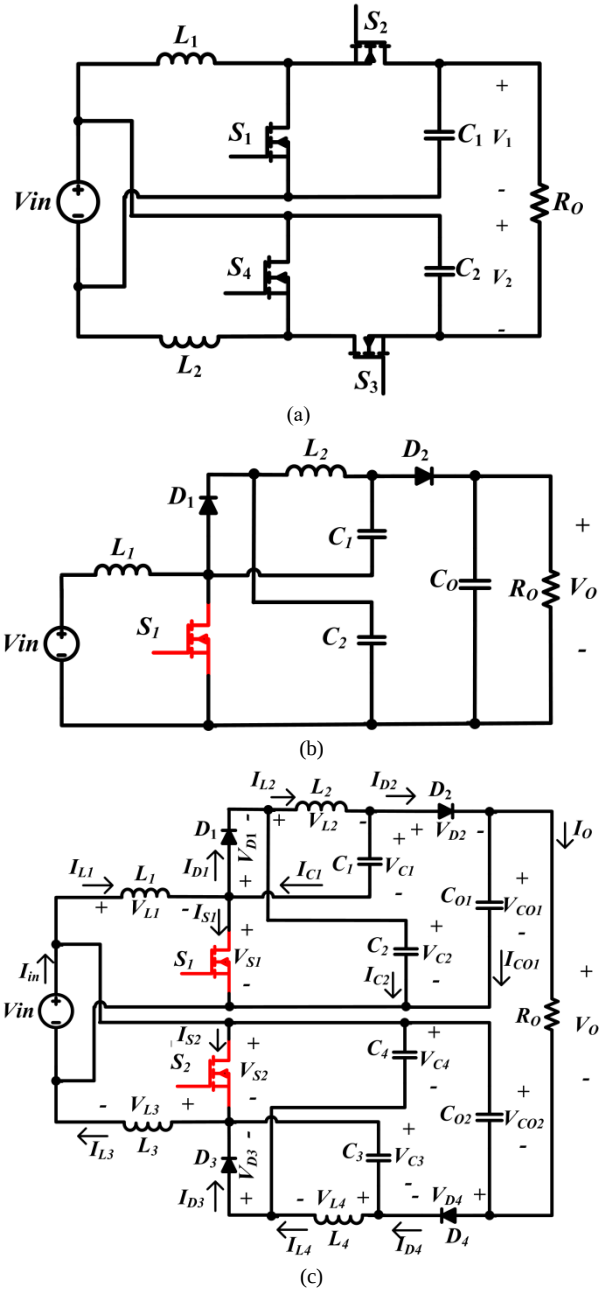


Fig. 2. (a) Base version of proposed interleaved double dual boost converter in [29], (b) Structure of modified step up KY converter, and (c) proposed interleaved DC-DC converter power circuit.

3) All components are ideal and all parasitic parameters are ignored**.**

2.1. Continuous conduction mode (CCM) operation

Following discussion is confined to CCM operation of proposed DC-DC converter in one switching period. The CCM can be divided into two operation modes. Key waveforms of the converter operation in CCM are illustrated in Fig. 3, and the corresponding equivalent circuits are shown in Fig. 4. Analysis of the converter operation in CCM is given in the following.

Mode 1 [t_0, t_1]: At the beginning of first mode, both power switches S_1 and S_2 are turned on, and diodes D_1-

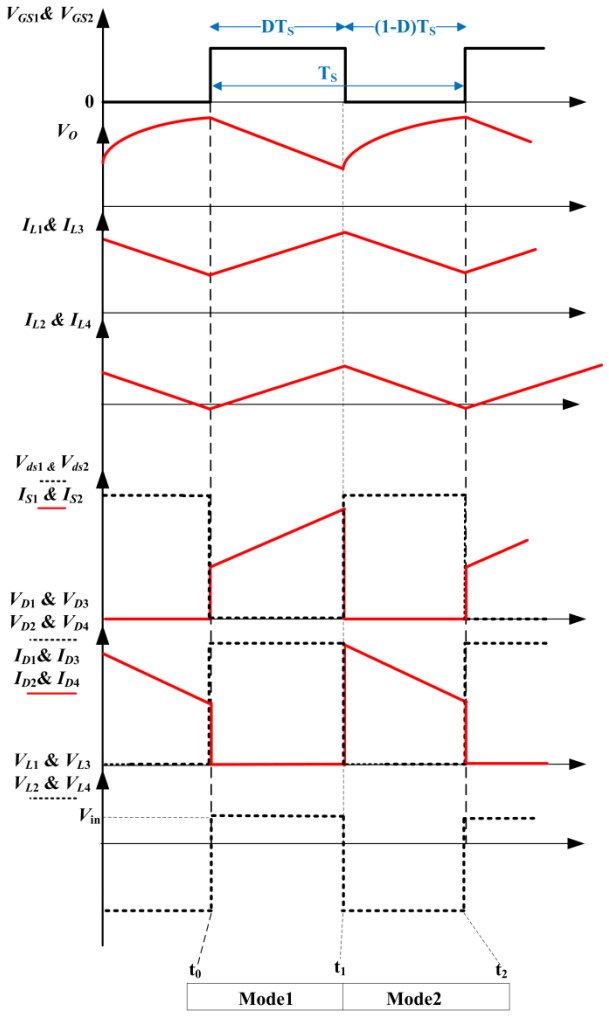


Fig. 3. Key waveforms of proposed converter operation in CCM.

D_4 are in off-state (blocked). The current flow path of this mode is indicated in Fig. 4(a). According to Fig.3, the current of inductors L_1-L_4 are linearly increased with the input voltage (V_{in}). During this time interval, the capacitors C_1 and C_3 are charged and the capacitors C_2, C_4, C_{O1} and C_{O2} are discharged. Moreover, the energy of output capacitors C_{O1} and C_{O2} transferred to the output load and supplied it. This mode ends when both power switches turned off at t=t_1. During the first mode, the voltages across the inductors L_1-L_4 are derived, as follow:

$$V_{L1(mode1)} = V_{L3(mode1)} = V_{in} \quad (2)$$

$$V_{L2(mode1)} = V_{C2} - V_{C1} \quad (3)$$

$$V_{L4(mode1)} = V_{C4} - V_{C3} \quad (4)$$

Mode 2 [t_1, t_2]: During the second mode, power switches S_1 and S_2 are turned off, and diodes D_1-D_4 starts conducting as shown in Fig. 4(b). The stored energies in inductors L_1-L_4 are decreased and their current is declined linearly to their minimum value. Moreover, the capacitors C_2 and C_4 are charged in this

time transition. The output capacitors C_{O1} and C_{O2} and

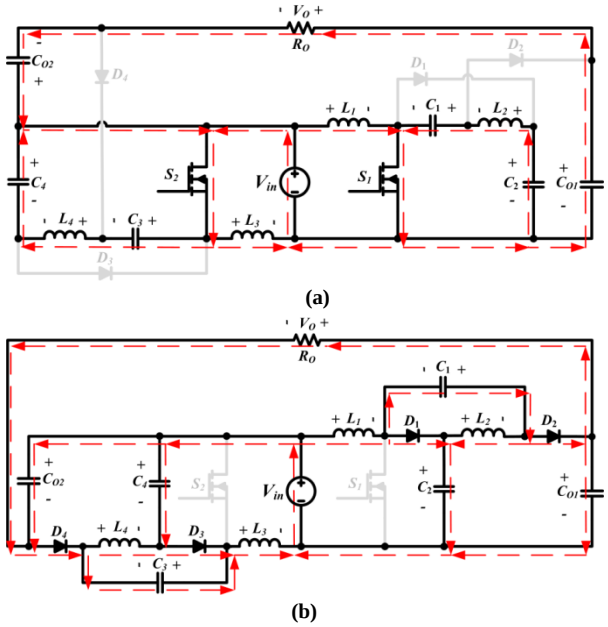


Fig. 4. Current flow path of operating modes during one switching period in CCM operation, (a) Mode 1, and (b) Mode 2.

load, R_O, are supplied from the capacitors C_1 and C_4 and input source V_{in} through diodes D_2 and D_4, respectively. This mode of operation finishes when both switches S_1 and S_2 are turned on at the next switching period. Also, the voltages across inductors L_1-L_4 during the second mode are determined, as follow:

$$V_{L1(mode\,2)} = V_{in} - V_{C2} \quad (5)$$

$$V_{L2(mode\,2)} = -V_{C1} \quad (6)$$

$$V_{L3(mode\,2)} = V_{in} - V_{C4} \quad (7)$$

$$V_{L4(mode\,2)} = -V_{C3} \quad (8)$$

2.1. Discontinuous conduction mode (DCM) operation

The key waveforms of proposed converter operation in DCM are shown in Fig. 5. There are three main modes during one switching cycle in DCM operation. The first mode operation in DCM is the same as the first mode in CCM. In the second mode, the current of the diodes are decreased, and in the third mode, the diode's D_1-D_4 currents are zero and so, diodes and switches turn off. The equivalent circuit of the third mode at DCM operation is shown in Fig. 6. In the third mode, the inductors L_1-L_4 currents are constant. Therefore, the voltages of the inductors are equal to zero.

3. STEADY-STATE ANALYSIS OF PROPOSED CONVERTER

3.1. CCM operation

In order to simplify the analysis, power losses of the switching devices are not considered. By applying volt-sec balance law on the inductors L_1-L_4 and using (2)–

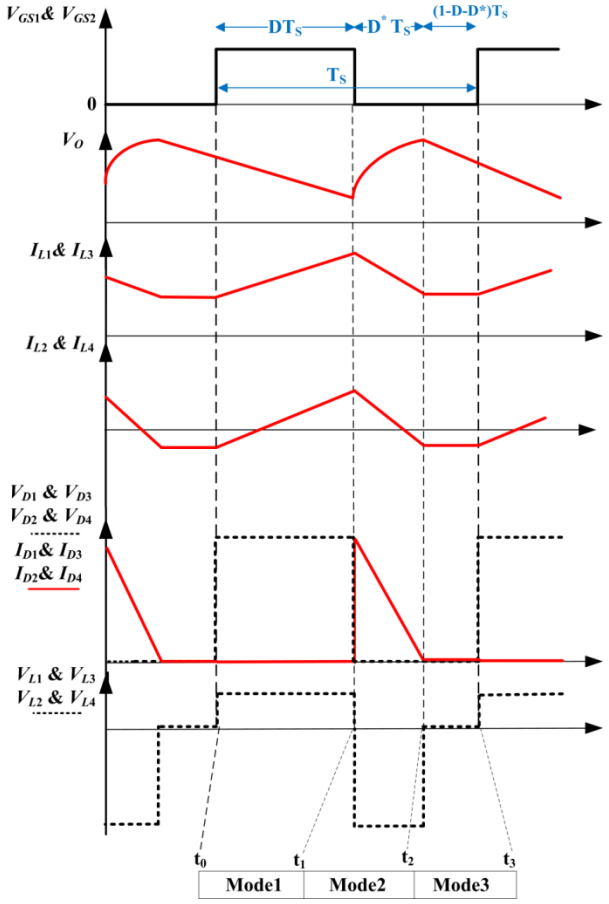


Fig. 5. Key waveforms of proposed converter operation in DCM.

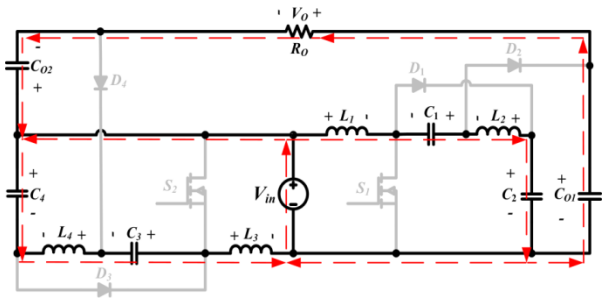


Fig. 6. Current flow path of proposed converter in third mode in DCM operation.

(8), we have:

$$\langle V_{L1}\rangle = \int_0^{DT_s} (V_{L1})dt + \int_{DT_s}^{T_s} (V_{L1})dt = \int_0^{DT_s} (V_{in})dt + \int_{DT_s}^{T_s} (V_{in} - V_{C2})dt = 0 \quad (9)$$

$$\langle V_{L2}\rangle = \int_0^{DT_s} (V_{L2})dt + \int_{DT_s}^{T_s} (V_{L2})dt = \int_0^{DT_s} (V_{C2} - V_{C1})dt + \int_{DT_s}^{T_s} (-V_{C1})dt = 0 \quad (10)$$

$$\langle V_{L3}\rangle = \int_0^{DT_s}(V_{L3})dt + \int_{DT_s}^{T_s}(V_{L3})dt = \\ = \int_0^{DT_s} V_{in}\,dt + \int_{DT_s}^{T_s}(V_{in} - V_{C4})dt = 0 \quad (11)$$

$$\langle V_{L4}\rangle = \int_0^{DT_s}(V_{L4})dt + \int_{DT_s}^{T_s}(V_{L4})dt = \\ = \int_0^{DT_s}(V_{C4} - V_{C3})dt + \int_{DT_s}^{T_s}(-V_{C3})dt = 0 \quad (12)$$

By applying KVL in mode 1, the output voltage is achieved as follows:

$$V_O = V_{CO1} - V_{in} + V_{CO2} \quad (13)$$

In mode 2, according to Fig. 4(b), the following equations are derived:

$$V_{CO1} = V_{C1} + V_{C2} \quad (14)$$

$$V_{CO2} = V_{C4} + V_{C3} \quad (15)$$

By using (9) and (10), the voltages across capacitors C_1 and C_2 are achieved as follow:

$$V_{C1} = \frac{D}{1-D}V_{in} \quad (16)$$

$$V_{C2} = \frac{1}{1-D}V_{in} \quad (17)$$

Also, by using (11) and (12), the voltages across capacitors C_3 and C_4 are obtained as given in (18) and (19).

$$V_{C3} = \frac{D}{1-D}V_{in} \quad (18)$$

$$V_{C4} = \frac{1}{1-D}V_{in} \quad (19)$$

By substituting (16) and (17) into (18), the voltage across capacitor C_{O1} is determined, as follows:

$$V_{CO1} = \frac{D+1}{(1-D)}V_{in} \quad (20)$$

Also, by substituting (18) and (19) into (15), the voltage across capacitor C_{O2} is equal to (21).

$$V_{CO2} = \frac{D+1}{(1-D)}V_{in} \quad (21)$$

From (13), (20) and (21), voltage gain of proposed converter in CCM, M_{CCM}, is calculated as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{1+3D}{1-D} \quad (22)$$

3.2. Calculation of currents

Current of inductors L_1 and L_2, I_{L1}, and I_{L2}, and capacitors C_1, C_2 and C_{O1}, $I_{C1_{(on)}}$, $I_{C2_{(on)}}$ and $I_{CO1_{(on)}}$, during switch on period (Mode1), are derived as follow:

$$I_{C1_{(on)}} = I_{L2} \quad (23)$$

$$I_{C2_{(on)}} = -I_{C1_{(on)}} = -I_{L2} \quad (24)$$

$$I_{CO1_{(on)}} = -I_O \quad (25)$$

The average of currents flow through the capacitors C_1, C_2 and C_{O1}, $I_{C1_{(off)}}$, $I_{C2_{(off)}}$ and $I_{CO1_{(off)}}$, during switch off period (Mode2), are achieved by using the following equations:

$$I_{C1_{(off)}} = I_{L2} - I_{CO1_{(off)}} - I_O = I_{L2} + I_{C2_{(off)}} - I_{L1} \quad (26)$$

$$I_{C2_{(off)}} = I_{L1} + I_{C1_{(off)}} - I_{L2} = I_{L1} - I_{CO1_{(off)}} + I_O \quad (27)$$

$$I_{CO1_{(off)}} = I_{L2} - I_{C1_{(off)}} - I_O \quad (28)$$

By applying KCL on the capacitors C_1, C_2 and C_{O1}, the following equations are expressed:

$$\int_0^{DT_s}(I_{C1_{(on)}})dt + \int_{DT_s}^{T_s}(I_{C1_{(off)}})dt = 0 \quad (29)$$

$$\int_0^{DT_s}(I_{C2_{(on)}})dt + \int_{DT_s}^{T_s}(I_{C2_{(off)}})dt = 0 \quad (30)$$

$$\int_0^{DT_s}(I_{CO1_{(on)}})dt + \int_{DT_s}^{T_s}(I_{CO1_{(off)}})dt = 0 \quad (31)$$

By substituting (23)-(28) into (29)-(31), the average of currents flow through the capacitor C_1 and C_2 during switch off period and the inductors L_1 and L_2 are calculated as given in the following:

$$I_{C1_{(off)}} = -I_{C2_{(off)}} = -\frac{D}{1-D}I_O \quad (32)$$

$$I_{L1} = \frac{I_O}{(1-D)} - I_{C1_{(off)}} = \frac{1+D}{1-D}I_O \quad (33)$$

$$I_{L2} = \frac{I_O}{1-D} + I_{C1_{(off)}} = I_O \quad (34)$$

According to Fig. (4), in the second Mode, the currents flow through the inductors L_3 and L_4, I_{L3} and I_{L4}, are equal to I_{L1} and I_{L2}, respectively; therefore, the following equations are obtained:

$$I_{L3} = \frac{1+D}{1-D}I_O \quad (35)$$

$$I_{L4} = I_O \quad (36)$$

The currents flow through the diodes D_1 and D_2, I_{D1} and I_{D2}, are determined by using the following equations.

$$I_{D1} = I_{L1} + I_{C1_{(off)}} = \frac{1}{1-D}I_O \quad (37)$$

$$I_{D1} = I_{L2} - I_{C1_{(off)}} = \frac{1}{1-D}I_O \quad (38)$$

According to Fig. 4, the currents flow through the diodes D_3 and D_4, I_{D3} and I_{D4}, are equal to I_{D1} and I_{D2}, respectively; thus, the following equation is obtained:

$$I_{D3} = I_{D4} = \frac{1}{1-D}I_O \quad (39)$$

And the currents flow through the switches S_1 and S_2, I_{S1}

and I_{S2}, are obtained as given in (40) and (41).

$$I_{S1}=I_{L1}+I_{L2}=\frac{2}{1-D}I_O \quad (40)$$

$$I_{S2}=I_{L3}+I_{L4}=\frac{2}{1-D}I_O \quad (41)$$

By using (2), (3) and (4), the integral form of currents I_{L1}-I_{L4} can be written as follow:

$$I_{L_1}=I_{L_3}=\frac{1}{L_{1,3}}\int_0^t (V_{in})dt+I_{L_{1,3}}(0) \quad (42)$$

$$I_{L_2}=\frac{1}{L_2}\int_0^t (V_{C2}-V_{C1})dt+I_{L_2}(0) \quad (43)$$

$$I_{L_4}=\frac{1}{L_4}\int_0^t (V_{C4}-V_{C3})dt+I_{L_4}(0) \quad (44)$$

According to (42)-(44), the currents ripple of inductors, ΔI_{L1}-ΔI_{L4}, are achieved as follow:

$$\Delta I_{L_1}=\Delta I_{L_3}=\frac{DV_{in}}{L_{1,3}f_S}=\frac{D(1-D)V_O}{L_{1,3}f_S(1+3D)} \quad (45)$$

$$\Delta I_{L_2}=\Delta I_{L_4}=\frac{DV_{in}}{L_{2,4}f_S}=\frac{D(1-D)V_O}{L_{2,4}f_S(1+3D)} \quad (46)$$

3.3. DCM operation

There are three modes in DCM operation. The main waveforms of DCM operation are shown in Fig. 5. Also, the current flow path of the third mode is given in Fig. 6. According to Fig. 4(b) and (37)-(39), the sum of the diodes D_1-D_4 currents can be obtained as follows:

$$I_{D1}+I_{D2}+I_{D3}+I_{D4}=I_{L1}+I_{L2}+I_{L3}+I_{L4} \quad (47)$$

The average of diodes current, $I_{D1_{(ave)}}$, $I_{D2_{(ave)}}$, $I_{D3_{(ave)}}$ and $I_{D4_{(ave)}}$, during the switching period, are derived as follows:

$$I_{D1_{(ave)}}=I_{D2_{(ave)}}=I_{D3_{(ave)}}=I_{D4_{(ave)}}=\frac{V_O}{R_O} \quad (48)$$

According to Fig. 5, the sum of the diodes average currents during one switching period is determined as given in (49).

$$I_{D1_{(ave)}}+I_{D2_{(ave)}}+I_{D3_{(ave)}}+I_{D4_{(ave)}}=\frac{1}{2}D^*I_D^{peak} \quad (49)$$

where D^* is the duty cycle in the second mode in DCM operation and I_D^{peak} is the sum of the peak currents of inductors L_1-L_4.

$$I_D^{peak}=I_{L1}^{peak}+I_{L2}^{peak}+I_{L3}^{peak}+I_{L4}^{peak}=\frac{V_{in}DT_S}{L_{eq}} \quad (50)$$

where $\frac{1}{L_{eq}}=\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3}+\frac{1}{L_4}$

By applying volt-sec balance law on inductors L_1-L_4, the switch duty cycle in the second mode in DCM, D^*, is expressed as follows:

$$D^*=\frac{4DV_{in}}{V_O-V_{in}} \quad (51)$$

Since the voltage gain in DCM operation is $M_{DCM}=(V_O/V_{in})$, therefore by using (49), the following equation is obtained:

$$D^*=\frac{4D}{M_{DCM}-1} \quad (52)$$

By using (47)-(52), the voltage gain in DCM is equal to (53).

$$M_{DCM}=\frac{V_O}{V_{in}}=\frac{1+\sqrt{1+\frac{4D^2}{\tau_L}}}{2} \quad (53)$$

where the parameter τ_L is defined as follows:

$$\tau_L=\frac{2L_{eq}}{T_S R_O} \quad (54)$$

3.4. BCM operation

When the proposed converter operates in boundary condition mode (BCM), the voltage gain of CCM operation, M_{CCM}, is equal to the voltage gain of DCM operation, M_{DCM}. Boundary normalized inductor time constant, τ_b, is derived from (22) and (53), as determined in (55):

$$\tau_b=\frac{D(1-D)^2}{2(1+3D)} \quad (55)$$

Variations of τ_b versus duty cycle are illustrated in Fig. 7. If τ_L is larger than τ_b, the proposed converter operates in CCM.

4. DESIGN PROCEDURE OF PROPOSED CONVERTER

4.1. Voltage stress analysis

In order to choose proper semiconductor devices for a converter, their voltage stress should be considered. According to operation principle of the proposed converter, the voltage stress on power switches can be achieved as follow:

$$V_{stress-S_1}=V_{stress-S_2}=\frac{1}{1-D}V_{in} \quad (56)$$

Also, the voltage stress of diodes D_1-D_4 is calculated as follow:

$$V_{stress-D_1}=-V_{C_2}=-\frac{1}{1-D}V_{in} \quad (57)$$

$$V_{stress-D_2} = V_{C_1} - V_{C_O} = -\frac{1}{1-D}V_{in} \quad (58)$$

$$V_{stress-D_3} = -V_{C_4} = -\frac{1}{1-D}V_{in} \quad (59)$$

$$V_{stress-D_4} = -V_{C_{O2}} + V_{C_3} = -\frac{1}{1-D}V_{in} \quad (60)$$

Therefore, one of the main merits of the proposed converter is that the voltage stress of switches and diodes are less than the output voltage.

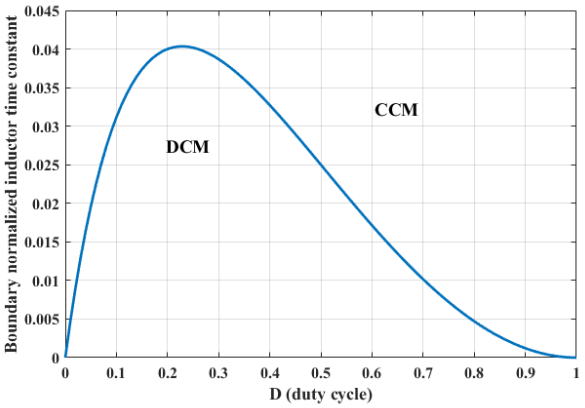


Fig. 7. Boundary normalized inductor time constant versus duty cycle.

4.2. Inductors design

To corroborate that the converter always operates in CCM, the required inductance values is obtained as given in (61).

$$I_L \geq \frac{\Delta I_L}{2} \quad (61)$$

According to (33) and (45), the minimum values of inductors L_1 and L_3 to operate in CCM are derived as follow:

$$\frac{(1+D)I_O}{(1-D)} \geq \frac{D(1-D)V_O}{2(1+3D)L_{1,3}f_S} \quad (62)$$

$$L_1 = L_3 \geq \frac{D(1-D)^2 V_O}{2(1+D)(1+3D)f_S I_O} \quad (63)$$

According to (34) and (46), the minimum values of inductors L_2 and L_4 to operate in CCM are determined as follow:

$$I_O \geq \frac{D(1-D)V_O}{2(1+3D)L_{2,4}f_S} \quad (64)$$

$$L_2 = L_4 \geq \frac{D(1-D)V_O}{2(1+3D)f_S I_O} \quad (65)$$

4.3. Capacitors design

Capacitors C_1-C_4 are designed for proposed converter by assuming same voltage ripple. According to (16)-(19), voltages of capacitors C_1-C_4 are achieved. Since the charge absorbed or produced by all the mentioned capacitors are equal, the sizes of the capacitors are obtained as follow:

$$\Delta Q = \frac{DI_O}{f_S} \quad (66)$$

$$\Delta V_C = \frac{\Delta Q}{C} \quad (67)$$

$$C_i = (DI_O / \Delta V_{Ci} f_S) \quad (68)$$

where i=1, 2, 3, 4

5. EFFICIENCY ANALYSIS

In efficiency analysis of proposed converter, parasitic resistances are expressed as follows: $r_{DS1\text{-}on}$ and $r_{DS2\text{-}on}$ are switches on-state resistances, and R_{L1}, R_{L2}, R_{L3} and R_{L4} are equivalent series resistance (ESR) of inductors L_1, L_2, L_3 and L_4, respectively. R_{FD1}, R_{FD2}, R_{FD3} and R_{FD4} are diodes D_1, D_2, D_3 and D_4 forward resistances, respectively, and V_{FD1}, V_{FD2}, V_{FD3} and V_{FD4} are their threshold voltages. Also, r_{C1}, r_{C2}, r_{C3}, r_{C4}, r_{CO1} and r_{CO2} are ESR of capacitors C_1, C_2, C_3, C_4, C_{O1} and C_{O2}, respectively. In the analysis, voltage ripple across the capacitors and the inductors are ignored.

RMS currents of the power switches S_1 and S_2, $I_{rms,S1}$, $I_{rms,S2}$, can be earned by following equations:

$$I_{rms,S1} = \sqrt{\frac{1}{T_S}\int_0^{DT_S}(I_{L1}+I_{L2})^2 dt} = \sqrt{\frac{1}{T_S}\int_0^{DT_S}(\frac{2I_O}{(1-D)})^2 dt} = \frac{2I_O\sqrt{D}}{(1-D)} \quad (69)$$

$$I_{rms,S2} = \sqrt{\frac{1}{T_S}\int_0^{DT_S}(I_{L3}+I_{L4})^2 dt} = \sqrt{\frac{1}{T_S}\int_0^{DT_S}(\frac{2I_O}{(1-D)})^2 dt} = \frac{2I_O\sqrt{D}}{(1-D)} \quad (70)$$

The conduction losses of switches S_1 and S_2 are achieved as follow:

$$P_{r_{DS1-on}} = r_{DS1-on} * (I_{rms,S1})^2 = \frac{4I_O^2 D}{(1-D)^2} r_{DS1-on} \quad (71)$$

$$P_{r_{DS2-on}} = r_{DS2-on} * (I_{rms,S2})^2 = \frac{4I_O^2 D}{(1-D)^2} r_{DS2-on} \quad (72)$$

The switching losses of the proposed converter, P_{SW1} and P_{SW2}, are obtained as given in (73) and (74).

$$P_{SW1} = f_S C_S V_{S1}^2 = f_S C_S (\frac{V_{in}}{1-D})^2 \quad (73)$$

$$P_{SW2} = f_S C_S V_{S2}^2 = f_S C_S (\frac{V_{in}}{1-D})^2 \quad (74)$$

where f_S and C_S are switching frequency and the parasitic capacitor of the main switches, respectively.

The total power losses of switches S_1 and S_2, $P_{Switch1}$ and

$P_{Switch2}$, are calculated as follow:

$$P_{Switch1} = P_{r_{DS\,1-on}} + \frac{P_{SW\,1}}{2} \tag{75}$$

$$P_{Switch2} = P_{r_{DS\,2-on}} + \frac{P_{SW\,2}}{2} \tag{76}$$

RMS currents of the diodes, $I_{rms,D1}$,, $I_{rms,D2}$ following the ained by , are obt $I_{rms,D4}$ and $I_{rms,D3}$ equation:

$$I_{rms,D1} = I_{rms,D2} = I_{rms,D3} = I_{rms,D4} = \frac{I_O}{\sqrt{(1-D)}} \tag{77}$$

The average of diodes current, $I_{D1_{(ave)}}$, $I_{D2_{(ave)}}$, , are derived as given in (78). $I_{D4_{(ave)}}$ and $I_{D3_{(ave)}}$

$$I_{D1_{(ave)}} = I_{D2_{(ave)}} = I_{D3_{(ave)}} = I_{D4_{(ave)}} = I_O \tag{78}$$

Diodes forward resistance losses, $P_{RF_{(D1)}}$, $P_{RF_{(D2)}}$, $P_{RF_{(D3)}}$ and $P_{RF_{(D4)}}$, are expressed in (79)-(82).

$$P_{RF_{(D1)}} = R_{FD1} I^2_{rms,D1} = \frac{I_O^2}{(1-D)} R_{FD1} \tag{79}$$

$$P_{RF_{(D2)}} = R_{FD2} I^2_{rms,D21} = \frac{I_O^2}{(1-D)} R_{FD2} \tag{80}$$

$$P_{RF_{(D3)}} = R_{FD3} I^2_{rms,D3} = \frac{I_O^2}{(1-D)} R_{FD3} \tag{81}$$

$$P_{RF_{(D4)}} = R_{FD4} I^2_{rms,D4} = \frac{I_O^2}{(1-D)} R_{FD4} \tag{82}$$

Diodes forward voltage losses, $P_{VF_{(D1)}}$, $P_{VF_{(D2)}}$, $P_{VF_{(D3)}}$ and $P_{VF_{(D4)}}$, are calculated as given in (83)-(86).

$$P_{VF_{(D1)}} = V_{FD1} I_{D1_{(ave)}} = I_O V_{FD1} \tag{83}$$

$$P_{VF_{(D2)}} = V_{FD2} I_{D2_{(ave)}} = I_O V_{FD2} \tag{84}$$

$$P_{VF_{(D3)}} = V_{FD3} I_{D3_{(ave)}} = I_O V_{FD3} \tag{85}$$

$$P_{VF_{(D4)}} = V_{FD4} I_{D4_{(ave)}} = I_O V_{FD4} \tag{86}$$

RMS currents of inductors, $I_{rms,L1}$, $I_{rms,L2}$, $I_{rms,L3}$ and, are determined as follow: $I_{rms,L4}$

$$I_{rms,L1} = I_{rms,L3} = \frac{(1+D)}{(1-D)} I_O \tag{87}$$

$$I_{rms,L2} = I_{rms,L4} = I_O \tag{88}$$

The conduction losses of inductors, P_{rL_1}, P_{rL_2}, P_{rL_3} and P_{rL_4}, are achieved by the following equations:

$$P_{rL_1} = R_{L1} I^2_{rms,L1} = \frac{(1+D)^2}{(1-D)^2} I_O^2 R_{L1} \tag{89}$$

$$P_{rL_2} = R_{L2} I^2_{rms,L2} = I_O^2 R_{L2} \tag{90}$$

$$P_{rL_3} = R_{L3} I^2_{rms,L3} = \frac{(1+D)^2}{(1-D)^2} I_O^2 R_{L3} \tag{91}$$

$$P_{rL_4} = R_{L4} I^2_{rms,L4} = I_O^2 R_{L4} \tag{92}$$

The RMS currents of capacitors, $I_{rms,C1}$, $I_{rms,C2}$, $I_{rms,C3}$, $I_{rms,C4}$, $I_{rms,CO1}$ and, are $I_{rms,CO2}$ obtained as given in (93).

$$I_{rms,C_{1,2,3,4}} = I_{rms,CO_{1,2}} = \sqrt{\frac{D}{(1-D)}} I_O \tag{93}$$

The power losses of capacitors, P_{RC1}, P_{RC2}, P_{RC3}, P_{RC4}, P_{RCO1} and P_{RCO2}, are according (94) and (95).

$$\begin{aligned} P_{RC\,1,2,3,4} &= r_{C\,1,2,3,4} I^2_{rms,C\,1,2,3,4} \\ &= \frac{D}{(1-D)} I_O^2 r_{C\,1,2,3,4} \end{aligned} \tag{94}$$

$$P_{RCO_{1,2}} = r_{CO_{1,2}} I^2_{rms,CO_{1,2}} = \frac{D}{(1-D)} I_O^2 r_{CO_{1,2}} \tag{95}$$

Therefore, the total power loss of the proposed DC-DC converter, P_{Loss}, is simplified as follows:

$$\begin{aligned} P_{Loss} &= P_{Switch1} + P_{Switch2} + \sum_{n=1}^{4} P_{RF_{(Dn)}} + \\ &+ \sum_{n=1}^{4} P_{VF_{(Dn)}} + \sum_{n=1}^{4} P_{rL_{(n)}} + \sum_{n=1}^{4} P_{RC_{(n)}} + \sum_{n=1}^{2} P_{RCO_{(n)}} \end{aligned} \tag{96}$$

The efficiency of the proposed converter, η, is defined as given in (97).

$$\eta = \frac{P_O}{P_O + P_{Loss}} = \frac{1}{1 + \frac{P_{Loss}}{P_O}} \tag{97}$$

According to (69)-(97), the efficiency of the proposed DC-DC converter is formulated as follows:

$$\eta = \frac{1}{1 + \frac{P_{Loss}}{P_O}} = \frac{1}{1 + \frac{A}{R_O (1-D)^2} + \frac{B}{R_O (1-D)} + \frac{C}{R_O}} \tag{98}$$

where,

$$A = 4D(r_{DS1} + r_{DS2}) + \frac{f_s C_s V_{in}^2}{I_O^2} + (1+D)^2 (R_{L1} + R_{L3})$$

$$\begin{aligned} B = &(R_{FD1} + R_{FD2} + R_{FD3} + R_{FD4}) + \\ &+ (r_{C1} + r_{C2} + r_{C3} + r_{C4}) + (r_{CO1} + r_{CO2}) \end{aligned}$$

$$C = \frac{(V_{FD1} + V_{FD2} + V_{FD3} + V_{FD4})}{I_O} + (R_{L2} + R_{L4}) .$$

6. COMPARISON STUDY

In this section, proposed DC-DC converter is compared with some similar topologies in terms of voltage gain, normalized voltage stress on power switches, boundary

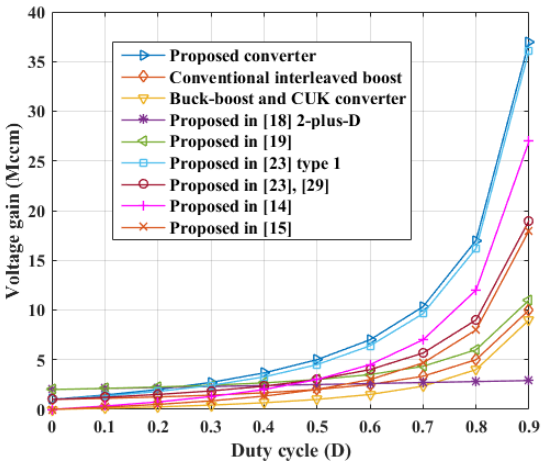
inductor time constant, cost and size. Fig. 8(a) shows comparison results of the voltage gain of the proposed converter and converters presented in [14, 15, 18, 19, 23] and [29] for various duty cycles. As shown in this figure, the voltage gain of the proposed converter is more than the other topologies for all ranges of duty cycles (even for low duty cycles). This advantage is due to using of interleaved configuration of two modified step-up KY converters in the proposed topology.

The relationship between the normalized voltage stress across power switches of the proposed converter and other converters is depicted in Fig. 8(b). According to this figure, the voltage stress of switches in the proposed topology is less than the other converters for any value of duty cycles. Hence, the cost of the proposed converter will be reduced and the overall efficiency will be increased. The boundary inductor time constant curves for the proposed converter and the other converters are shown in Fig. 8(c).

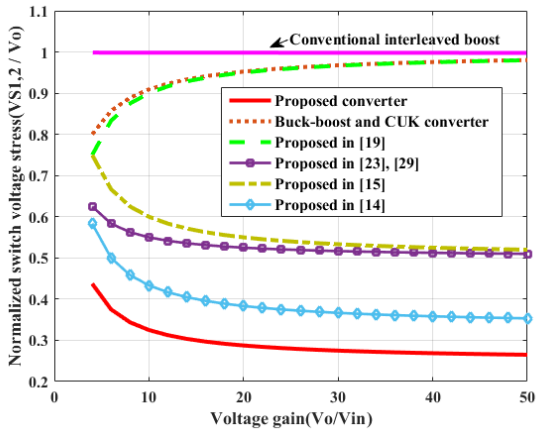
The cost comparison of the suggested converter is indicated in Table 1. With regarding this table, it is obvious that the proposed converter has low cost. By increasing the power rating the number of cores and nominal values of the power components can be decreased. So, it can be concluded that, by choosing the suitable cost of the power components, the proposed converter can be operated in high efficiency with lower cost. The size comparison of the proposed converter with other converters is indicated in table 2. According to this table, the converters presented in [14, 15, 19, 23] and [29] have lower components count versus the proposed converter. However, these converters voltage gain is very lower than the proposed converter. Also, the suggested converter has less normalized voltage stress across main power switches versus other converters. It is important to note that the proposed converter has a very low input current ripple because of its interleaved structure.

7. SIMULATION AND EXPERIMENTAL RESULTS

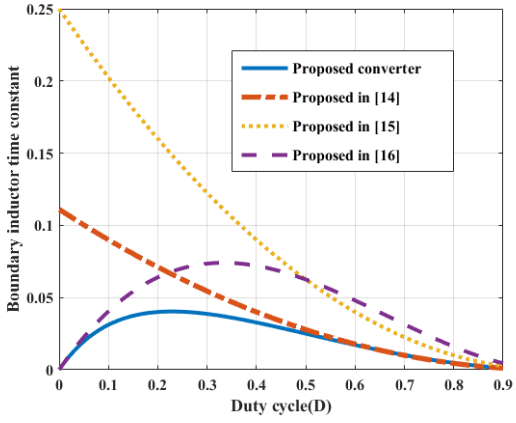
In order to confirm performance of proposed converter and evaluate its operation by a renewable energy source such as a PV, the simulation results are presented in this section. Simulation results are obtained via PSIM. The overall structure of the system studied in the simulation is indicated in Fig. 9. One of the most important factors related to a PV system is to extract the maximum power from the PV array. Many MPPT algorithms and techniques have been presented. Among them, Perturb and Observe (P&O) technique is a simple and effective method for MPPT implementation with good tracking factor [30]. The MPPT is realized by sensing the current and voltage of PV and implementing the P&O algorithm. Moreover, the duty cycle for all switching devices is generated through the P&O algorithm. The specifications of the PV array used in this study are expressed completely in Table. 3. During the simulation, the temperature is maintained at a standard level (25°C)



(a)



(b)



(c)

Fig. 8. Comparison results of proposed DC-DC converter with some similar step up topologies: (a) voltage gain of different topologies for various duty cycles, (b) normalized voltage stress of switches versus voltage conversion ratio in different topologies, and (c) curves of boundary inductor time constant.

and the intense radiation varies from 800 W/m^2 to 1000 W/m^2 and eventually changes to a radiation level of 1200 W/m^2. The I-V and P-V characteristic curves of the PV array in the intended intensity radiations are shown in Fig. 10. The simulation specifications of the proposed converter are given as follow:

C_1, C_2, C_3 and C_4: 47uF; C_{O1} and C_{O2}: 180uF; L_1, L_2, L_3 and L_4: 350uH. Simulation results of the converter operation by a PV source are given in Figs. 11 and 12. Fig. 11(a) shows the applied changes in intensity radiation.

Table 1. Costs analysis of proposed converter.

Components	No. of items	Parameters	Cost
Switches (S) (Including driver board)	4	2 IRFP260n + 2 TLP250	2*($1.65) + 2*($1.13) =$5.56
Diodes (D_1, D_2, D_3 and D_4)	4	MUR1560	4 * ($2.25)=$9
Inductors (including core and wire)	4	2*(350uH-6A) + 2*(350uH-2A)	2*($6) + 2*(4) = $20
Capacitors (C_1, C_2, C_3 and C_4)	4	(47uF/250V)	4*($0.22) =$0.88
Output capacitors (C_{O1} and C_{O2})	2	(180uF/400V)	2*($1.32) =$2.64
Input capacitor (C_{in})	1	470 uF/ 63V	$0.17

Table 2. Size comparison of proposed converter with other presented topologies.

Reference	Number of Components				Voltage Gain	NVS on Switch
	D	C	S	Co		
Proposed converter	4	6	2	4	$\frac{1+3D}{1-D}$	$\frac{M-1}{M+3}$
Converter in [14]	3	5	1	3	$\frac{3D}{1-D}$	$\frac{M+3}{3M}$
Converter in [15]	2	4	1	3	$\frac{2D}{1-D}$	$\frac{M+2}{2M}$
Converter in [19]	1	2	2	2	$\frac{2-D}{1-D}$	$\frac{M-1}{M}$
Converter in [23]	1	3	2	1	$\frac{1+D}{1-D}$	$\frac{M+1}{2M}$
Converter in [29]	4	2	4	2	$\frac{1+D}{1-D}$	$\frac{M+1}{2M}$

D: Diode; C: Capacitor; S:switch; Co: Core; NVS: Normalized voltage stress; M= V_O/V_{in}

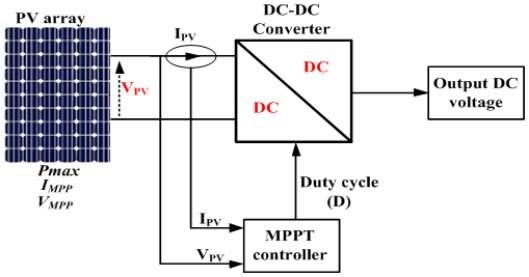


Fig. 9. General structure of simulated system in the PSIM.

Table 3. Specifications of utilized PV array in simulation (1000 W/m^2, 25°C).

Specifications	Values
Number of Cells (N_S)	62
Maximum power of PV (P_{max})	104.25 W
Voltage of MPP (V_{max})	29.34 V
Current of MPP (I_{max})	3.55 A
Open circuit voltage of PV (V_{OC})	21.1 V
Short circuit current of PV (I_{SC})	3.8 A
Temperature Coeff of V_{OC}	-0.38
Temperature Coeff of I_{SC}	0.065
dv/di at V_{OC}	-0.68

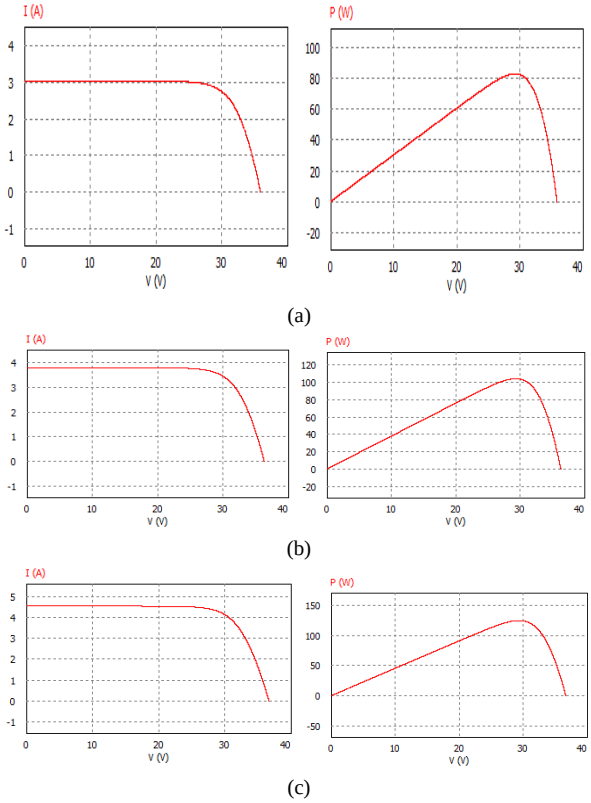
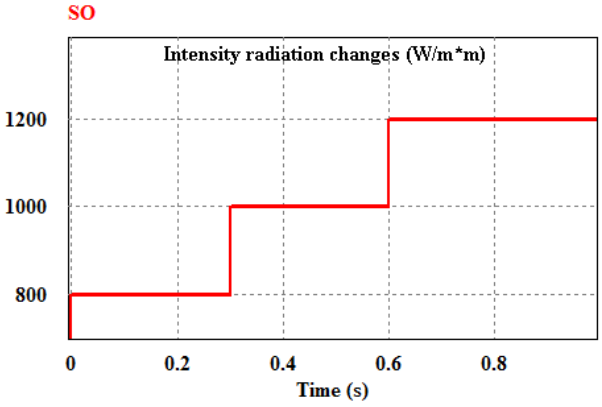


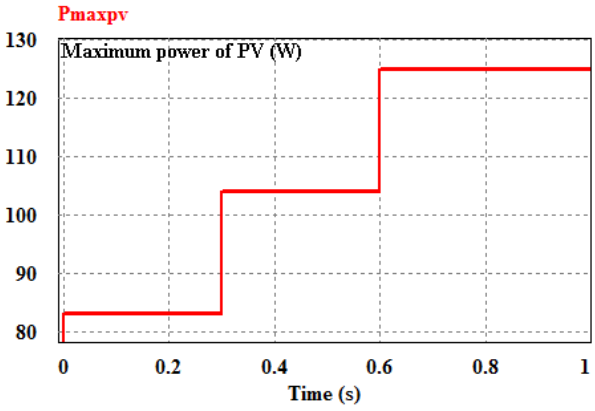
Fig. 10. I-V and P-V characteristic curves of the PV array, (a) 800 W/m^2, (b) 1000 W/m^2, and (c) 1200 W/m^2.

According to Fig. 11(b), the maximum power of the PV for each intensity radiation is indicated. The PV array outputs; power, voltage and current are illustrated in

Fig. 12(a)-(c), respectively. The PV array voltage is less and the proposed DC-DC converter boosts PV voltage. The presented converter boosts PV voltage and extracts maximum power from the PV array. According to PV array specifications in Table.3 and Fig. 10, the maximum power of PV array in 800, 1000 and 1200 (W/m^2) irradiance are 83.19, 104.25 and 125.09 (W) in standard test conditions. Fig. 12(a)-(c) verifies extracting maximum power from PV array.



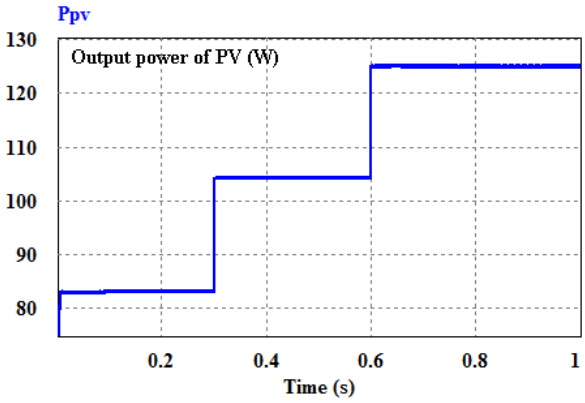
(a)



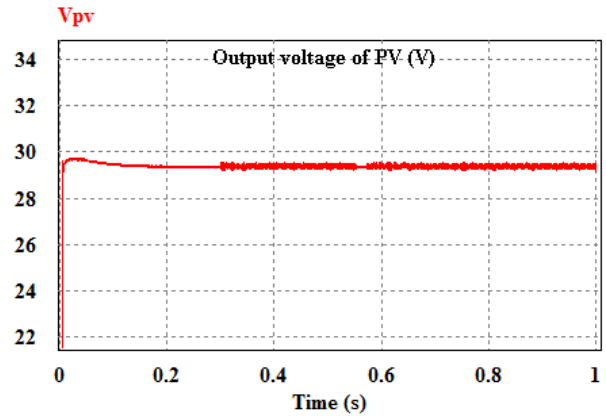
(b)

Fig. 11. Simulation results, (a) applied changes in intensity radiation, and (b) maximum PV power diagram for each three intensity radiations.

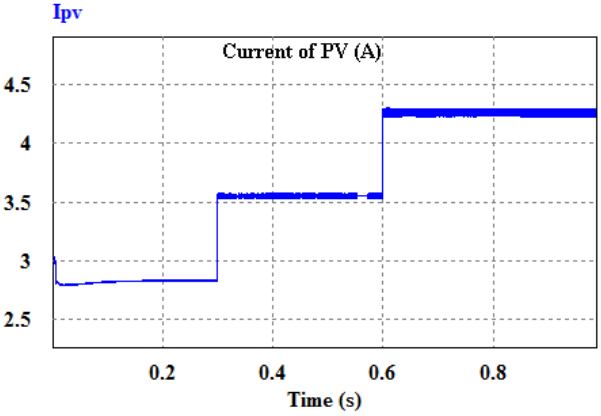
Moreover, the output power and voltage of the proposed converter for the applied changes is shown in Fig. 12(d) and (e), respectively.



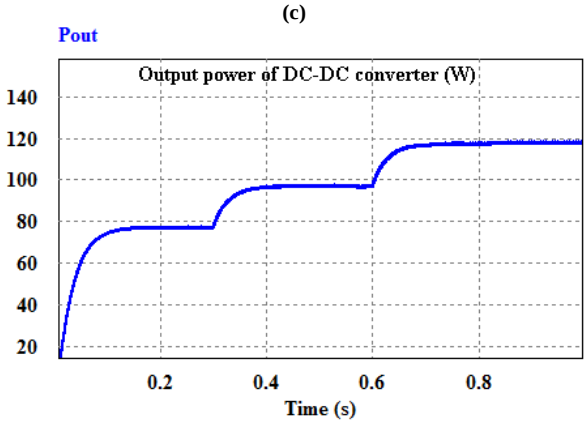
(a)



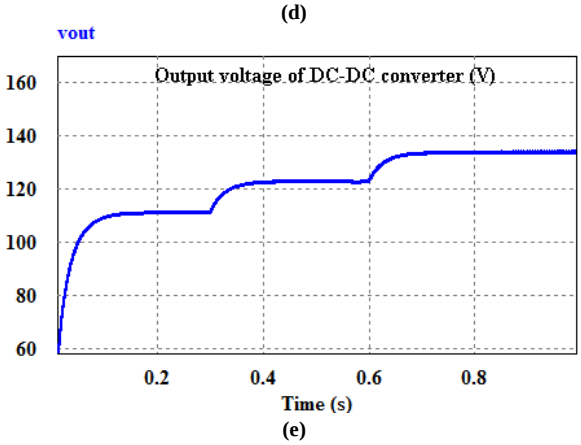
(b)



(c)



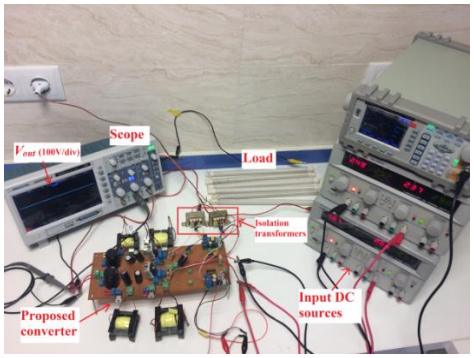
(d)



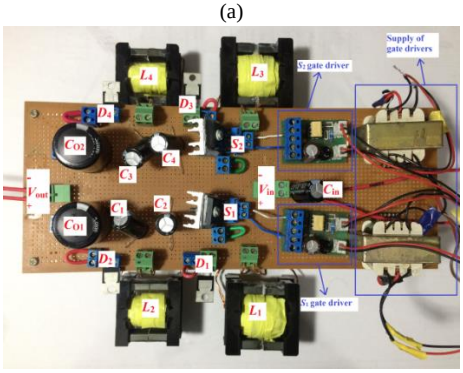
(e)

Fig. 12. Simulation results, (a) output power of PV, (b) output voltage of PV, (c) current of PV, (d) output power of DC-DC converter, and (e) output voltage of DC-DC converter.

In order to verify theoretical analysis of proposed DC-DC converter, a 220W prototype is implemented in the laboratory as shown in Fig. 13. The specifications of the implemented prototype are given in Table 4. The proposed converter converts 29V input voltage to 325V in the output. The switching frequency of the prototype is selected 30KHz. All applied diodes are ultrafast rectifiers (MUR1560) with low forward voltage drop, and power switches are selected MOSFET IRFP260n with low on-resistance. According to Table 4, all of applied diodes D_1-D_4, inductors L_1-L_4 and capacitors C_1-C_4 are identical in the structure of implemented prototype.



(a)



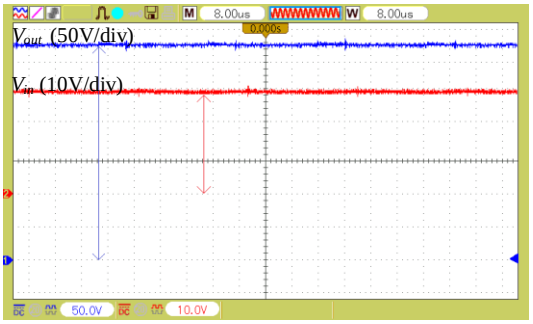
(b)

Fig. 13. Implemented prototype of proposed DC-DC converter, (a) overall system, and (b) power circuit.

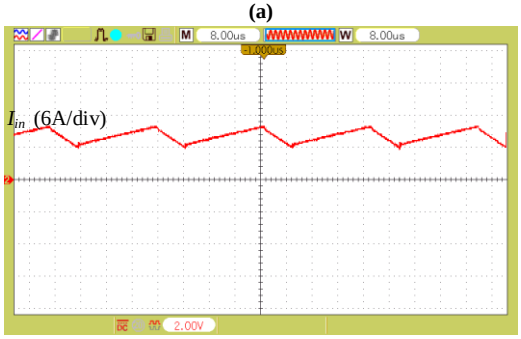
Table 4. Circuit parameters of implemented prototype.

Specifications	Values
Input voltage	29 V
Output voltage	325 V
Output power	220 Watt
Switching frequency	30 kHz
C_1, C_2, C_3, and C_4	47 uF/ 250 V
C_{O1}, C_{O2}	180 uF/ 400V
C_{in}	470 uF/ 63V
Inductors, L_1, L_2, L_3, L_4	350 uH
Power switches, S_1 and S_2	IRFP260n
D_1, D_2, D_3 *and* D_4	MUR1560
Switch gate drivers	TLP250
Duty cycle	0.73

Experimental measurement results of the converter operation in CCM are given in Figs. 14-17. In all of the figures, time per division is set to be 8µs. Output and input voltage waveforms are shown in Fig. 14(a). The input and output voltages are equal to 29V and 325V, respectively. Also, as shown in this figure, the output voltage ripple is very low. The measured input current, I_{in}, is shown in Fig. 14(b). As indicated in this figure, the input current is continuous, so the proposed converter is suitable for photovoltaic application. Voltage stress of switch S_1 is shown in Fig. 14(c). It is shown that the maximum voltage on the power switch is about 100V.



(a)



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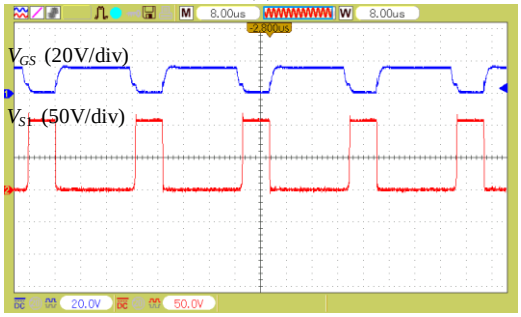

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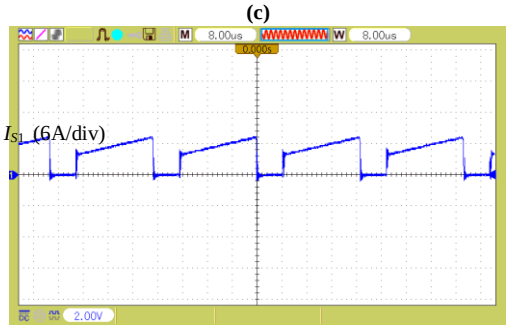

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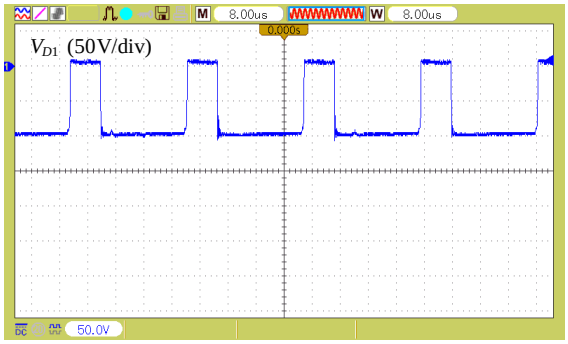

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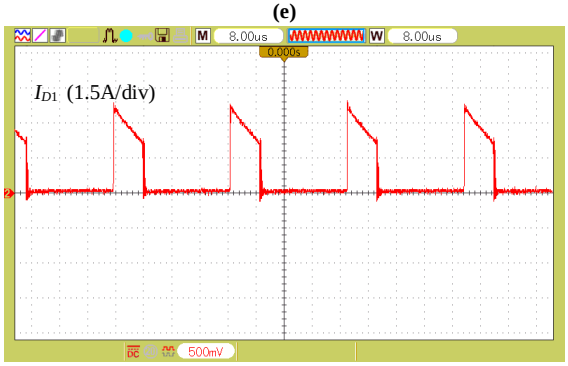
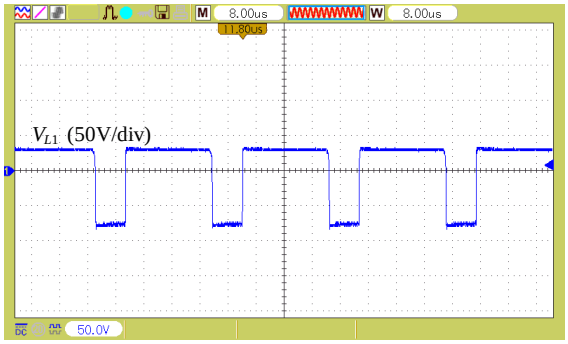


(f)

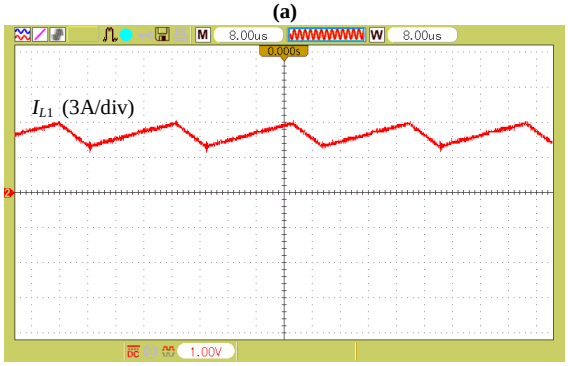
Fig. 14. Experimental measurement results of proposed DC-DC converter at CCM operation, (a) input and output voltages, (b) input current, (c) voltage of switch S_1, (d) current of switch S_1, (e) voltage of diode D_1, and (f) current of diode D_1.

Therefore, a switch with low on-resistant can be used. Also, according to Fig. 14(c), the duty ratio of the power switch is about 0.73. The switch current waveform is shown in Fig. 14(d). When the switch is turned on, the current with a maximum of 7.2A flows through the switch. Fig. 14(e) represents the voltage stress waveform of diode D_1. The measured voltage across the diodes D_1 is found to be about 100V. It is clear that the voltage stress is far lower than the output voltage; hence, the ultrafast diode is used to completely eliminate the reverse recovery current. Also, the current of the diode is depicted in Fig. 14(f). The current with a maximum of 3.9A flows through the diode when it is turned on. Voltage and current waveforms of inductors L_1 and L_2 are shown in Fig. 15. The obtained waveforms are similar to Fig. 3 that confirms the theoretical analysis. The voltage waveforms of the capacitors C_1, C_2, C_3, C_4, C_{O1} and C_{O1} are shown in Fig. 16. As shown in this figure, the voltages across the capacitors C_1 and C_2 are about 80V and 100V, respectively which are in good agreement with the results achieved in (15) and (16), respectively. Fig. 16(c) shows the voltages of capacitors C_{O1} and C_{O2} which are equal to 180V. This value confirms the theoretical results obtained from (19) and (20), respectively.

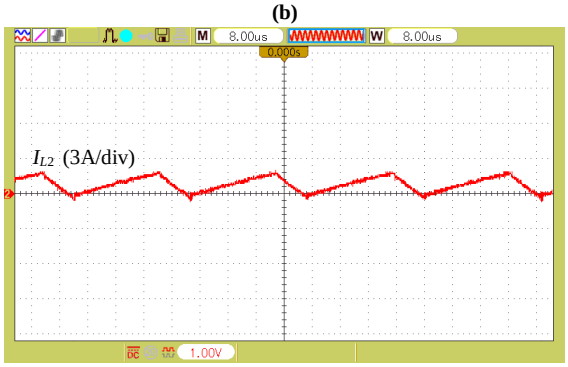
Fig. 17 shows theoretical and experimental measured efficiency of the proposed converter for several output powers. To draw the theoretical efficiency curve, the on-state resistances of the switches and diodes are considered to be 0.045Ω and 0.02Ω, respectively. The experimentally measured efficiency of the proposed converter under the output power of 220W is equal to 96.2%. The results confirm the high conversion efficiency of the presented converter.



(a)



(b)



(c)

Fig. 15. Measured waveforms of (a) inductor L_1 voltage, (b) inductor L_1 current, and (c) inductor L_2 current.

Furthermore, to confirm the theoretical analysis of proposed converter at DCM operation and validate the performance of the converter, the experimental results of the implemented converter during DCM operation are presented. For the operation of the converter in DCM, the duty cycle is considered 25% (D = 25%). The switching frequency is also considered to be 20 kHz and the output load is chosen to be 320 ohms. Experimental measurement results of the converter operation in DCM are given in Figs. 18-20. In all of the figures, time per division is set to be 20μs. Output voltage waveform is

shown in Fig. 18(a). The measured input current, I_{in}, is shown in Fig. 18(b). Fig. 18(c) indicates the signal which is applied to the switch and voltage stress across it. Fig. 18(d) show the current flows through the switch in DCM operation. Fig. 18(e) and (f) represent the voltage stress and current waveform of diode D_1. The obtained waveforms are similar to Fig. 5 that confirms the theoretical analysis. Voltage and current waveforms of inductors L_1 and L_2 are shown in Fig. 19. As it is shown in this figure, the converter operates in DCM. Moreover, the voltage waveforms of the capacitors C_1, C_2, C_3, C_4, C_{O1} and C_{O2} in DCM operation are shown in Fig. 20.

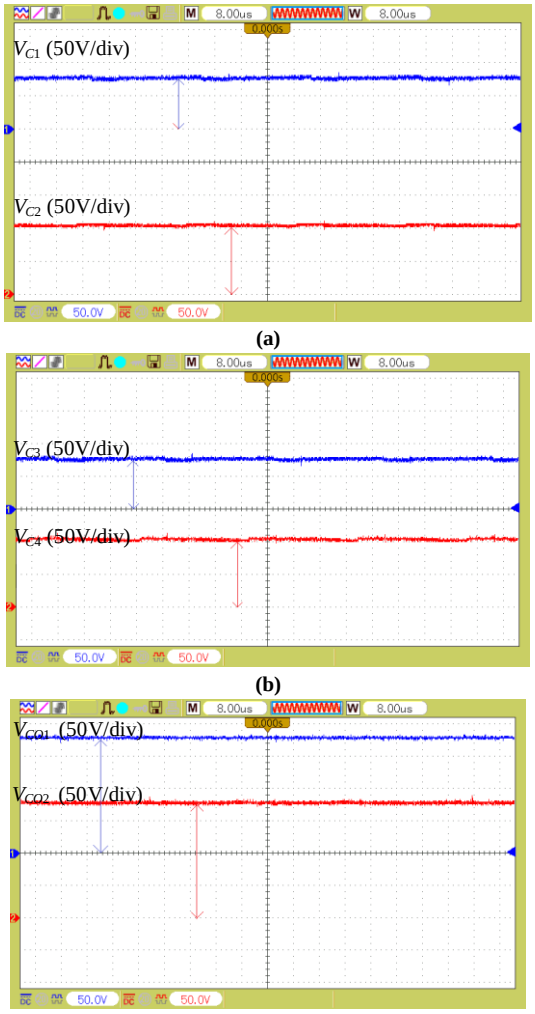


Fig. 16. Measured voltage waveforms of capacitors, (a) C_1 and C_2, (b) C_3 and C_4, and (c) C_{O1} and C_{O2}.

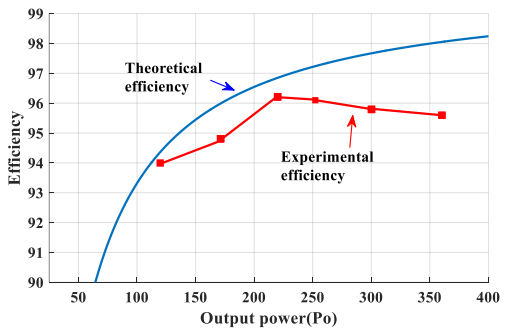
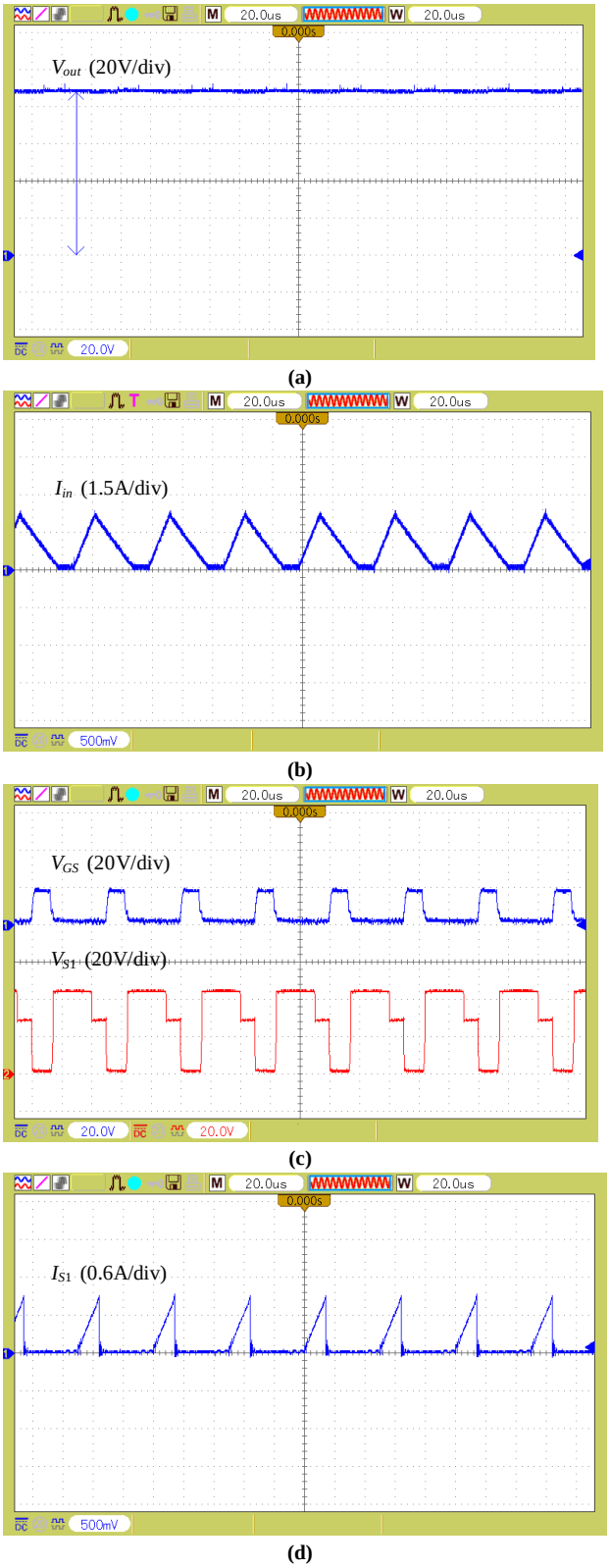
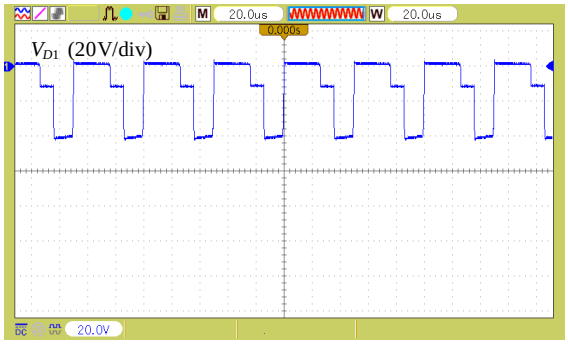
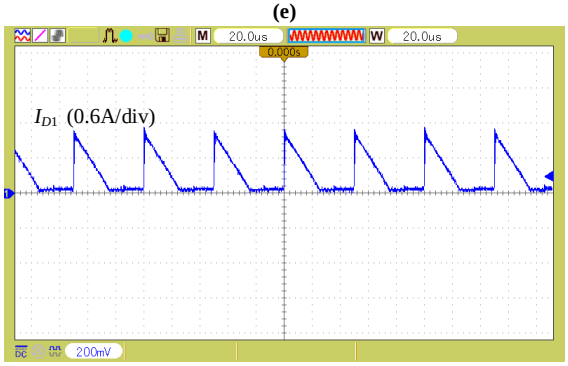


Fig. 17. Theoretical and experimental measured efficiency of proposed converter for $R_{L1,3}$=40mΩ, $R_{L2,4}$=30mΩ, $r_{CO1,2}$=10mΩ, r_{C1-4}=10mΩ, f_S=30kHz, C_S=603pF, $V_{FD1,2,3,4}$=1.2V, V_O=325V, P_O=220W.





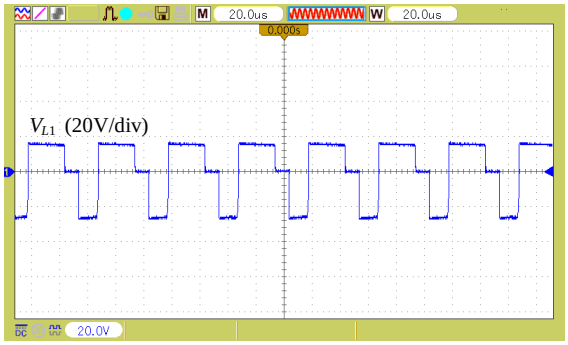
(e)



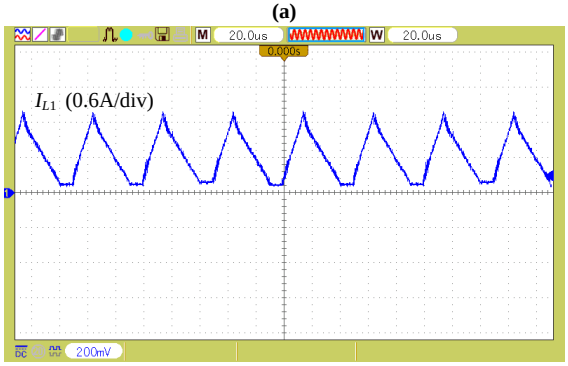
(f)

Fig. 18. Experimental measurement results of proposed DC-DC converter operation in DCM, (a) output voltage, (b) input current, (c) voltage of switch S_1, (d) current of switch S_1, (e) voltage of diode D_1, and (f) current of diode D_1.

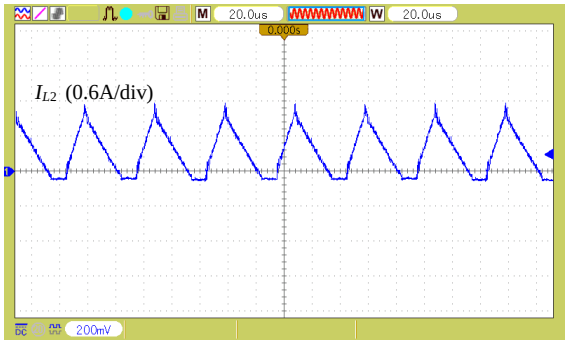
Finally, according to the experimental measurement results, the analysis and feasibility of the proposed converter in CCM and DCM are validated.



(a)



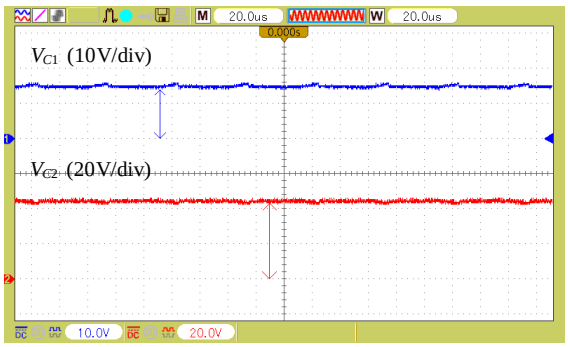
(b)



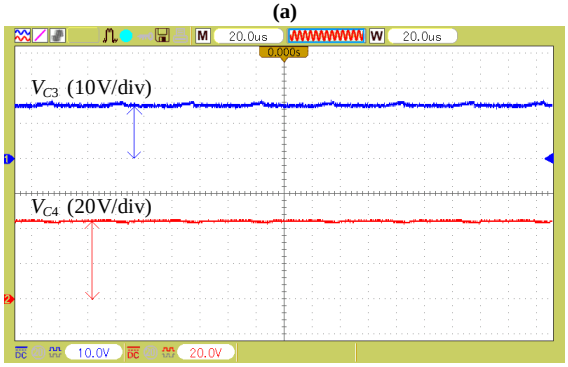
(c)

Fig. 19. Experimental measurement results in DCM operation: measured waveforms of (a) inductor L_1 voltage, (b) inductor L_1 current, and (c) inductor L_2 current.

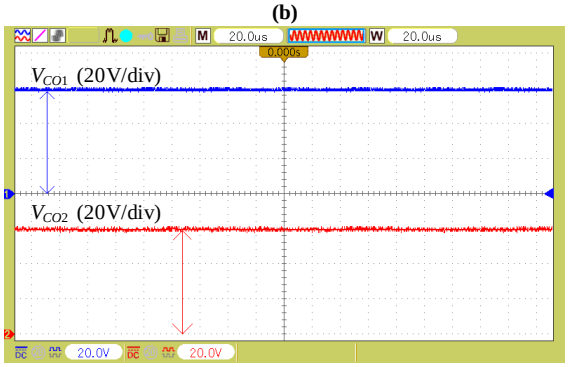
Analysis and experimental tests indicate the suitability of the presented interleaved DC-DC converter for applications such as PV power systems.



(a)



(b)



(c)

Fig. 20. Measured voltage waveforms of capacitors in DCM operation, (a) C_1 and C_2, (b) C_3 and C_4, and (c) C_{O1} and C_{O2}

8. CONCLUSIONS

A high step-up, non-isolated, interleaved DC-DC converter was presented in this paper. By using two interleaved modified KY converters, a high voltage gain is achieved for the proposed converter. The voltage stress across the power switches is low and so, switches with low on-state resistance can be applied. Due to low ripple in the input current, the proposed converter is suitable for applications such as PV power system. The converter operation in CCM, DCM and BCM were discussed in detail. Then, the converter voltage gain, capacitors and inductors design procedure and voltage stress of semiconductors in steady-state were analyzed. The proposed converter is compared with some similar topologies where the comparison results show that the proposed converter voltage gain is higher and voltage stress on semiconductors is lower than the other topologies. Also, according to comparison section, the results confirm that the proposed converter has a wide CCM operation range and can be operated in high efficiency with lower cost. Moreover, the theoretical efficiency of the presented converter was calculated in detail. Finally, simulation results of the proposed converter operation by a PV source were presented. Moreover, to validate the theoretical analysis, a laboratory prototype of the proposed converter was implemented in 220W of output power with 96.2% conversion efficiency.

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