Analysis and Design of a New Single Switch Non-Isolated Buck-Boost DC-DC Converter

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Abstract- *In this paper, a new transformerless buck-boost converter based on ZETA converter is introduced. The proposed converter has the ZETA converter advantages such as, buck-boost capability and input to output DC insulation. The suggested converter voltage gain is higher than the classic ZETA converter. In the presented converter, only one main switch is utilized. The proposed converter offers low voltage stress of the switch; therefore, the low on-state resistance of the main switch can be selected to decrease losses of the switch. The presented converter topology is simple; hence, the control of the converter is simple. The mathematical analyses of the proposed converter are given. The experimental results confirm the correctness of the analysis.*

Keyword: Transformerless buck-boost converter, voltage gain, main switch, voltage stress.

1. INTRODUCTION

Fossil fuels are vital sources and these fuels are utilized widely in recent years. Fossil fuels have produced many problems such as air pollution, climate change, global warming problems, and other similar troubles to the environment. Renewable energy systems have been distinguished as the best alternative to fossil fuels [1-3]. Fuel cell and Photovoltaic (PV) are the two main renewable energy sources. However, the voltage of these systems is too low and unstable to be connected to the utility grid. Hence, high voltage converters should be used to increase the DC voltage of the fuel cell and PV into the DC voltage. The classic boost converter could be a suitable choice, owing to static voltage gain and simple structure [4]. A classic boost converter can be utilized to create high step-up voltage gain with high duty cycle. However, this converter has some disadvantage such as high switching losses, diode reverse-recovery problem, and electromagnetic interference (EMI) problem. In addition, the stresses of the switch and the diode of the classic boost converter are high. Hence, the high voltage rated switch should be used and the conduction and switching losses will be

increased. The maximum of the voltage gain of the classic boost cannot be more than five [5-9]. The quadratic boost converter is high voltage gain converter, which has only one main switch. The voltage gain of the converter is a quadratic function of a classic boost converter. The switch stress of the converter is equal to the output voltage. Hence, switch with high current can be selected [10-11]. Converters with the coupled inductor are good choices for achieving high voltage by adjusting the coupled inductor turns ratio. However, the coupled inductor leakage inductance makes high voltage stress of the switch and conduction loss. The switched-capacitor technique can be used for earning high voltage. However, in these converters, many switches are utilized, which cause high losses. Some advantages of these converters are the low input ripple, high voltage gain, and low voltage stress of the switch [12-13]. In Ref. [14], a high voltage gain transformerless converter based on the switched inductor and capacitor and active network is proposed. This converter has two switches, which cause high conduction losses. The converter provides high voltage gain with low voltage stress. In Ref. [15], a transformerless converter with very high step-down voltage gain is proposed. In this converter, five power switches are utilized, which cause high switching and conduction losses. The voltage gain of the converter is three times lower compared to the voltage gain of the classic buck converter. In Ref. [16], a transformerless converter based on diode-capacitor cell is proposed. The converter has some advantages such as high voltage gain, low diodes and switches

stresses, low ripple, and high efficiency. In Ref. [17], high step-up transformerless converters are proposed. In these converters one main switch is used. In Ref. [18], a transformerless buck-boost converter is proposed. This converter has three main switches. In this converter, the voltage stress of the switch is equal to the output voltage. The converter conduction and switching losses are high. In Ref. [19], a buck-boost converter combining KY and the classic buck converter is proposed. In this converter two switches are used. Hence, the conduction and switching losses will be high. In Ref. [20], a transformerless buck-boost converter with high voltage gain is proposed. The voltage gain of the converter is squared times of the classic buck-boost converter. The stress of the switch and the diode is high. Hence, the losses of the converter will be high. In Ref. [21], a multi phase transformerless dc-dc converter with high voltage gain is proposed. The voltage stress of the converter is low. Hence, the losses can be reduced. In Ref. [22], a high step-down transformerless converter is suggested. In this converter, four switches are used. The voltage stress of the elements of the converter is high. Hence, the efficiency will be low. In Ref. [23], a DC-DC converter based on ZETA and Buck-Boost converters is presented. This converter has two-output. In the converter, one switch is used and converter has low number of components. In Ref. [24], a bidirectional dc-dc converter based on ZETA converter is proposed. This converter has high conversion ratio and the leakage-inductor energy can be recycled; therefore, the switch stress will be low. In Ref. [25], transformerless high step-up dc-dc converters are proposed. In Ref. [26], a high voltage gain converter is presented. In this converter, the switched inductor and three level converters are used. The converter has two switches; hence the conduction losses of the converter will be high. In Ref. [27], a high step-up converter is proposed. In this converter, active clamp circuit is used; therefore the voltage stress of the switch can be reduced. In Ref. [28] a high step-up transformerless converter is proposed. In this converter, two switches are used and the switched-inductor and switched-capacitor are utilized. In the converter, the output current is continuous. In Ref. [29] a buck-boost converter is suggested. The advantages of the converter are high voltage gain and positive output voltage. The converter has two switches and the voltage stresses of the switches are high and therefore, the losses of the converter will be high. In Ref. [30] a transformerless high step-up DC-DC converter based on the Cockcroft-Walton Voltage Multiplier is proposed. This converter employs two main switches and the diodes and switches

stresses are high. In Ref. [31] a high step-up interleaved converter is presented. In this converter, the interleaved boost converter and the voltage-double module are used and the converter has two main switches and the stresses of the diodes of the converter are high. In Ref. [32] a high step-up converter with the coupled inductor is proposed. This converter has one main switch and the stress across the main switch is reduced. However, the voltage stresses of the three diodes of the converter are high. In this converter, the leakage inductance energy can be recycled. In Ref. [33] a transformerless buck-boost converter is suggested. In this converter, one main switch is used. The switch voltage stress of the converter is high and therefore, the converter switch loss will be high. In referneces [34-37] high voltage gain transformerless converters are proposed. In this paper, a novel transformerless buck boost converter based on ZETA converter is proposed. The converter voltage gain is higher than the classic buck-boost converter, ZETA, CUK, and SEPIC converters. The proposed converter topology is very simple; hence, the converter control is simple. This converter has one main switch. The main switch and diodes stresses are less than the output voltage, hence the switch loss will be low and the converter efficiency can be improved. The buck-boost converters are used in some applications like LED drivers, fuel-cell, and car electronic devices. The modes analysis is explained and to confirm the operation of the converter, experimental results are given.

2. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 1 shows the circuit topology of the presented converter. The converter consists one main switch S , two diodes D_1 and D_2, three inductors L_1, L_2 and L_3, four capacitors C_1, C_2, C_3 and C_4 and load R .

To simplify the analysis of the new buck-boost converter, the following conditions were considered:

1) All capacitors are large enough hence; the voltages of the capacitors can be seen as constant.

2) Semiconductor elements such as diodes and switch are ideal.

The proposed converter can be used in the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM). The continuous conduction mode has two operating modes. The analysis of the converter at (CCM) is presented in detail as follows:

1) State 1 $[t_0, t_1]$ *:* During this time interval, the switch S is turned ON and the diodes D_1 and D_2 are

turned OFF. The current-flow path is shown in Fig. 2(a). The inductors L_1, L_2 and L_3 are magnetized. The capacitor C_1 and C_2 are discharged and the capacitor C_4 is charged. Thus, the corresponding equations can be achieved as follows:

$$V_{L1} = V_i \tag{1}$$

$$V_{L2} = V_{C1} + V_i - V_{C4} \tag{2}$$

$$V_{L3} = V_i + V_{C1} + V_{C2} - V_{C3} - V_{C4} \tag{3}$$

2) State 2 $[t_1, t_2]$: The current-flow path is shown in Fig. 2(b). During this time interval, switch S is turned OFF. Diodes D_1 and D_2 are turned ON. The inductors L_1, L_2 and L_3 are demagnetized. The capacitor C_1 is charged by the inductor L_1 and the capacitor C_2 is charged by the inductor L_2 . The capacitor C_4 is discharged. The voltages of inductors are obtained as follows:

$$V_{L1} = -V_{C1} \tag{4}$$

$$V_{L2} = -V_{C2} = -V_{C4} \tag{5}$$

$$V_{L3} = -V_{C3} \tag{6}$$

3. STEADY STATE ANALYSIS OF THE PROPOSED CONVERTER

3.1. Voltage gain

By applying volt-sec balance principle on L_1, L_2 and L_3 and using (1)-(6), we have:

$$\frac{1}{T_s} \left(\int_0^{DT_s} (V_i) dt + \int_{DT_s}^{T_s} (-V_{C1}) dt \right) = 0 \tag{7}$$

$$\frac{1}{T_s} \left(\int_0^{DT_s} (V_{C1} + V_i - V_{C4}) dt + \int_{DT_s}^{T_s} (-V_{C4}) dt \right) = 0 \tag{8}$$

$$\frac{1}{T_s} \left(\int_0^{DT_s} (V_i + V_{C1} + V_{C2} - V_{C3} - V_{C4}) dt + \int_{DT_s}^{T_s} (-V_{C3}) dt \right) = 0 \tag{9}$$

By using (5), (7), (8) and (9), the voltage of the capacitors C_1, C_2 and C_3 $(V_{C1}, V_{C2}, V_{C3}$ and $V_{C4})$ can be achieved as follows:

$$V_{C1} = V_{C2} = V_{C3} = V_{C4} = \frac{D}{1-D} V_i \tag{10}$$

By using (10), the voltage transfer gain (M_{CCM}) can be found as follows:

$$M_{CCM} = \frac{V_o}{V_i} = \frac{2D}{1-D} \tag{11}$$

According to (11), it is apparent that the voltage gain of the proposed converter is twice as large as the ZETA converter. Therefore, the voltage gain of the converter is higher than that of ZETA converter. Fig. 3. shows some key waveforms of the proposed converter in (CCM).
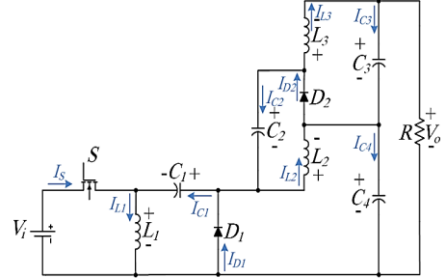

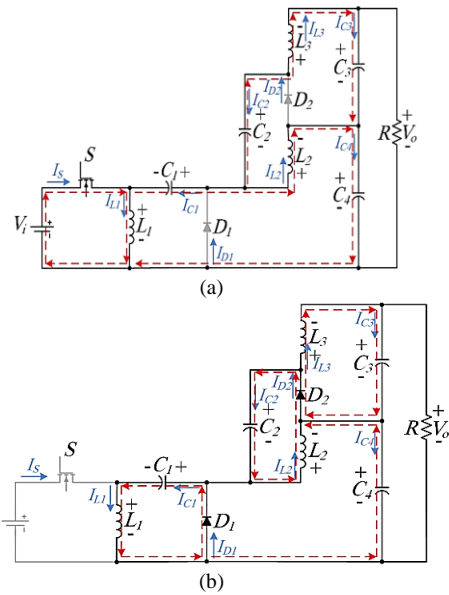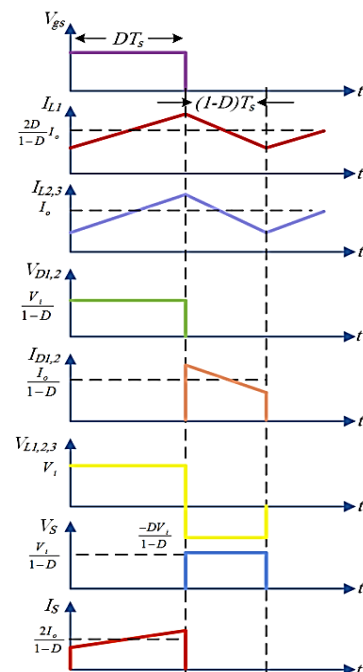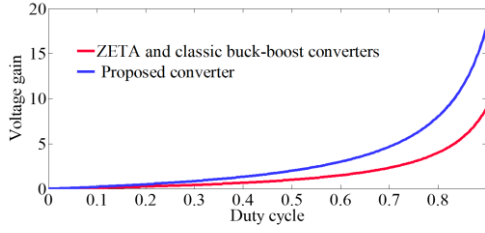**Fig. 1. Circuit topology of the proposed converter**

(a)

(b)

**Fig. 2. Operation modes of the proposed converter
(a) First mode, (b) Second mode**

Fig. 3. Some waveforms of the proposed converter

Fig. 4. Curves of voltage gain comparison of proposed converter and other converters at CCM operation

The voltage gain curves for the proposed converter, ZETA and classic buck-boost converter are shown in Fig. 4. It is seen that the voltage transfer gain of the converter is higher than that of the other converters.

3.2. Calculation of the currents

The capacitor C_3 performs as a low-pass filter, therefore the average current of the capacitors C_1, C_2 and C_4 during state 1 $\left(I_{C1,\text{st}1}, I_{C2,\text{st}1} \text{ and } I_{C4,\text{st}1}\right)$ can be obtained as follows:

$$I_{C1,\text{st}1} = I_{C2,\text{st}1} - I_{L2} \tag{12}$$

$$I_{C2,\text{st}1} = -I_{L3} = -\frac{(2D)V_i}{(1-D)R} \tag{13}$$

$$I_{C4,\text{st}1} = I_{L2} \tag{14}$$

The average current of the capacitor C_4 during state 2 $\left(I_{C4,\text{st}2}\right)$ can be obtained as follows:

$$I_{C4,\text{st}2} = I_{L2} - I_{C2,\text{st}2} \tag{15}$$

Where, $I_{C2,\text{st}2}$ is the average current of the capacitor C_2 during state 2. By applying ampere-second balance principle on the capacitor C_4 to yield:

$$\frac{1}{T_s}\left(\int_0^{DT_s} I_{C4,\text{st}1}dt + \int_{DT_s}^{T_s} I_{C4,\text{st}2}dt\right) = 0 \tag{16}$$

By substituting (14) and (15) into (16), the average current of the capacitors C_1, C_2 and C_4 during state 1 and the inductors L_1, L_2 and L_3 $\left(I_{C1,\text{st}1}, I_{C2,\text{st}1}, I_{C4,\text{st}1}, I_{L1}, I_{L2} \text{ and } I_{L3}\right)$ can be expressed as follows:

$$I_{C1,\text{st}1} = -\frac{(4D)V_i}{(1-D)R} \tag{17}$$

$$I_{C2,\text{st}1} = -I_{L3} = -\frac{(2D)V_i}{(1-D)R} \tag{18}$$

$$I_{C4,\text{st}1} = I_{L2} = \frac{(2D)V_i}{(1-D)R} \tag{19}$$

$$I_{L1} = I_{C1,\text{st}2} = \frac{(4D^2)V_i}{(1-D)^2 R} \tag{20}$$

Table 1. The component normalized voltage and rms current stresses

Circuit parameter	Normalized voltage	Normalized rms current
Switch S	$\dfrac{M_{CCM}+2}{2M_{CCM}}$	$\dfrac{\sqrt{M_{CCM}+2}}{\sqrt{M_{CCM}}}$
Capacitor C_1	$\dfrac{1}{2}$	$\dfrac{\sqrt{2}}{\sqrt{M_{CCM}}}$
Capacitors C_2 and C_4	$\dfrac{1}{2}$	$\dfrac{1}{\sqrt{2M_{CCM}}}$
Capacitor C_3	$\dfrac{1}{2}$	$\dfrac{R}{\sqrt{12}M_{CCM}(M_{CCM}+2)L_3 f_s}$
Diodes D_1 and D_2	$\dfrac{M_{CCM}+2}{2M_{CCM}}$	$\dfrac{\sqrt{M_{CCM}+2}}{M_{CCM}\sqrt{2}}$
Inductor L_1	-	1
Inductors L_2 and L_3	-	$\dfrac{1}{M_{CCM}}$

The current stress of the diodes D_1 and D_2 and the main switch S $\left(I_{D1}, I_{D2} \text{ and } I_S\right)$ can be calculated as follows:

$$I_{D1} = I_{D2} = \frac{(2D)V_i}{(1-D)^2 R} \tag{21}$$

$$I_S = \frac{(4D)V_i}{(1-D)^2 R} \tag{22}$$

The component normalized rms current and voltage stresses for the presented converter in CCM are shown in Table 1.

3.3. Discontinuous conduction mode

There are three modes in Discontinuous conduction mode (DCM). The state 1 in (DCM) is the same as the state 1 in (CCM). In the state 2, the currents of the diodes will decrease. In the state 3, the current of the diodes decreases to zero. In this state, the diodes are turned off. The equivalent circuit is shown in Fig. 5. In this state, the inductors L_1, L_2 and L_3 voltage will be zero.

According to Fig 2(b), the sum of the average currents of the diodes D_1 and D_2 can be earned as follows:

$$I_{D1} + I_{D2} = I_{L1} + I_{L2} + I_{L3} \tag{23}$$

The average of diodes D_1 and D_2 currents $\left(I_{D1,av} \text{ and } I_{D2,av}\right)$ can be achieved as follows:

$$I_{D1,av} = I_{D2,av} = \frac{V_o}{R} \tag{24}$$

According to Fig. 6, the sum of the average of the diodes D_1 and D_2 over one switching period can be earned as follows:

$$I_{D1,av} + I_{D2,av} = \frac{1}{2} \times D_{m2} \times I_{D-PK} \quad (25)$$

Where, D_{m2} is duty cycle in state 2 under DCM and I_{D-PK} is sum of the inductors L_1, L_2 and L_3 peak currents.

$$I_{D-pk} = I_{L1-pk} + I_{L2-pk} + I_{L3-pk} = \frac{V_i D T_s}{L_e} \quad (26)$$

Where,

$$\frac{1}{L_e} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3} \quad (27)$$

By using volt-sec balance on inductors L_1, L_2 and L_3 duty cycle in state 2 under DCM (D_{m2}) can be obtained as follows:

$$D_{m2} = \frac{2DV_i}{V_o} \quad (28)$$

According to (23)-(28), the voltage gain of the converter in discontinuous conduction mode (M_{DCM}) can be achieved as follows:
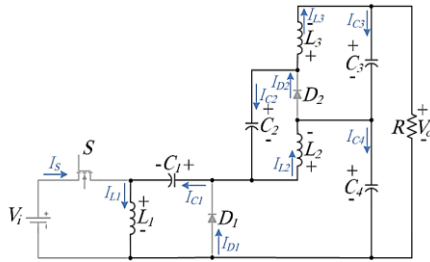
$$M_{DCM} = \frac{D}{\sqrt{\tau_L}} \quad (29)$$

Fig. 5. Equivalent circuits of the presented converter in third mode at DCM operation
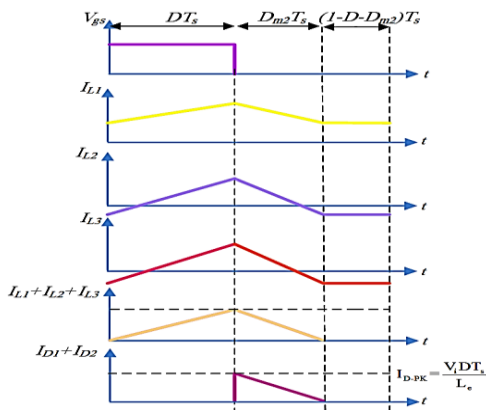

Fig.6. Some illustrated waveforms of the proposed converter at DCM operation
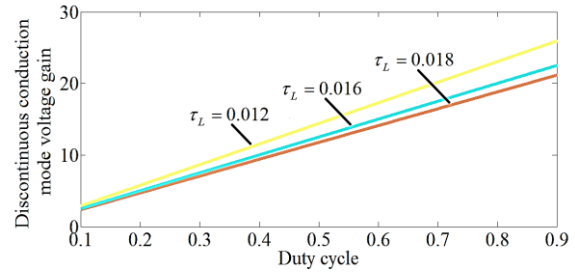

Fig. 7. Discontinuous conduction mode voltage gain versus duty cycle

Where, the normalized inductor time constant τ_L is obtained as follows:

$$\tau_L = \frac{2L_e}{RT_s} \quad (30)$$

Fig. 7. shows the DCM voltage gain of the proposed converter versus duty cycle by different τ_L.

3.4. Boundary condition mode

When the proposed converter is operated in boundary conduction mode (BCM) operation, the voltage gain in CCM is equal to DCM. Combing (11) and (29), the boundary normalized inductor time constant (τ_b) is:

$$\tau_b = \frac{(1-D)^2}{4} \quad (31)$$

Fig. 8. shows the boundary normalized inductor time constant curve (τ_b). When τ_L is larger than τ_b, the presented buck-boost converter operates in CCM.

The boundary normalized inductor time constant curves for the proposed and the ZETA and classic buck-boost converters are shown in Fig. 9.
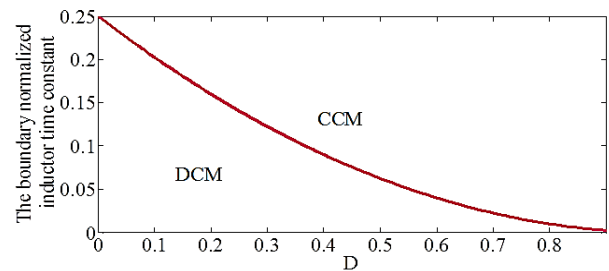

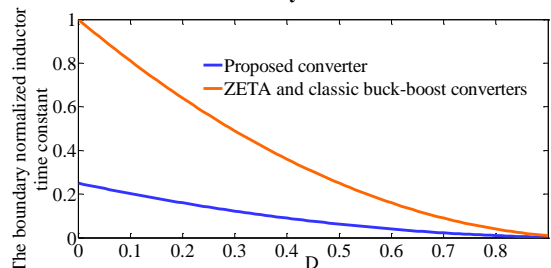**Fig. 8. Boundary normalized inductor time constant versus duty cycle**

Fig. 9. Curves of boundary inductor time constant comparison of proposed converter and other converters

3.5. Efficiency analysis

For efficiency analysis of the presented buck-boost converter, parasitic resistances are defined as follows: switch on-state resistances is r_{DS} , forward resistances of the diodes D_1 and D_2 are R_{F1} and R_{F2} respectively, V_{F1} and V_{F2} are the threshold voltages of the diodes D_1 and D_2 respectively, inductors L_1 , L_2 and L_3 equivalent series resistances (ESR) are R_{L1} , R_{L2} and R_{L3} respectively, the capacitors C_1 , C_2 , C_3 and C_4 ESR are r_{C1} , r_{C2} , r_{C3} and r_{C4} respectively and the voltage ripple of the capacitors and the inductors is ignored.

The condition loss of the switch S $\left(P_{rDS}\right)$ can be obtained as follows:

$$P_{rDS} = r_{DS} I_{S,rms}{}^2 = r_{DS}\frac{4D}{(1-D)^2}I_o{}^2 \tag{32}$$

The proposed converter switching loss $\left(P_{Sw}\right)$ can be achieved as follows:

$$P_{Sw} = f_s C_S V_S{}^2 = f_s C_S \left(\frac{V_i}{1-D}\right)^2 \tag{33}$$

The total losses of the switch S $\left(P_{Switch}\right)$ can be achieved as follows:

$$P_{Switch} = P_{rDS} + \frac{P_{Sw}}{2} \tag{34}$$

The losses of the diodes D_1 and D_2 $\left(P_{D1,2}\right)$ can be obtained as follows:

$$P_{D1,2} = R_{F1,2}\frac{1}{1-D}I_o{}^2 + V_{F1,2}I_o \tag{35}$$

The losses of capacitors C_1 , C_2 , C_3 and C_4 $\left(P_{C1,2,3,4}\right)$ can be derived as:

$$P_{C1,2,3,4} = r_{C1}\frac{4DP_o}{(1-D)R} + r_{C2,4}\frac{DP_o}{(1-D)R} + r_{C3}\frac{(1-D)^2 RP_o}{48L_3{}^2 f_s{}^2} \tag{36}$$

The losses of inductors L_1 , L_2 and L_3 $\left(P_{L1,2,3}\right)$ can be achieved as follows:

$$P_{L1,2,3} = R_{L1}\left(\frac{2D}{1-D}\right)^2 \frac{P_o}{R} + R_{L2,3}\frac{P_o}{R} \tag{37}$$

The total loss of the proposed converter $\left(P_{Loss}\right)$ can be expressed as follows:

$$P_{Loss} = P_{Switch} + \sum_{u=1}^{2}(P_{RF})_{Du} + \sum_{u=1}^{2}(P_{VF})_{Du} + \sum_{u=1}^{4}P_{RCu} + P_{rL1} + P_{rL2} + P_{rL3} \tag{38}$$

The efficiency of the proposed converter $\left(\eta\right)$ can be

achieved as follows:

$$\eta = \frac{P_O}{P_O + P_{Loss}} = \frac{1}{1+\dfrac{P_{Loss}}{P_O}} \tag{39}$$

According to above equations, the proposed converter efficiency can be obtained as follows:

$$\eta = \frac{1}{1+\dfrac{A_1}{R(1-D)^2}+r_{C3}\dfrac{(1-D)^2 R}{48Lf_s{}^2}+\dfrac{f_s C_s V_i{}^2}{2(1-D)^2 R I_o{}^2}} \tag{40}$$

Where,

$$A_1 = 4Dr_{DS} + (1-D)(R_{F1}+R_{F2}) + \frac{(1-D)^2}{I_o}(V_{F1}+V_{F2}) +$$
$$4D(1-D)r_{C1} + D(1-D)(r_{C2}+r_{C4}) + 4D^2 R_{L1} \tag{41}$$
$$+(1-D)^2(R_{L2}+R_{L3})$$

3.6. Voltage stress

The voltage stress of the converter is an important parameter in the circuits. The voltage stress of the diodes and switch can be achieved as follows:

$$V_S = \frac{V_i}{1-D} \tag{42}$$

$$V_{D1} = V_{D2} = \frac{V_i}{1-D} \tag{43}$$

From Eq. (42) and Eq. (43), the voltage stresses of the diodes and switch are smaller than the output voltage. The comparison of the normalized voltage stress of the switch for the proposed converter and ZETA and classic buck-boost converters is shown in Fig. 10. The normalized voltage stress of the ZETA converter is higher than the presented converter therefore; the switch with low conduction loss can be selected.

Table 2 shows the comparison among the voltage and current stresses, efficiency, voltage gain and the number of elements of the converters. According to Table 2, the voltage gain of the proposed converter is higher than other converters comparing to the number of elements. The normalized voltage stress of the proposed converter is less than other converters and the structure of the converter is simple. The switch number of the proposed converter is less than that in the other converters.

As shown in Table 2, the proposed converter has much wider operating range than other converters and in this converter, only one power switch is used, but the costs of the extra switches of the converter in [18] and converter in [19] are high and control of the switches of the converters is complex. The total device of the other converters is higher comparing to their gains and

voltage stresses. Based on the low voltage stress of the proposed converter, the efficiency of the proposed converter is higher comparing to its gain.
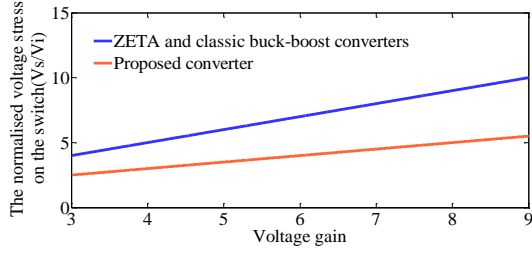

Fig. 10. Normalized switch voltage stress of the proposed converter versus voltage gain

Table 2. Comparison between proposed converter and other structures

	Proposed converter	Converter in [18]			ZETA converter	KY converter in [19]
Quantities of switches	1	3			1	2
Quantities of diodes	2	3			1	1
Quantities of capacitors	4	1			2	3
Quantities of inductors	3	2			2	2
Total device count	10	10			6	8
Voltage stress of the switch	$\dfrac{V_o + 2V_i}{2V_i}$	1	$\dfrac{V_o}{V_i}$	$\dfrac{V_o}{V_i}$	$\dfrac{V_o + V_i}{V_i}$	$\dfrac{V_o}{V_i}$
Voltage gain	$\dfrac{2D}{1-D}$	$\dfrac{2D}{1-D}$			$\dfrac{D}{1-D}$	$2D$
$V_{Diode(Max)}/V_o$	$\dfrac{1}{2D}$	1			$\dfrac{1}{D}$	$\dfrac{1}{2}$
Average current of the diode	I_o	$I_o(1-2D)$	$\dfrac{I_o}{2}(1-D)$		I_o	I_o
Maximum efficiency	97.2 %	90.2 %			92.8 %	94.8 %

3.7. Calculation of the voltage ripple of the capacitors

According to Fig. 11, the capacitor C_1 voltage ripple called ΔV_{C1}, $\Delta V_{C1,ESR}$ is created from the voltage ripple composed from the current of the equivalent series resistance of the capacitor C_1 and the voltage ripple created from the charging and discharging of the capacitor C_1 is denoted by $\Delta V_{C1,cap}$. Figs. 11-12. show the voltage and current of the capacitors C_2 and C_4. Therefore, the voltage ripple of the capacitor C_1 can be obtained as follows:

$$\Delta V_{C1} = \Delta V_{C1,ESR} + \Delta V_{C1,cap} \qquad (44)$$

$\Delta V_{C1,ESR}$ can be achieved as follows:

$$\Delta V_{C1,ESR} = ESR_{C1}\Delta I_{C1} \simeq ESR_{C1}(I_{C1,on} - I_{C1,off}) = \frac{ESR_{C1}(4D)V_i}{(1-D)^2 R} \qquad (45)$$
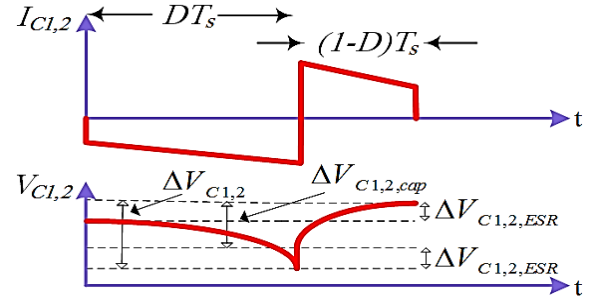

Fig. 11. The current and voltage of the capacitors C_1 and C_2
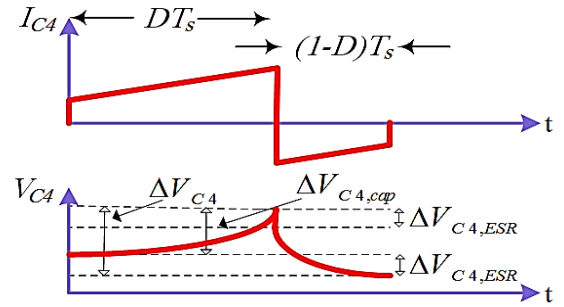

Fig. 12. The current and voltage of the capacitor C_4

Where,

$$ESR_{C1} = \frac{\tan \delta_{C1}}{2\pi f_s} \qquad (46)$$

Where, $\tan \delta_{C1}$ is the dissipation factor of capacitor C_1. $\Delta V_{C1,cap}$ can be obtained as follows:

$$\Delta V_{C1,cap} = \frac{I_{C1,on}DT_s}{C_1} = \frac{2DT_s V_o}{RC_1} \qquad (47)$$

Similarly, the voltage ripple of the capacitors C_2 and C_4 $\left(\Delta V_{C2,4}\right)$ can be expressed as follows:

$$\Delta V_{C2,4} = \Delta V_{C2,4,ESR} + \Delta V_{C2,4,cap} = \frac{ESR_{C2,4}(2D)V_i}{(1-D)^2 R} + \frac{DT_s V_o}{RC_{2,4}} \qquad (48)$$

3.8. Capacitors and inductors design

The theoretical value of the inductors L_1, L_2 and L_3 to work in CCM can be derived as follows:

$$L_1 \geq \frac{V_o(1-D)^2}{8DI_o f_s} = \frac{92 \times (1-0.65)^2}{8 \times 0.65 \times 2.2 \times 43 \times 10^3} = 22\mu H \qquad (49)$$

$$L_{2,3} \geq \frac{V_o(1-D)}{4I_o f_s} = \frac{92 \times (1-0.65)}{4 \times 2.2 \times 43000} = 85\mu H \qquad (50)$$

The theoretical value of the capacitors C_1, C_2, C_3 and C_4 can be achieved as follows:

$$C_1 \ge \frac{2DT_s V_o}{R\Delta V_{C1}} = \frac{2DV_o}{R\times 0.01 \times V_o \times f_s} =$$

$$\frac{2\times 0.65 \times 92}{42\times 0.01 \times 92 \times 43000} = 71.9\mu F \qquad (51)$$

$$C_{2,4} \ge \frac{DT_s V_o}{R\Delta V_{C2,4}} = \frac{DV_o}{R\times 0.01 \times V_o \times f_s} =$$

$$\frac{0.65 \times 92}{42\times 0.01 \times 92 \times 43000} = 35.9\mu F \qquad (52)$$

$$C_3 \ge \frac{V_o(1-D)}{16 L_3 f_s^2 \Delta V_{C3}} = \frac{92\times(1-0.65)}{16\times 315\times 10^{-6}\times(43\times 10^3)^2 \times 1} = 3.45\mu F \qquad (53)$$

3.9. Small signal modeling

According to Fig. 2(a), the equations for the state 1 can be achieved as follows:

$$L_1 \frac{di_{L1}}{dt} = V_i \qquad (54)$$

$$L_2 \frac{di_{L2}}{dt} = V_{C1} - V_{C4} + V_i \qquad (55)$$

$$L_3 \frac{di_{L3}}{dt} = V_{C1} + V_{C2} + V_i - V_{C3} - V_{C4} \qquad (56)$$

$$C_1 \frac{dV_{C1}}{dt} = -i_{L2} - i_{L3} \qquad (57)$$

$$C_2 \frac{dV_{C2}}{dt} = -i_{L3} \qquad (58)$$

$$C_3 \frac{dV_{C3}}{dt} = i_{L3} - \frac{V_{C3} + V_{C4}}{R} \qquad (59)$$

$$C_4 \frac{dV_{C4}}{dt} = i_{L2} + i_{L3} - \frac{V_{C3} + V_{C4}}{R} \qquad (60)$$

According to Fig 2(b), the equations for the state 2 can be expressed as follows:

$$L_1 \frac{di_{L1}}{dt} = -V_{C1} \qquad (61)$$

$$L_2 \frac{di_{L2}}{dt} = -V_{C2} \qquad (62)$$

$$L_3 \frac{di_{L3}}{dt} = -V_{C3} \qquad (63)$$

$$C_1 \frac{dV_{C1}}{dt} = i_{L1} \qquad (64)$$

$$C_2 \frac{dV_{C2}}{dt} = -\frac{1}{1-d}\frac{V_{C3} + V_{C4}}{R} + \frac{1}{1-d}i_{L2} + \frac{d}{1-d}i_{L3} \qquad (65)$$

$$C_3 \frac{dV_{C3}}{dt} = i_{L3} - \frac{V_{C3} + V_{C4}}{R} \qquad (66)$$

$$C_4 \frac{dV_{C4}}{dt} = i_{L2} - \frac{d}{1-d}i_{L3} - \frac{V_{C3} + V_{C4}}{R} \qquad (67)$$

According to the average method and using equations (54)-(67), the average model for the proposed converter can be achieved as follows:

$$L_1 \frac{d\langle i_{L1}\rangle}{dt} = d\langle V_i \rangle - (1-d)\langle V_{C1}\rangle \qquad (68)$$

$$L_2 \frac{d\langle i_{L2}\rangle}{dt} = d\langle V_{C1}\rangle - d\langle V_{C4}\rangle + d\langle V_i \rangle - (1-d)\langle V_{C2}\rangle \qquad (69)$$

$$L_3 \frac{d\langle i_{L3}\rangle}{dt} = d\langle V_{C1}\rangle + d\langle V_{C2}\rangle + d\langle V_i \rangle - \langle V_{C3}\rangle - d\langle V_{C4}\rangle \qquad (70)$$

$$C_1 \frac{d\langle V_{C1}\rangle}{dt} = -d\langle i_{L2}\rangle - d\langle i_{L3}\rangle + (1-d)\langle i_{L1}\rangle \qquad (71)$$

$$C_2 \frac{d\langle V_{C2}\rangle}{dt} = \langle i_{L2}\rangle - \frac{\langle V_{C3}\rangle + \langle V_{C4}\rangle}{R} \qquad (72)$$

$$C_3 \frac{d\langle V_{C3}\rangle}{dt} = \langle i_{L3}\rangle - \frac{\langle V_{C3}\rangle + \langle V_{C4}\rangle}{R} \qquad (73)$$

$$C_4 \frac{d\langle V_{C4}\rangle}{dt} = \langle i_{L2}\rangle - \frac{\langle V_{C3}\rangle + \langle V_{C4}\rangle}{R} \qquad (74)$$

where $\langle i_{L1}\rangle$, $\langle i_{L2}\rangle$, $\langle i_{L3}\rangle$, $\langle V_{C1}\rangle$, $\langle V_{C2}\rangle$, $\langle V_{C3}\rangle$, $\langle V_{C4}\rangle$ and $\langle V_i\rangle$ are the average values of i_{L1}, i_{L2}, i_{L3}, V_{C1}, V_{C2}, V_{C3}, V_{C4} and V_i respectively, and d is the duty cycle.

For obtaining the small-signal model, small AC values of the mentioned elements are defined as:

$\hat{i}_{L1}$, $\hat{i}_{L2}$, $\hat{i}_{L3}$, $\hat{V}_{C1}$, $\hat{V}_{C2}$, $\hat{V}_{C3}$, $\hat{V}_{C4}$, $\hat{V}_i$ and $\hat{d}$. In addition, the relationship among DC values, AC values and average values can be earned as follows:

$$\langle V_i \rangle = V_i + \hat{V}_i \qquad \text{and} \quad \hat{V}_i \ll V_i \qquad (75)$$

$$\langle d \rangle = d + \hat{d} \qquad \text{and} \quad \hat{d} \ll d \qquad (76)$$

$$\langle i_{L1}\rangle = i_{L1} + \hat{i}_{L1} \qquad \text{and} \quad \hat{i}_{L1} \ll i_{L1} \qquad (77)$$

$$\langle i_{L2}\rangle = i_{L2} + \hat{i}_{L2} \qquad \text{and} \quad \hat{i}_{L2} \ll i_{L2} \qquad (78)$$

$$\langle i_{L3}\rangle = i_{L3} + \hat{i}_{L3} \qquad \text{and} \quad \hat{i}_{L3} \ll i_{L3} \qquad (79)$$

$$\langle V_{C1}\rangle = V_{C1} + \hat{V}_{C1} \quad \text{and} \quad \hat{V}_{C1} \ll V_{C1} \qquad (80)$$

$$\langle V_{C2}\rangle = V_{C2} + \hat{V}_{C2} \quad \text{and} \quad \hat{V}_{C2} \ll V_{C2} \qquad (81)$$

$$\langle V_{C3}\rangle = V_{C3} + \hat{V}_{C3} \quad \text{and} \quad \hat{V}_{C3} \ll V_{C3} \qquad (82)$$

$$\langle V_{C4}\rangle = V_{C4} + \hat{V}_{C4} \quad \text{and} \quad \hat{V}_{C4} \ll V_{C4} \qquad (83)$$

By substituting (75)-(83) into (68)-(74), extracting the DC and AC values and omitting the higher order small signal terms we have:

$$L_1 \frac{d\hat{i}_{L1}}{dt} = d\hat{V}_i + \hat{d}(V_{C1} + V_i) - (1-d)\hat{V}_{C1} \qquad (84)$$

$$L_2 \frac{d\hat{i}_{L2}}{dt} = d\hat{V}_{C1} - d\hat{V}_{C4} + \hat{d}(V_{C1} - V_{C4} + V_i + V_{C2}) + d\hat{V}_i - (1-d)\hat{V}_{C2} \qquad (85)$$

$$L_3 \frac{d\hat{i}_{L3}}{dt} = dV̂_{C1} + dV̂_{C2} - V̂_{C3} - dV̂_{C4} + \quad (86)$$

$$\hat{d}(V_{C1} - V_{C4} + V_i + V_{C2}) + dV̂_i$$

$$C_1 \frac{dV̂_{C1}}{dt} = -d\hat{i}_{L2} + \hat{d}(-i_{L1} - i_{L2} - i_{L3}) - d\hat{i}_{L3} + (1-d)\hat{i}_{L_1} \quad (87)$$

$$C_2 \frac{dV̂_{C2}}{dt} = \hat{i}_{L2} - \frac{V̂_{C3} + V̂_{C4}}{R} \quad (88)$$

$$C_3 \frac{dV̂_{C3}}{dt} = \hat{i}_{L3} - \frac{V̂_{C3} + V̂_{C4}}{R} \quad (89)$$

$$C_4 \frac{dV̂_{C4}}{dt} = \hat{i}_{L2} - \frac{V̂_{C3} + V̂_{C4}}{R} \quad (90)$$

From equations (84)-(90), the state-space form of the equations can be achieved as follows:

$$K\dot{x} = Ax + Bu \quad (91)$$
$$y = Cx + Eu \quad (92)$$

with

$$x = \begin{bmatrix} \hat{i}_{L1} & \hat{i}_{L2} & \hat{i}_{L3} & V̂_{C1} & V̂_{C2} & V̂_{C3} & V̂_{C4} \end{bmatrix}^T \quad (93)$$

$$u = \begin{bmatrix} \hat{d} & V̂_i \end{bmatrix}^T \quad (94)$$

$$K = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_3 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & C_4 \end{bmatrix} \quad (95)$$

$$A = \begin{bmatrix} 0 & 0 & 0 & -(1-d) & 0 & 0 & 0 \\ 0 & 0 & 0 & d & -(1-d) & 0 & -d \\ 0 & 0 & 0 & d & d & -1 & -d \\ (1-d) & -d & -d & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -\frac{1}{R} & -\frac{1}{R} \\ 0 & 0 & 1 & 0 & 0 & -\frac{1}{R} & -\frac{1}{R} \\ 0 & 1 & 0 & 0 & 0 & -\frac{1}{R} & -\frac{1}{R} \end{bmatrix} \quad (96)$$

$$B = \begin{bmatrix} V_i + V_{C1} & d \\ V_i - V_{C4} + V_{C1} + V_{C2} & d \\ V_{C1} + V_{C2} + V_i - V_{C4} & d \\ -i_{L1} - i_{L2} - i_{L3} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad (97)$$

The matrices for the output equation (**y**) can be obtained as follows:

$$V_o = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{i}_{L3} \\ V̂_{C1} \\ V̂_{C2} \\ V̂_{C3} \\ V̂_{C4} \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{d} \\ V̂_i \end{bmatrix} \quad (98)$$

4. EXPERIMENTAL RESULTS

In order to verify the performance of the presented converter, experimental results are provided. A prototype of the proposed converter is built as shown in Fig. 13.

The proposed converter utilized components are as follows:

1) Input voltage : 25 V
2) Switching frequency: 43 kHz
3) switch: IRFP460A
4) switch on-state resistance: 0.03 ohm
5) diodes D_1 and D_2 : MUR860
6) diodes D_1 and D_2 forward resistances: 0.02 ohm
7) diodes D_1 and D_2 threshold voltages: 0.7 V
8) inductor L_1 : 150 μH
9) inductors L_2 and L_3 : 315 μH
10) the equivalent series resistances (ESR) of inductor L_1 :0.01 ohm
11) the equivalent series resistances (ESR) of inductors L_2 and L_3 :0.018 ohm
12) capacitors C_2 , C_3 and C_4 : 100 μF
13) capacitor C_1 : 470 μF
14) the equivalent series resistances (ESR)of capacitors C_2 , C_3 and C_4 : 0.012 ohm
15) the equivalent series resistances (ESR)of capacitor C_1 : 0.023 ohm

The output voltage is shown in Fig. 14(a). The output voltage is 92 V and the output power is 200 W. Figs. 14(b), 14(c) and 14(d) show the waveform of the inductors currents of L_1 , L_2 and L_3 respectively. According to Eqns. (18)-(20), the average of inductors currents of L_1 , L_2 and L_3 are 8.1, 2.2 and 2.2 A respectively. The diode D_2 voltage waveform is similar to diode D_1 voltage waveform. The voltage on the diodes D_1 and D_2 is given in Fig. 14(e). According to Eq. (43), the voltage across the diodes D_1 and D_2 is equal to 71 V. The voltage on the switch

S is shown in Fig. 14(f). According to (42), the switch S voltage is 71 V. The voltage of inductors L_1, L_2 and L_3 is shown in Fig. 14(g). The voltage of inductors L_1, L_2 and L_3 during state 1 is 25 V and during state 2 is equal to -46 V. Fig. 14(h) shows the waveform of the diodes currents of D_1 and D_2. According to (21), the average of diodes currents of D_1 and D_2 is 6.25 A. Fig. 14(i) shows the waveform of the switch S current. According to (22), the average of switch S current is 12.5 A.

The conventional ZETA converter used components are as follows:

1) input voltage : 25 V

2) switching frequency: 43 kHz

3) switch on-state resistance: 0.03 ohm

4) diode D_1 forward resistance: 0.02 ohm

5) diode D_1 threshold voltage: 0.7 V

6) inductor L_1 : 150 µH

7) inductor L_2 : 315 µH

8) the equivalent series resistances (ESR) of inductor L_1 :0.01 ohm

9) the equivalent series resistances (ESR) of inductor L_2 :0.018 ohm

10) capacitor C_1 : 100 µF

11) capacitor C_2 : 470 µF

12) the equivalent series resistances (ESR)of capacitor C_1: 0.023 ohm

13) the equivalent series resistances (ESR)of capacitor C_2 : 0.012 ohm

Fig. 15 shows the theoretical and experimental voltage transfer gains of the proposed converter. Fig. 16 shows the efficiency curves of converters with different output power. It is seen that the efficiency of proposed converter is higher than that of ZETA converter. Fig. 17. shows the curve of efficiency of the proposed converter versus output power. It is seen that the theoretical efficiency is higher than the experimental efficiency. Fig. 18 shows the efficiency curves of converters with different output power. It is seen that the efficiency of proposed converter is higher than that of the converter in Ref. [18] and converter II in Ref. [25].
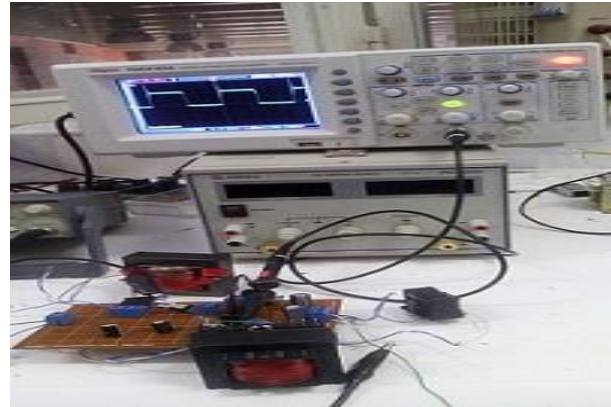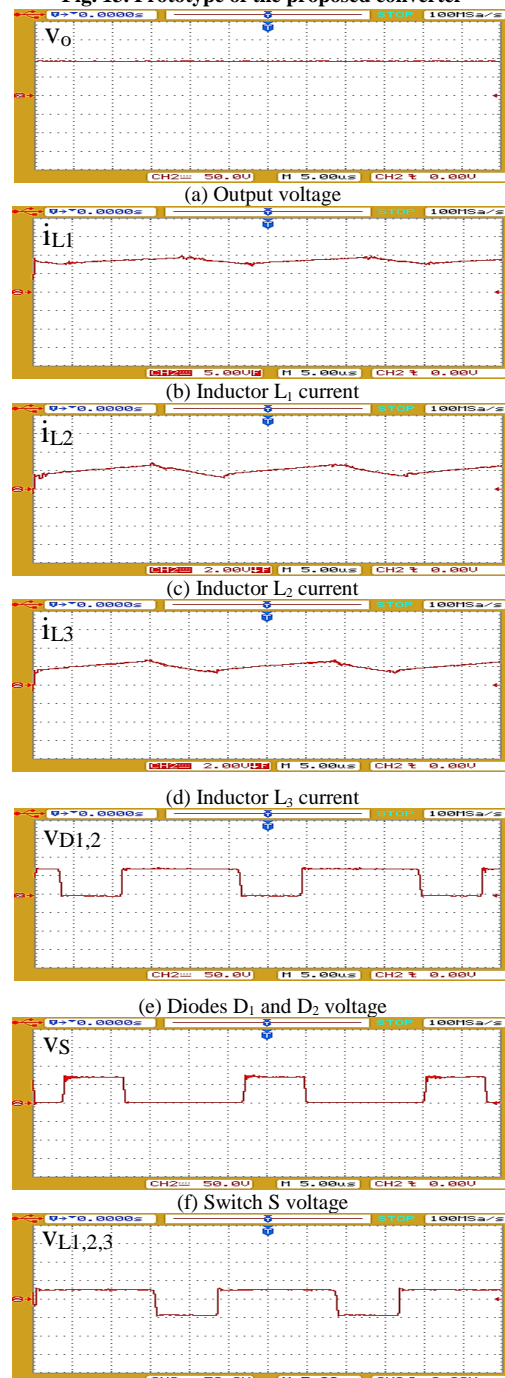

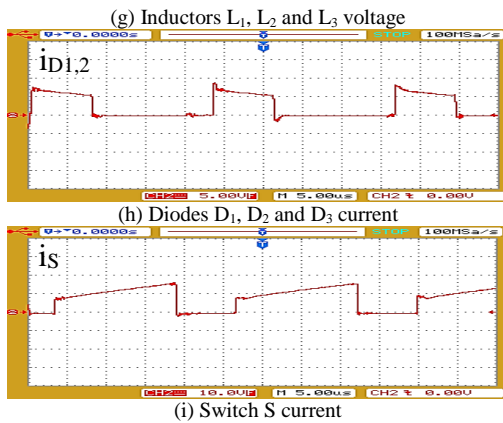Fig. 13. Prototype of the proposed converter

(a) Output voltage

(b) Inductor L_1 current

(c) Inductor L_2 current

(d) Inductor L_3 current

(e) Diodes D_1 and D_2 voltage

(f) Switch S voltage

(g) Inductors L_1, L_2 and L_3 voltage

(h) Diodes D_1, D_2 and D_3 current

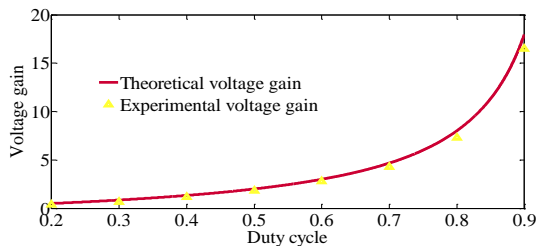(i) Switch S current

Fig. 14. Experimental results

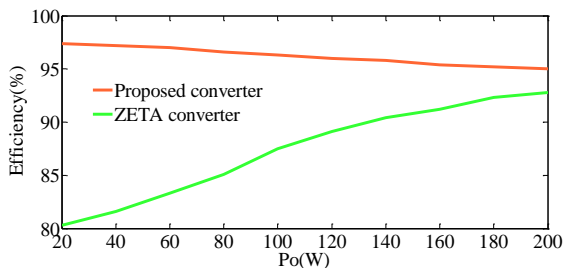**Fig. 15. Theoretical and experimental voltage gains of the proposed converter**

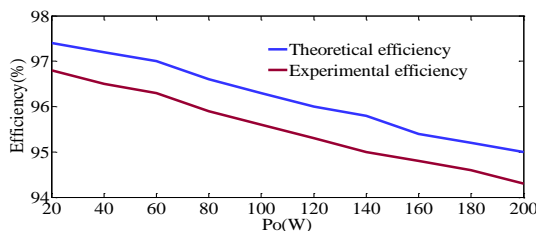**Fig. 16. Measured efficiency of the converters versus output power**

Fig. 17. Measured efficiency of the presented converter versus output power
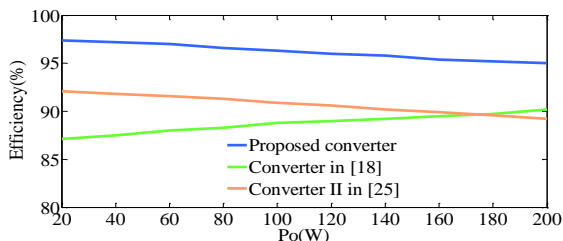

Fig. 18. Measured efficiency of the proposed converter and other converters versus output power

5. CONCLUSIONS

In this paper, a novel transformerless buck boost converter based on ZETA converter is presented. In this converter, only one main switch is used, which decreases the losses and improves efficiency. The active switch voltage stress is low and switch with low on-state resistance can be utilized. The voltage gain of the converter is higher than that of the classic boost, buck-boost, ZETA, CUK and SEPIC converters. The presented converter structure is simple; hence, the converter control is simple. The buck-boost converters are used in some applications such as fuel-cell, car electronic devices, and LED drivers. Finally, the experimental results are given to verify the proposed converter.

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