Analysis and Design of a New Single Switch Non-Isolated Buck-Boost DC-DC Converter

M. R. Banaei†, H. Ajdar Faeghi Bonab, N. Taghizadegan Kalantari
Department of Electrical Engineering, Azarbaijan Shahid Madani University, Tabriz, Iran
Research Institute of Applied Power System Studies, Azarbaijan Shahid Madani University, Tabriz, Iran

Abstract - In this paper, a new transformerless buck-boost converter based on ZETA converter is introduced. The proposed converter has the ZETA converter advantages such as, buck-boost capability and input to output DC insulation. The suggested converter voltage gain is higher than the classic ZETA converter. In the presented converter, only one main switch is utilized. The proposed converter offers low voltage stress of the switch; therefore, the low on-state resistance of the main switch can be selected to decrease losses of the switch. The presented converter topology is simple; hence, the control of the converter is simple. The mathematical analyses of the proposed converter are given. The experimental results confirm the correctness of the analysis.

Keyword: Transformerless buck-boost converter, voltage gain, main switch, voltage stress.

1. INTRODUCTION
Fossil fuels are vital sources and these fuels are utilized widely in recent years. Fossil fuels have produced many problems such as air pollution, climate change, global warming problems, and other similar troubles to the environment. Renewable energy systems have been distinguished as the best alternative to fossil fuels [1-3]. Fuel cell and Photovoltaic (PV) are the two main renewable energy sources. However, the voltage of these systems is too low and unstable to be connected to the utility grid. Hence, high voltage converters should be used to increase the DC voltage of the fuel cell and PV into the DC voltage. The classic boost converter could be a suitable choice, owing to static voltage gain and simple structure [4]. A classic boost converter can be utilized to create high step-up voltage gain with high duty cycle. However, this converter has some disadvantage such as high switching losses, diode reverse-recovery problem, and electromagnetic interference (EMI) problem. In addition, the stresses of the switch and the diode of the classic boost converter are high. Hence, the high voltage rated switch should be used and the conduction and switching losses will be increased. The maximum of the voltage gain of the classic boost cannot be more than five [5-9]. The quadratic boost converter is high voltage gain converter, which has only one main switch. The voltage gain of the converter is a quadratic function of a classic boost converter. The switch stress of the converter is equal to the output voltage. Hence, switch with high current can be selected [10-11]. Converters with the coupled inductor are good choices for achieving high voltage by adjusting the coupled inductor turns ratio. However, the coupled inductor leakage inductance makes high voltage stress of the switch and conduction loss. The switched-capacitor technique can be used for earning high voltage. However, in these converters, many switches are utilized, which cause high losses. Some advantages of these converters are the low input ripple, high voltage gain, and low voltage stress of the switch [12-13]. In Ref. [14], a high voltage gain transformerless converter based on the switched inductor and capacitor and active network is proposed. This converter has two switches, which cause high conduction losses. The converter provides high voltage gain with low voltage stress. In Ref. [15], a transformerless converter with very high step-down voltage gain is proposed. In this converter, five power switches are utilized, which cause high switching and conduction losses. The voltage gain of the converter is three times lower compared to the voltage gain of the classic buck converter. In Ref. [16], a transformerless converter based on diode-capacitor cell is proposed. The converter has some advantages such as high voltage gain, low diodes and switches.
stresses, low ripple, and high efficiency. In Ref. [17], high step-up transformerless converters are proposed. In these converters one main switch is used. In Ref. [18], a transformerless buck-boost converter is proposed. This converter has three main switches. In this converter, the voltage stress of the switch is equal to the output voltage. The converter conduction and switching losses are high. In Ref. [19], a buck-boost converter combining KY and the classic buck converter is proposed. In this converter two switches are used. Hence, the conduction and switching losses will be high. In Ref. [20], a transformerless buck-boost converter with high voltage gain is proposed. The voltage gain of the converter is squared times of the classic buck-boost converter. The stress of the switch and the diode is high. Hence, the losses of the converter will be high. In Ref. [21], a multi phase transformerless dc-dc converter with high voltage gain is proposed. The voltage stress of the converter is low. Hence, the losses can be reduced. In Ref. [22], a high step-down transformerless converter is suggested. In this converter, four switches are used. The voltage stress of the elements of the converter is high. Hence, the efficiency will be low. In Ref. [23], a DC-DC converter based on ZETA and Buck-Boost converters is presented. This converter has two-output. In the converter, one switch is used and converter has low number of components. In Ref. [24], a bidirectional dc-dc converter based on ZETA converter is proposed. This converter has high conversion ratio and the leakage-inductor energy can be recycled; therefore, the switch stress will be low. In Ref. [25], transformerless high step-up dc-dc converters are proposed. In Ref. [26], a high voltage gain converter is presented. In this converter, the switched inductor and three level converters are used. The converter has two switches; hence the conduction losses of the converter will be high. In Ref. [27], a high step-up converter is proposed. In this converter, active clamp circuit is used; therefore the voltage stress of the switch can be reduced. In Ref. [28] a high step-up transformerless converter is proposed. In this converter, two switches are used and the switched-inductor and switched-capacitor are utilized. In the converter, the output current is continuous. In Ref. [29] a buck-boost converter is suggested. The advantages of the converter are high voltage gain and positive output voltage. The converter has two switches and the voltage stresses of the switches are high and therefore, the losses of the converter will be high. In Ref. [30] a transformerless high step-up DC-DC converter based on the Cockcroft-Walton Voltage Multiplier is proposed. This converter employs two main switches and the diodes and switches stresses are high. In Ref. [31] a high step-up interleaved converter is presented. In this converter, the interleaved boost converter and the voltage-double module are used and the converter has two main switches and the stresses of the diodes of the converter are high. In Ref. [32] a high step-up converter with the coupled inductor is proposed. This converter has one main switch and the stress across the main switch is reduced. However, the voltage stresses of the three diodes of the converter are high. In this converter, the leakage inductance energy can be recycled. In Ref. [33] a transformerless buck-boost converter is suggested. In this converter, one main switch is used. The switch voltage stress of the converter is high and therefore, the converter switch loss will be high. In references [34-37] high voltage gain transformerless converters are proposed. In this paper, a novel transformerless boost converter based on ZETA converter is proposed. The converter voltage gain is higher than the classic buck-boost converter, ZETA, CUK, and SEPIC converters. The proposed converter topology is very simple; hence, the converter control is simple. This converter has one main switch. The main switch and diodes stresses are less than the output voltage, hence the switch loss will be low and the converter efficiency can be improved. The buck-boost converters are used in some applications like LED drivers, fuel-cell, and car electronic devices. The modes analysis is explained and to confirm the operation of the converter, experimental results are given.

2. OPERATING PRINCIPLE OF THE PROPOSED CONVERTER

Fig. 1 shows the circuit topology of the presented converter. The converter consists one main switch S, two diodes D1 and D2, three inductors L1, L2 and L3, four capacitors C1, C2, C3 and C4 and load R.

To simplify the analysis of the new buck-boost converter, the following conditions were considered:

1) All capacitors are large enough hence; the voltages of the capacitors can be seen as constant.
2) Semiconductor elements such as diodes and switch are ideal.

The proposed converter can be used in the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM). The continuous conduction mode has two operating modes. The analysis of the converter at (CCM) is presented in detail as follows:

1) State 1 [t0,t1] : During this time interval, the switch S is turned ON and the diodes D1 and D2 are
turned OFF. The current-flow path is shown in Fig. 2(a). The inductors \( L_1, L_2 \) and \( L_3 \) are magnetized. The capacitor \( C_1 \) and \( C_2 \) are discharged and the capacitor \( C_4 \) is charged. Thus, the corresponding equations can be achieved as follows:

\[
V_{L_1} = V_i \quad (1)
\]
\[
V_{L_2} = V_{C1} + V_i - V_{C4} \quad (2)
\]
\[
V_{L_3} = V_i + V_{C1} + V_{C2} - V_{C3} - V_{C4} \quad (3)
\]

2) State 2 \([t_1, t_2]\): The current-flow path is shown in Fig. 2(b). During this time interval, switch \( S \) is turned OFF. Diodes \( D_1 \) and \( D_2 \) are turned ON. The inductors \( L_1 \), \( L_2 \) and \( L_3 \) are demagnetized. The capacitor \( C_1 \) is charged by the inductor \( L_1 \) and the capacitor \( C_2 \) is charged by the inductor \( L_2 \). The capacitor \( C_4 \) is discharged. The voltages of inductors are obtained as follows:

\[
V_{L_1} = -V_{C1} \quad (4)
\]
\[
V_{L_2} = -V_{C2} = -V_{C4} \quad (5)
\]
\[
V_{L_3} = -V_{C3} \quad (6)
\]

3. STEADY STATE ANALYSIS OF THE PROPOSED CONVERTER

3.1. Voltage gain

By applying volt-sec balance principle on \( L_1, L_2 \) and \( L_3 \) and using (1)-(6), we have:

\[
\frac{1}{T_s} \int_0^{T_s} (V_i) dt + \int_{t_s} (V_{C1}) dt = 0 \quad (7)
\]
\[
\frac{1}{T_s} \int_0^{T_s} (V_{C1} + V_i - V_{C4}) dt + \int_{t_s} (V_{C4}) dt = 0 \quad (8)
\]
\[
\frac{1}{T_s} \int_0^{T_s} (V_i + V_{C1} + V_{C2} - V_{C3} - V_{C4}) dt + \int_{t_s} (V_{C4}) dt = 0 \quad (9)
\]

By using (5), (7), (8) and (9), the voltage of the capacitors \( C_1, C_2 \) and \( C_3 \) \((V_{C1}, V_{C2}, V_{C3} \) and \( V_{C4} \)) can be achieved as follows:

\[
V_{C1} = V_{C2} = V_{C3} = V_{C4} = \frac{D}{1-D}, \quad (10)
\]

By using (10), the voltage transfer gain \((M_{CCM})\) can be found as follows:

\[
M_{CCM} = \frac{V_o}{V_i} = \frac{2D}{1-D}, \quad (11)
\]

According to (11), it is apparent that the voltage gain of the proposed converter is twice as large as the ZETA converter. Therefore, the voltage gain of the converter is higher than that of ZETA converter. Fig. 3 shows some key waveforms of the proposed converter in (CCM).
Fig. 3. Some waveforms of the proposed converter.

Fig. 4. Curves of voltage gain comparison of proposed converter and other converters at CCM operation.

The voltage gain curves for the proposed converter, ZETA and classic buck-boost converter are shown in Fig. 4. It is seen that the voltage transfer gain of the converter is higher than that of the other converters.

3.2. Calculation of the currents

The capacitor $C_3$ performs as a low-pass filter, therefore the average current of the capacitors $C_1$, $C_2$ and $C_4$ during state 1 ($I_{C_{1,1}}$, $I_{C_{2,1}}$ and $I_{C_{4,1}}$) can be obtained as follows:

$$I_{C_{1,1}} = I_{C_{2,1}} - I_{L_2} \tag{12}$$

$$I_{C_{2,1}} = -I_{L_3} = -\frac{(2DV_2)}{(1-D)R} \tag{13}$$

$$I_{C_{4,1}} = I_{L_2} \tag{14}$$

The average current of the capacitor $C_3$ during state 2 ($I_{C_{4,2}}$) can be obtained as follows:

$$I_{C_{4,2}} = I_{L_2} - I_{C_{2,2}} \tag{15}$$

Where, $I_{C_{2,2}}$ is the average current of the capacitor $C_2$ during state 2. By applying ampere-second balance principle on the capacitor $C_3$ to yield:

$$\frac{1}{T_s} \left( I_{C_{4,2}} \int_{D_f} I_C dt + \int_{D_f} I_{C_{4,2}} dt \right) = 0 \tag{16}$$

By substituting (14) and (15) into (16), the average current of the capacitors $C_1$, $C_2$ and $C_4$ during state 1 and the inductors $L_1$, $L_2$ and $L_3$ ($I_{C_{1,1}}$, $I_{C_{2,1}}$, $I_{C_{4,1}}$, $I_{L_1}$, $I_{L_2}$ and $I_{L_3}$) can be expressed as follows:

$$I_{C_{1,1}} = \frac{(4DV_2)}{(1-D)R} \tag{17}$$

$$I_{C_{2,1}} = -I_{L_3} = \frac{(2DV_2)}{(1-D)R} \tag{18}$$

$$I_{C_{4,1}} = I_{L_2} = \frac{(2DV_2)}{(1-D)R} \tag{19}$$

The current stress of the diodes $D_1$ and $D_2$ and the main switch $S$ ($I_{D_1}$, $I_{D_2}$ and $I_S$) can be calculated as follows:

$$I_{D_1} = I_{D_2} = \frac{(2DV_2)}{(1-D)R} \tag{20}$$

$$I_S = \frac{(4DV_2)}{(1-D)^2R} \tag{21}$$

The component normalized rms current and voltage stresses for the presented converter in CCM are shown in Table 1.

3.3. Discontinuous conduction mode

There are three modes in Discontinuous conduction mode (DCM). The state 1 in (DCM) is the same as the state 1 in (CCM). In the state 2, the currents of the diodes will decrease. In the state 3, the current of the diodes decreases to zero. In this state, the diodes are turned off. The equivalent circuit is shown in Fig. 5. In this state, the inductors $L_4$, $L_5$ and $L_3$ voltage will be zero.

According to Fig 2(b), the sum of the average currents of the diodes $D_1$ and $D_2$ can be earned as follows:

$$I_{D_{1}} + I_{D_{2}} = I_{L_{1}} + I_{L_{2}} + I_{L_{3}} \tag{22}$$

The average of diodes $D_1$ and $D_2$ currents ($I_{D_{1,m}}$ and $I_{D_{2,m}}$) can be achieved as follows:

$$I_{D_{1,m}} = I_{D_{2,m}} = \frac{V_o}{R} \tag{23}$$
According to Fig. 6, the sum of the average of the diodes $D_1$ and $D_2$ over one switching period can be earned as follows:

$$I_{D_{1,av}} + I_{D_{2,av}} = \frac{1}{2} \times D_{m_2} \times I_{D_{pk}}$$  (25)

Where, $D_{m_2}$ is duty cycle in state 2 under DCM and $I_{D_{pk}}$ is sum of the inductors $L_1$, $L_2$ and $L_3$, peak currents.

$$I_{D_{pk}} = I_{D_{1,pk}} + I_{D_{2,pk}} + I_{D_{3,pk}} = \frac{V_i DT_s}{L_s}$$  (26)

Where,

$$\frac{1}{L_s} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}$$  (27)

By using volt-sec balance on inductors $L_1$, $L_2$ and $L_3$, duty cycle in state 2 under DCM ($D_{m_2}$) can be obtained as follows:

$$D_{m_2} = \frac{2DV_i}{V_i}$$  (28)

According to (23)-(28), the voltage gain of the converter in discontinuous conduction mode ($M_{DCM}$) can be achieved as follows:

$$M_{DCM} = \frac{D}{\sqrt{\tau_L}}$$  (29)

Fig. 7. Discontinuous conduction mode voltage gain versus duty cycle

Where, the normalized inductor time constant $\tau_L$ is obtained as follows:

$$\tau_L = \frac{2L_s}{RT_s}$$  (30)

Fig. 7 shows the DCM voltage gain of the proposed converter versus duty cycle by different $\tau_L$.

### 3.4. Boundary condition mode

When the proposed converter is operated in boundary conduction mode (BCM) operation, the voltage gain in CCM is equal to DCM. Combing (11) and (29), the boundary normalized inductor time constant ($\tau_b$) is:

$$\tau_b = \frac{(1-D)^2}{4}$$  (31)

Fig. 8 shows the boundary normalized inductor time constant curve ($\tau_b$). When $\tau_L$ is larger than $\tau_b$, the presented buck-boost converter operates in CCM.

The boundary normalized inductor time constant curves for the proposed and the ZETA and classic buck-boost converters are shown in Fig. 9.
3.5. Efficiency analysis

For efficiency analysis of the presented buck-boost converter, parasitic resistances are defined as follows: switch on-state resistances is $r_{DS}$, forward resistances of the diodes $D_1$ and $D_2$ are $r_{F1}$ and $r_{F2}$ respectively, $V_{F1}$ and $V_{F2}$ are the threshold voltages of the diodes $D_1$ and $D_2$ respectively, inductors $L_1$, $L_2$ and $L_3$ equivalent series resistances (ESR) are $r_{L1}$, $r_{L2}$ and $r_{L3}$ respectively, the capacitors $C_1$, $C_2$, $C_3$ and $C_4$ ESR are $r_{C1}$, $r_{C2}$, $r_{C3}$ and $r_{C4}$ respectively and the voltage ripple of the capacitors and the inductors is ignored.

The condition loss of the switch $S$ ($P_{ds}$) can be obtained as follows:

$$P_{ds} = r_{DS} I_s^2, \text{s, max} = r_{DS} \frac{4D}{(1 - D)} I_o^2 \quad (32)$$

The proposed converter switching loss ($P_{sw}$) can be achieved as follows:

$$P_{sw} = f_s C_s V_s^2 = f_s C_s \left(\frac{V_1}{1 - D}\right)^2 \quad (33)$$

The total losses of the switch $S$ ($P_{switch}$) can be achieved as follows:

$$P_{switch} = P_{ds} + \frac{P_{sw}}{2} \quad (34)$$

The losses of the diodes $D_1$ and $D_2$ ($P_{d1,2}$) can be obtained as follows:

$$P_{d1,2} = \frac{R_{F1,2}}{1 - D} I_o^2 + V_{F1,2} I_o \quad (35)$$

The losses of capacitors $C_1$, $C_2$, $C_3$ and $C_4$ ($P_{c1,2,3,4}$) can be derived as:

$$P_{c1,2,3,4} = r_{c1} \frac{4D P_n}{(1 - D) R} + r_{c2,4} \frac{D P_n}{(1 - D) R} + r_{c3} \frac{(1 - D) R P_n}{48L_s f_s^2} \quad (36)$$

The losses of inductors $L_1$, $L_2$ and $L_3$ ($P_{l1,2,3}$) can be achieved as follows:

$$P_{l1,2,3} = \frac{2D}{1 - D} \frac{V_p}{R} + R_{l1,2,3} \frac{P_n}{R} \quad (37)$$

The total loss of the proposed converter ($P_{loss}$) can be expressed as follows:

$$P_{loss} = \sum_{n=1}^{4} P_{ds,n} + \sum_{n=1}^{4} P_{d1,2} + \sum_{n=1}^{4} P_{c1,2,3,4} + \sum_{n=1}^{4} P_{l1,2,3} \quad (38)$$

The efficiency of the proposed converter ($\eta$) can be achieved as follows:

$$\eta = \frac{P_o}{P_o + P_{loss}} = \frac{1}{1 + \frac{P_{loss}}{P_o}} \quad (39)$$

According to above equations, the proposed converter efficiency can be obtained as follows:

$$\eta = \frac{1}{1 + \frac{A_1}{R(|D - 1|)^2} + \frac{f C V_s^2}{48L_s f_s^2} + \frac{1}{2|D - 1|^2 R I_o^2} + R(|D - 1|)^2 (r_{C1} + r_{C2} + r_{C3} + r_{C4}) + 4D^2 (r_{l1,2,3})} \quad (40)$$

Where,

$$A_1 = 4D r_{DS} + (1 - D)(r_{F1} + r_{F2}) + \frac{(1 - D)^2}{I_o} (V_{F1} + V_{F2}) + 4D^2 (r_{l1,2,3}) + (1 - D)(r_{C1} + r_{C2} + r_{C3} + r_{C4}) + 4D^2 R_{l1,2,3}$$

3.6. Voltage stress

The voltage stress of the converter is an important parameter in the circuits. The voltage stress of the diodes and switch can be achieved as follows:

$$V_s = \frac{V_i}{1 - D} \quad (42)$$

$$V_{D1} = V_{D2} = \frac{V_i}{1 - D} \quad (43)$$

From Eq. (42) and Eq. (43), the voltage stresses of the diodes and switch are smaller than the output voltage. The comparison of the normalized voltage stress of the switch for the proposed converter and ZETA and classic buck-boost converters is shown in Fig. 10. The normalized voltage stress of the ZETA converter is higher than the presented converter therefore; the switch with low conduction loss can be selected.

Table 2 shows the comparison among the voltage and current stresses, efficiency, voltage gain and the number of elements of the converters. According to Table 2, the voltage gain of the proposed converter is higher than other converters comparing to the number of elements. The normalized voltage stress of the proposed converter is less than other converters and the structure of the converter is simple. The switch number of the proposed converter is less than that in the other converters.

As shown in Table 2, the proposed converter has much wider operating range than other converters and in this converter, only one power switch is used, but the costs of the extra switches of the converter in [18] and converter in [19] are high and control of the switches of the converters is complex. The total device of the other converters is higher comparing to their gains and
voltage stresses. Based on the low voltage stress of the proposed converter, the efficiency of the proposed converter is higher comparing to its gain.

\[ \Delta V_{C,ESR} = ESR_C (1 - C_{on}) \Delta V \]

\[ \Delta V_{C,ESR} = \frac{ESR_C (4D V_o)}{(1-D)^2 R} \]

\[ ESR_C = \tan \delta_C \frac{2\pi f}{2} \]

\[ \Delta V_{C,ESR} + \Delta V_{C,ESR,OP} = \frac{ESR_C (4D V_o)}{(1-D)^2 R} + \frac{DT V_o}{RC_1} \]

3.7. Calculation of the voltage ripple of the capacitors

According to Fig. 11, the capacitor \( C_1 \), voltage ripple called \( \Delta V_{C_1} \), \( \Delta V_{C,1,ESR} \) is created from the voltage ripple composed from the current of the equivalent series resistance of the capacitor \( C_1 \) and the voltage ripple created from the charging and discharging of the capacitor \( C_1 \) is denoted by \( \Delta V_{C,1,ESR} \). Figs. 11-12 show the voltage and current of the capacitors \( C_2 \) and \( C_4 \). Therefore, the voltage ripple of the capacitor \( C_1 \) can be obtained as follows:

\[ \Delta V_{C_1} = \Delta V_{C,1,ESR} + \Delta V_{C,1,OP} \]

\[ \Delta V_{C,1,ESR} \] can be achieved as follows:

\[ \Delta V_{C,1,OP} = \frac{I_{C,1} (1-D) T_s}{C_1} \]

Fig. 10. Normalized switch voltage stress of the proposed converter versus voltage gain

Table 2. Comparison between proposed converter and other structures

<table>
<thead>
<tr>
<th>Quantities of switches</th>
<th>Proposed converter</th>
<th>Converter in [18]</th>
<th>ZETA converter</th>
<th>KY converter in [19]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total device count</td>
<td>10</td>
<td>10</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td>Voltage stress of the switch</td>
<td>( \frac{V_o + 2V_i}{2V_i} )</td>
<td>( V_o )</td>
<td>( V_o )</td>
<td>( V_o )</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>( 2D )</td>
<td>( 2D )</td>
<td>( D )</td>
<td>( 2D )</td>
</tr>
<tr>
<td>( V_{D_{total}}/V_i )</td>
<td>( \frac{1}{2D} )</td>
<td>( \frac{1}{1-D} )</td>
<td>( \frac{1}{1-D} )</td>
<td>( \frac{1}{2D} )</td>
</tr>
<tr>
<td>Average current of the diode</td>
<td>( I_s )</td>
<td>( I_s (1-2D) )</td>
<td>( I_s )</td>
<td>( I_s )</td>
</tr>
<tr>
<td>Maximum efficiency</td>
<td>97.2 %</td>
<td>90.2 %</td>
<td>92.8 %</td>
<td>94.8 %</td>
</tr>
</tbody>
</table>

3.8. Capacitors and inductors design

The theoretical value of the inductors \( L_1 \), \( L_2 \) and \( L_3 \) to work in CCM can be derived as follows:

\[ L_1 \geq \frac{V_o (1-D)^2}{8D I f_s} = \frac{92 \times (1-0.65)^2}{8 \times 0.65 \times 2.2 \times 43 \times 10^3} = 22 \mu H \]

\[ L_2,3 \geq \frac{V_o (1-D)}{4I f_s} = \frac{92 \times (1-0.65)}{4 \times 2.2 \times 43000} = 85 \mu H \]
\[
 C_i \geq \frac{2DV}{RAV_{c1}} + \frac{2DV}{RAV_{c2}} = \frac{2DV}{R \times 0.01 \times V_c \times f_i}
\]
\[
 2 \times 0.65 \times 92 
\]
\[
 42 \times 0.01 \times 92 \times 43000 = 71.9 \mu F
\]
\[
 C_{2,*} \geq \frac{4DV}{RAV_{c2}} = \frac{DV}{R \times 0.01 \times V_c \times f_i} = \frac{0.65 \times 92}{42 \times 0.01 \times 92 \times 43000} = 35.9 \mu F
\]
\[
 C_i \geq \frac{V_c \left(1-D\right)}{16L_{f_1}^2AV_{c3}} = \frac{92 \times (1-0.65)}{16 \times 315 \times 10^4 \times (43 \times 10^7)^2} = 3.45 \mu F
\]

### 3.9. Small signal modeling

According to Fig. 2(a), the equations for the state 1 can be achieved as follows:

\[
 L_i \frac{d\hat{i}_{l1}}{dt} = V_i
\]

\[
 L_i \frac{d\hat{i}_{l2}}{dt} = V_{c1} - V_{c4} + V_i
\]

\[
 L_i \frac{d\hat{i}_{l3}}{dt} = V_{c1} + V_{c2} + V_i - V_{c3} - V_{c4}
\]

\[
 C_1 \frac{dV_{c1}}{dt} = -i_{l2} - i_{l3}
\]

\[
 C_2 \frac{dV_{c2}}{dt} = -i_{l3}
\]

\[
 C_3 \frac{dV_{c3}}{dt} = i_{l3} - \frac{V_{c3} + V_{c4}}{R}
\]

\[
 C_4 \frac{dV_{c4}}{dt} = i_{l2} + i_{l3} - \frac{V_{c3} + V_{c4}}{R}
\]

According to Fig 2(b), the equations for the state 2 can be expressed as follows:

\[
 L_i \frac{d\hat{i}_{l1}}{dt} = -V_{c1}
\]

\[
 L_i \frac{d\hat{i}_{l2}}{dt} = -V_{c2}
\]

\[
 L_i \frac{d\hat{i}_{l3}}{dt} = V_{c3}
\]

\[
 C_1 \frac{dV_{c1}}{dt} = i_{l1}
\]

\[
 C_2 \frac{dV_{c2}}{dt} = - \frac{1}{1-d} \frac{V_{c3} + V_{c4}}{R} + \frac{1}{1-d} \frac{d}{1-d} i_{l2}
\]

\[
 C_3 \frac{dV_{c3}}{dt} = i_{l3} - \frac{V_{c3} + V_{c4}}{R}
\]

\[
 C_4 \frac{dV_{c4}}{dt} = i_{l2} - \frac{d}{1-d} i_{l3} - \frac{V_{c3} + V_{c4}}{R}
\]

By substituting (75)-(83) into (68)-(74), extracting the DC and AC values and omitting the higher order small signal terms we have:

\[
 L_i \frac{d\hat{i}_{l1}}{dt} = dV_i + \hat{d} \left( V_{c1} + V_{c3} \right) \left( -1-d \right) \hat{V}_i
\]

\[
 L_i \frac{d\hat{i}_{l2}}{dt} = dV_{c1} + \hat{d} \left( V_{c1} - V_{c4} + V_i + V_{c2} \right) + dV_i \left( -1-d \right) \hat{V}_c
\]
\[
L_3 \frac{di_{L3}}{dt} = dV_{c1} + dV_{c2} - dV_{c3} + dV_{c4} +
\]
\[
\dot{d}(V_{c1} - V_{c4} + V_s + V_{c2}) + dV_s,
\]
\[
C_i \frac{dV_{c1}}{dt} = -d\dot{i}_{L1} \dot{i}_{L2} (1 - d) \dot{i}_{L3} I_i + (1 - d) \dot{i}_{L1} i_i
\]
\[
C_2 \frac{dV_{c2}}{dt} = \frac{\dot{i}_{L2}}{R} - \frac{V_{c1} + V_{c4}}{R}
\]
\[
C_3 \frac{dV_{c3}}{dt} = \frac{\dot{i}_{L3}}{R} - \frac{V_{c1} + V_{c4}}{R}
\]
\[
C_4 \frac{dV_{c4}}{dt} = \frac{\dot{i}_{L4}}{R} - \frac{V_{c1} + V_{c4}}{R}
\]

From equations (84)-(90), the state-space form of the equations can be achieved as follows:

\[
x = [\dot{i}_{L1} \dot{i}_{L2} \dot{i}_{L3} V_{c1} V_{c2} V_{c3} V_{c4}]
\]
\[
u = [d V_s]
\]
\[
K = \begin{bmatrix}
L_1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & L_2 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & L_3 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & C_1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & C_2 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & C_3 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & C_4 \\
\end{bmatrix}
\]
\[
A = \begin{bmatrix}
0 & 0 & 0 & -1 & -d & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 0 \\
\end{bmatrix}
\]
\[
B = \begin{bmatrix}
V_s + V_{c1} \\
V_s - V_{c4} + V_{c1} + V_{c2} \\
V_{c1} + V_{c2} + V_s - V_{c4} \\
-i_{L1} - i_{L2} - i_{L3} \\
0 \\
0 \\
0 \\
\end{bmatrix}
\]

The matrices for the output equation (y) can be obtained as follows:

\[
y = [0 0 0 0 0 0 1]
\]
\[
V_o = [0 0 0 0 1] \begin{bmatrix}
\dot{i}_{L1} \\
\dot{i}_{L2} \\
\dot{i}_{L3} \\
V_{c1} \\
V_{c2} \\
V_{c3} \\
V_{c4} \\
\end{bmatrix}
\]

4. EXPERIMENTAL RESULTS

In order to verify the performance of the presented converter, experimental results are provided. A prototype of the proposed converter is built as shown in Fig. 13.

The proposed converter utilized components are as follows:

1) Input voltage : 25 V
2) Switching frequency: 43 kHz
3) switch: IRFP460A
4) switch on-state resistance: 0.03 ohm
5) diodes D1 and D2 : MUR860
6) diodes D1 and D2 forward resistances: 0.02 ohm
7) diodes D1 and D2 threshold voltages: 0.7 V
8) inductor L1 : 150 µH
9) inductors L2 and L3 : 315 µH
10) the equivalent series resistances (ESR) of inductor L1 : 0.01 ohm
11) the equivalent series resistances (ESR) of inductors L2 and L3 : 0.018 ohm
12) capacitors C2, C3 and C4 : 100 µF
13) capacitor C1 : 470 µF
14) the equivalent series resistances (ESR) of capacitors C2, C3 and C4 : 0.012 ohm
15) the equivalent series resistances (ESR) of capacitor C1 : 0.023 ohm

The output voltage is shown in Fig. 14(a). The output voltage is 92 V and the output power is 200 W. Figs. 14(b), 14(c) and 14(d) show the waveform of the inductors currents of L1, L2 and L3 respectively. According to Eqsns. (18)-(20), the average of inductors currents of L1, L2 and L3 are 8.1, 2.2 and 2.2 A respectively. The diode D2 voltage waveform is similar to diode D1 voltage waveform. The voltage on the diodes D1 and D2 is given in Fig. 14(e). According to Eq. (43), the voltage across the diodes D1 and D2 is equal to 71 V. The voltage on the switch
$S$ is shown in Fig. 14(f). According to (42), the switch $S$ voltage is 71 V. The voltage of inductors $L_1$, $L_2$ and $L_3$ is shown in Fig. 14(g). The voltage of inductors $L_1$, $L_2$ and $L_3$ during state 1 is 25 V and during state 2 is equal to -46 V. Fig. 14(h) shows the waveform of the diodes currents of $D_1$ and $D_2$. According to (21), the average of diodes currents of $D_1$ and $D_2$ is 6.25 A. Fig. 14(i) shows the waveform of the switch $S$ current. According to (22), the average of switch $S$ current is 12.5 A.

The conventional ZETA converter used components are as follows:

1) input voltage : 25 V
2) switching frequency: 43 kHz
3) switch on-state resistance: 0.03 ohm
4) diode $D_1$ forward resistance: 0.02 ohm
5) diode $D_1$ threshold voltage: 0.7 V
6) inductor $L_1$: 150 μH
7) inductor $L_2$: 315 μH
8) the equivalent series resistances (ESR) of inductor $L_1$: 0.01 ohm
9) the equivalent series resistances (ESR) of inductor $L_2$: 0.018 ohm
10) capacitor $C_1$: 100 μF
11) capacitor $C_2$: 470 μF
12) the equivalent series resistances (ESR) of capacitor $C_1$: 0.023 ohm
13) the equivalent series resistances (ESR) of capacitor $C_2$: 0.012 ohm

Fig. 15 shows the theoretical and experimental voltage transfer gains of the proposed converter. Fig. 16 shows the efficiency curves of converters with different output power. It is seen that the efficiency of proposed converter is higher than that of ZETA converter. Fig. 17 shows the curve of efficiency of the proposed converter versus output power. It is seen that the theoretical efficiency is higher than the experimental efficiency. Fig. 18 shows the efficiency curves of converters with different output power. It is seen that the efficiency of proposed converter is higher than that of the converter in Ref. [18] and converter II in Ref. [25].
A novel transformerless buck-boost converter based on ZETA converter is presented. In this converter, only one main switch is used, which decreases the losses and improves efficiency. The active switch voltage stress is low and switch with low on-state resistance can be utilized. The voltage gain of the converter is higher than that of the classic boost, buck-boost, ZETA, CUK and SEPIC converters. The presented converter structure is simple; hence, the converter control is simple. The buck-boost converters are used in some applications such as fuel-cell, car electronic devices, and LED drivers. Finally, the experimental results are given to verify the proposed converter.

REFERENCES


5. CONCLUSIONS

In this paper, a novel transformerless buck-boost converter...


