Design of A Single-Phase Transformerless Grid-Connected PV Inverter Considering Reduced Leakage Current and LVRT Grid Codes

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Abstract- A new single-phase transformerless grid-connected PV inverter is presented in this paper. Investigations in transformerless grid-connected PV inverters indicate the existence of the leakage current is directly related to the variable common-mode voltage (CMV), which is presented in detail. On the other hand, in recent years it has become mandatory for the transformerless grid-connected PV inverters to satisfy new grid-codes such as low-voltage ride-through (LVRT) capability via injecting reactive power during grid faults. Therefore, in this paper, the design of the proposed topolgy is based on retaining the constant CMV to suppress the leakage current and also to provide reactive power injection capability during grid faults. The control strategies for injecting reactive power in the LVRT condition are also examined. To validate the presented theoretical concepts, the performance and dynamic response of the proposed transformerless PV inverter are investigated by MATLAB/Simulink and the simulation results are presented and discussed.

Keyword: Transformerless grid-connected PV inverter; Leakage current; Common-mode voltage (CMV); LVRT.

1. INTRODUCTION

With rising energy consumption in the world, subsequently, the production of energy is demanded using fossil fuels, which leads to environmental degradation factors, and especially the rising temperature of the earth and the melting of the polar ice. Therefore, the tendency to use renewable energies is much higher than in the past decades. Among the various kinds of renewable energies, there has been great interest in exploring PV systems [1, 2]. The PV systems have become a popular trend for its great flexibility in system installation and expansion. In general, PV systems are used such two configurations as stand-alone and grid-connected [3, 4]. In grid-connected PV systems, the energy-yielding and payback period are mainly depending on the initial cost and the efficiency of the entire system. Furthermore, small size, lightweight, compact structure, and cost-effective are the important factors in the grid-connected PV systems. Therefore, the use of the transformerless grid-connected PV systems is much more considered [5, 6].

In the transformerless PV systems, due to lack of the galvanic isolation between the PV panel and the grid, also, the variable CMV in the inverter, it is possible that flows the leakage current through the parasitic capacitor of the PV panels. The leakage current increases the system losses, reduced grid-connected current quality, induces the severe conducted and causes to intensify personnel safety issues. Therefore, the leakage current should be suppressed. In order to eliminate the leakage current and also to improve the efficiency and other features in the inverter, many research works have been accomplished [7-16]. In Ref. [7], the H5 inverter is presented. This structure is based on H-Bridge with an additional switch on the DC-side to prevent the exchange of reactive power between the DC-link capacitor and the filter inductors and also to separate the grid-connected inverter from the DC source at the zero voltage levels, which has a great effect on limiting the leakage current. In Ref. [9], the authors propose the H5-D structure. This inverter is based on the H5 inverter with an additional diode to remain constant the CMV, consequently suppressing the leakage current. In Ref. [10], the H6D1 inverter which is based on H6 inverter is presented. To keep the CMV constant, a diode has been added in parallel with the inverter leg. In Ref. [11], the improved grid-connected inverter topology so-called H6D2 is presented, which can meet the condition of eliminating common-mode leakage current. This
The proposed method is based on a reconfigurable PWM method, in which it is switched between two PWM methods in the two operation conditions (normal and LVRT). Therefore, an extra control unit is required to carry out the replacement PWM. In recent years, several research works have been presented leakage current solutions for popular topologies. Also, several researchers have worked on the LVRT strategy. However, an investigation that involves these features, such as LVRT capability and reduced leakage current techniques simultaneously, has not been conducted yet. Those aspects should be taken into consideration for the design and operation of transformerless PV inverters. Otherwise, they increase the maintenance cost and decrease the total efficiency. Hence, this paper proposes a new structure of the grid-tied transformerless PV inverter and design the control system with the consideration of such operating conditions. The multilevel inverter topology that has a low leakage current and provides the LVRT capability with reactive power injection in three and five levels of the output voltage. Also, the balance in the DC-link capacitors voltage is achieved without a complicated control method and only with proper modulation. Moreover, the proposed control system is flexible and provides a satisfactory operation under different conditions.

This paper is organized as follows: in section 2, the relation between leakage current and CMV is studied and the topology of the new transformerless grid-connected PV inverter along with its modulation and operation principle is presented. In section 3, the proposed control system and LVRT strategy with reactive power injection is presented. The comprehensive comparison study on the recently proposed inverters is presented in section 4. The simulation results of performance under the LVRT and
normal conditions are indicated in section 5. Finally, the conclusion is presented in section 6.

2. LEAKAGE CURRENT STUDY AND DESCRIBE PROPOSED TOPOLOGY

2.1. Leakage current study

In the transformerless PV systems, there is no isolation due to lack of a transformer, and there is a direct connection between the panels and the grid. In these conditions, due to the absence of a parasitic capacitor between the panel and the ground, a path to flow a leakage current is created. However, if the CMV, which is the voltage of the parasitic capacitor, is varying, the leakage current flows.

![Fig. 1. Conventional H-Bridge grid-connected PV inverter](image)

![Fig. 2. The simplified equivalent circuit for analyzing leakage current](image)

In damp environments or rainy days, the leakage currents could achieve high values and increase EMI because of the parasitic capacitor capacitance increase. In this section, the exact expression of the leakage current is calculated for H-Bridge inverter with the symmetric filter, as shown in Fig. 1. Due to the very high-frequency analysis, the grid and capacitor can be ignored. The CMV and differential voltage can be obtained from the voltage of the two midpoints, A and B, as shown in Fig. 1.

\[ V_{CMV} = \frac{V_{AN} + V_{BN}}{2} \]  

\[ V_{DMV} = V_{AN} - V_{BN} \]  

By using Eq. (1) and Eq. (2), the following expression can be obtained.

\[ V_{AN} = V_{CMV} + 0.5V_{DMV} \]  

\[ V_{BN} = V_{CMV} - 0.5V_{DMV} \]  

Therefore, the equivalent circuit is simplified, as shown in Fig. 2. As you can see in Fig. 2, if the two inductors \( L_1 \) and \( L_2 \) are considered equal, the leakage current between the two parallel branches is equally divided. Therefore, the following equations can be written.

\[ -V_c - V_{CMV} - 0.5V_{DMV} + V_L = 0 \]  

\[ -V_c - V_{CMV} + 0.5V_{DMV} + V_L = 0 \]  

Using Eq. (5) and Eq. (6), the following expression can be achieved.

\[ L \frac{di_{CMV}}{dt} = 2V_c + 2V_{CMV} \]  

From Eq. (7), the following expression is derived.

\[ L \frac{d^2i_{CMV}(t)}{dt^2} = 2 \frac{i_{CMV}(t)}{C} + 2 \frac{dV_{CMV}(t)}{dt} \]  

If the CMV is constant, the following equation from Eq. (8) is obtained.

\[ L \frac{d^2i_{CMV}(t)}{dt^2} = 2 \frac{i_{CMV}(t)}{C} \]  

Using Eq. (9) can be calculated \( i_{CMV} \) as follows:

\[ i_{CMV}(t) = Ae^{\frac{\sqrt{2}}{LC}t} + Be^{-\frac{\sqrt{2}}{LC}t} \]

\[ i_{CMV}(0) = 0 \rightarrow i_{CMV}(0) = A + B \rightarrow A = -B \]

\[ \frac{di_{CMV}(0)}{dt} = 0 \rightarrow \sqrt{ \frac{2}{LC} } A - \sqrt{ \frac{2}{LC} } B = 0 \rightarrow A = B \]

\[ A = B = 0 \rightarrow i_{CMV}(t) = 0 \]

If the CMV varies. The following expression from Eq. (8) is achieved.

\[ L \frac{d^2i_{CMV}(t)}{dt^2} = 2 \frac{i_{CMV}(t)}{C} + \frac{d(V_{AN}(t) + V_{BN}(t))}{dt} \]  

Considering the fundamental harmonic of VAN and VBN (\( V_{AN_i}, V_{BN_i} \)), which are as follows, can be obtained the following equation using Eq. (11).

\[ V_{AN_i} = \frac{4}{\pi} \sin(w + \alpha)t \]

\[ V_{BN_i} = -\frac{4}{\pi} \sin(w + \alpha)t \]

\[ L \frac{d^2i_{CMV}(t)}{dt^2} = \]

\[ 2 \frac{a_{CMV}(t)}{C} + \frac{4}{\pi} (w + \alpha) \cos(w + \alpha)t - (w + \alpha) \cos(w + \alpha)t \]

Therefore, the equation above can be achieved as follows.
The characteristics of HERIC inverter relative to the conventional H-Bridge inverter have the addition of a back-to-back switch on the grid side to create zero-level output voltage. This switch provides the zero level voltage so that the reactive power exchange between the DC-link capacitor and the filter inductors will be prevented. Another feature of the HERIC inverter is its switching modulation, which is switching $S_1$ to $S_2$ with a grid frequency and a back-to-back switch alone with high frequency. This improves inverter efficiency by reducing switching losses. On the other hand, the three-level output voltage improves the waveform quality, which reduces the size of the filter. Furthermore, the proposed HERIC-II inverter adds some features to the HERIC structure by adding two back-to-back switches, as shown in Fig. 4. One of the most important characteristics in the proposed HERIC-II inverter is to isolate the panels from the grid during the zero voltage level due to the additional switch $S_5$, which blocks the leakage current path and the reactive exchange between the DC-link capacitor and the filter. Another feature is the creation of a constant CMV, according to (14), the leakage current in this condition is zero or negligible. In the proposed HERIC-II inverter, such as the HERIC inverter, switches $S_1$ to $S_3$ are switched with a grid frequency. Also, another feature of the inverter provided is the three-level and five-level output voltage due to the additional switch $S_5$. Therefore, as the number of voltage levels increases, the filter size decreases, and the design of a complex filter is not required. Besides, the LVRT standard for transformerless grid-connected PV systems has been mandatory in recent years. The grid-connected PV inverter during the severe voltage drop (voltage sag) in the grid should be connected to the grid for a definite time interval, and also can inject reactive power to support the grid. Therefore, attention to this point is quite significant in designing of the grid-connected inverter because the maintenance costs and energy losses may increase. The addition of two back-to-back switches ($S_7$, $S_8$) makes it possible to provide the LVRT standard to be satisfied with only the proposed modulation without the extra LVRT control unit, and the proposed HERIC-II inverter can have the capability of the reactive power injection to support the grid.

2.2. Description of the proposed topology and modulation

2.2.1. The proposed topology

In 2006, the Sunway presented the highly efficient and reliable inverter concept so-called HERIC, which is shown in Fig. 3. As shown in Fig. 4, the proposed structure is based on HERIC inverter, which is called HERIC-II.

According to the study, if the filter does not exist, the leakage current depends only on the state of the CMV, thus, can be expressed as follows:

$$I_{cmv} = C \frac{dV_{cmv}}{dt} \quad (14)$$

In order to prevent the flow of the leakage current, the CMV must be retained constantly.

2.2.2. The proposed modulation

As mentioned in the previous section, the proposed HERIC-II inverter can have three-level and five-level output voltage. So, in this section, the five-level strategy will be shown. The three-level modulation is a subset of the five-level modulation. In the proposed modulation, the four carrier waves $V_{c1}$, $V_{c2}$, $V_{c3}$, and $V_{c4}$ are considered with the modulation wave $V_m$, as shown in Fig. 5. The comparison of $V_m$ with four-wave the gate signal $S_1$ to $S_4$ is generated. As shown in Fig. 5, the four switches $S_1$ to $S_4$ are switched with the grid frequency, each of which will turn on a half-cycle. Only $S_5$ to $S_7$ are switched at a high rate. Therefore, in this method of modulation, the decrease in switching losses can be achieved. As shown in Fig. 6, in the switch conduction modes, in each switching mode, the number of current path elements is less than or equal to three components, which also reduces conduction losses in the proposed inverter circuit. In Fig. 6 (a), $S_1$, $S_4$, and $S_5$ are
conducted, and the output voltage is equal to \( V_{dc} \), and the \( V_{AN} \) and \( V_{BN} \) in this switching state is equal to \( V_{dc} \), and zero, respectively. Therefore, CMV is equal to \( V_{dc}/2 \). The \( S_1 \) is turned off, and the \( S_7 \) turns on. In this case, the current path is provided to create a \( V_{dc}/2 \), as shown in Fig. 6(b). The notable point is that again, the CMV is equal to \( V_{dc}/2 \), and no change in the \( V_{AN} \) and \( V_{BN} \) voltages. In Fig. 6(c), the \( S_6 \) is on, and the \( S_8 \) is off, the output voltage level is zero. However, \( V_{AN} \) and \( V_{BN} \) voltage does not change because \( S_4 \) and \( S_5 \) remain on. In this case, the displacement of the CMV does not occur. In the negative half-cycle, as in Fig. 6(d) to 6(f), the same process is repeated. All switching combinations are presented in Table 1.

![Fig. 5. The proposed modulation strategy](image)

<table>
<thead>
<tr>
<th>No.</th>
<th>On switches</th>
<th>( V_{CMV} )</th>
<th>( V_o )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>( S_1, S_4, S_3 )</td>
<td>( V_{dc}/2 )</td>
<td>( V_{dc} )</td>
</tr>
<tr>
<td>2.</td>
<td>( S_1, S_4, S_7 )</td>
<td>( V_{dc}/2 )</td>
<td>( V_{dc}/2 )</td>
</tr>
<tr>
<td>3.</td>
<td>( S_2, S_5, S_5 )</td>
<td>( V_{dc}/2 )</td>
<td>( -V_{dc}/2 )</td>
</tr>
<tr>
<td>4.</td>
<td>( S_2, S_7, S_7 )</td>
<td>( V_{dc}/2 )</td>
<td>( -V_{dc}/2 )</td>
</tr>
<tr>
<td>5.</td>
<td>( V_g &gt; 0 )</td>
<td>( S_1, S_4, S_6 )</td>
<td>( I_o &gt; 0 )</td>
</tr>
<tr>
<td>6.</td>
<td>( I_o &lt; 0 )</td>
<td>( S_3, S_6 )</td>
<td>( V_{dc}/2 )</td>
</tr>
</tbody>
</table>

As indicated in Table 1, under the normal condition \( (V_g > 0, I_o > 0 \) and \( V_g < 0, I_o < 0) \) of the grid, the proposed HERIC-II inverter has a CMV constant equal to half the DC-link voltage. However, the proposed HERIC-II inverter must be examined in the LVRT condition. For this purpose, it is assumed that the sever voltage sag has occurred in the grid voltage in positive half-cycle; therefore, the sign of the grid current \( I_o \) and the sign of the grid voltage \( V_g \) are apposite. Thus, under this condition, a negative power region (non-unity power factor) is created. In this case, the direction of the grid current \( I_o \) is through the grid to the inverter at the zero voltage state. As shown in Fig. 7, there are also current paths to create a zero voltage level in \( V_g < 0 \) and \( V_g > 0 \).

As seen in Fig. 6(a), if \( S_1, S_6 \), and \( S_7 \) are turned on at zero voltage level, the current passes through the freewheeling diode and the other switch (S6 package). Therefore, \( V_g > 0 \) and \( I_o < 0 \) has the current path to create the zero voltage state. Thus, the operation of the proposed HERIC-II inverter in unity and non-unity power factor is the same as shown in Figs. 7(a)-(b). The same process occurs in the negative half-cycle and, as shown in Figs. 7(c)-(d), the current path is the same as normal operation. According to the above, it can be concluded that the proposed HERIC-II inverter has a reactive power injection capability because in both normal and LVRT conditions, the current path does not vary in different states. Therefore, dose not causing spike or distortion in the zero levels of the output voltage. Also, it can inject reactive power without affecting the quality of output current waveform [21].

### 3. Control System

#### 3.1. Control Strategy

The control objective is to deliver a definite active and reactive power (\( P_{ref}, Q_{ref} \)) to the grid. \( P_{ref} \) is achieved from the MPPT unit and \( Q_{ref} \) is usually set to zero in normal operating condition. For this purpose, the grid voltage position must be available at any time. Therefore, to synchronize with the grid, it is necessary to estimate the amplitude and phase of the grid voltage. By using the Second-Order Generalized Integrator Quadrature Signal Generator (SOGI-QSG) that is the advanced method of the phase-locked loop (PLL) [22, 23], the orthogonal signals, \( V_a \) and \( V_f \) are generated.

Further, applying the Park transformation (\( \alpha, \beta \rightarrow dq \) ) leads to the \( V_q \) signal is given the amplitude of the output voltage and the \( V_d \) signal that is representative of grid voltage phase is made equal to zero in the steady-state. By this action, the phase and amplitude of the grid voltage are determined at any time. As shown in Fig. 8, the transfer function \( G_q(s) \) from \( V_g \) to \( V_q \) can be written as follows:

\[
G_q(s) = \frac{k\cos}{s^2 + k\cos + \omega^2^2} \tag{15}
\]

Where, \( \omega = \Omega \) is the resonant frequency of the SOGI-QSG, and the transfer function \( G_q(s) \) from \( V_g \) to \( V_f \) can be obtained as follows:

\[
G_f(s) = \frac{k\Omega^2}{s^2 + k\cos + \omega^2^2} \tag{16}
\]
Fig. 6. Operation modes of the proposed HERIC-II inverter with proposed modulation

(a) $S_1, S_4, S_5: V_{dc}$, (b) $S_1, S_6, S_7: V_{dc}/2$, (c) $S_1, S_4, S_5: V_{dc}$, (d) $S_2, S_3, S_5: V_{dc}$, (e) $S_2, S_3, S_7: V_{dc}/2$, (f) $S_2, S_3, S_6: V_{dc}$

Fig. 7. Operation modes of the proposed HERIC-II inverter with proposed modulation

(a) Unity power factor ($V_g>0$, $I_o>0$), (b) non-unity power factor ($V_g>0$, $I_o<0$), (c) unity power factor ($V_g<0$, $I_o<0$), (d) non-unity power factor ($V_g<0$, $I_o>0$)

Fig. 8. The control system includes SOGI-QSG PLL, Sag detection and LVRT strategy, and PR controller
The components $V_a$ and $V_b$ are generated, which are further transferred into DC components $V_{dc}$ and $V_{dq}$ using the park transformation. The output of the PI controller is added with the nominal frequency $\omega_c$ to form the estimated frequency $\hat{\theta}$, which is then integrated to obtain the estimated phase angle $\hat{\theta}$. Note that the estimated frequency $\hat{\theta}$ is fed-back to SOGI-QSG so that it is able to select the component at the right frequency. When the phase is locked, $V_{dq}=0$. As a result, the frequency, the phase and the amplitude of signal $V_{dq}$ are all available. The injected grid current reference can be produced by regulating the DC-link voltage and reactive power to add inner current control loop to shape the grid current in normal operation mode. For the current control loop, the Proportional-Resonant (PR) current controller is used. The PR controller with harmonic compensators presents an acceptable performance in terms of accurate tracking and fast dynamic response. The transfer function of this current controller can be obtained as follows:

$$G_c(s) = k_p + k_R \frac{s}{s^2 + \omega_n^2} + \sum_{h=3,5} k_{Rh} \frac{s}{s^2 + (h\omega_n)^2} \quad (17)$$

Where, $k_p$ is the proportional gain, $k_R$ is the fundamental resonant control gain, $k_{Rh}$ is the control gain for the $h$-order resonant controller and $\omega_n$ is the grid fundamental frequency.

The output of the current controller divided by the DC-link voltage is the reference voltage ($V_{ref}$) for inverter modulation. Then the reference voltage ($V_{ref}$) is compared with triangular carrier waves to generate the gate signals of the inverter. Therefore, under normal conditions, with the reference waveform and the desired switching combinations, the proposed inverter will operate at the unity power factor. However, if there is a decrease in the grid voltage due to the phase and amplitude change of the grid voltage, taking into

### Table 2. The Comprehensive Comparison

<table>
<thead>
<tr>
<th>Inverters</th>
<th>Semiconductor Devices</th>
<th>CMV</th>
<th>LVRT Capability (Reactive power injection)</th>
<th>Loss Distributions (%)</th>
<th>Filter</th>
<th>Device Switching Frequency ($f_d$)</th>
<th>Output Voltage Levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>H5 [7]</td>
<td>5/0</td>
<td>0</td>
<td>Variable</td>
<td>$S_1-S_2$</td>
<td>1 2</td>
<td>S:&lt; High</td>
<td>3</td>
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<tr>
<td>H5d [9]</td>
<td>5/1</td>
<td>0</td>
<td>Constant</td>
<td>$S_1-S_2$</td>
<td>1 2</td>
<td>S:&lt; High</td>
<td>3</td>
</tr>
<tr>
<td>Cascaded H5 [16]</td>
<td>10/0</td>
<td>0</td>
<td>Constant</td>
<td>$S_1-S_2$</td>
<td>2 4</td>
<td>S:&lt; High</td>
<td>3/5</td>
</tr>
<tr>
<td>Cascaded H4 [16]</td>
<td>8/0</td>
<td>0</td>
<td>Variable</td>
<td>$S_1-S_2$</td>
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<td>3/5</td>
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<td>HERIC [12]</td>
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<td>1</td>
<td>Constant</td>
<td>(by additional control unit) [19, 21]</td>
<td>1 2</td>
<td>S:&lt; Grid Freq. S:&lt; High</td>
<td>3</td>
</tr>
<tr>
<td>HERIC 1 [25]</td>
<td>7/2</td>
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<td>1 2</td>
<td>S:&lt; High</td>
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<tr>
<td>HERIC 2 [25]</td>
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<td>S:&lt; High</td>
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<td>HERIC 3 [25]</td>
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<td>H7 [26]</td>
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<td>1 2</td>
<td>S:&lt; High</td>
<td>3/5</td>
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<tr>
<td>Proposed Inverter (HERIC-II)</td>
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<td>3</td>
<td>3-levels: Constant. 5-levels: constant.</td>
<td>Yes</td>
<td>1 2</td>
<td>S:&lt; Grid Freq. S:&lt; High</td>
<td>3/5</td>
</tr>
</tbody>
</table>
account the appropriate method in LVRT operation, which is presented in the next section, reactive power injection provides without the additional control unit. Based on the analysis, the proposed inverter with the modulation technique provides current paths during the freewheeling period. As a result, reactive power injection is accomplished in the proposed HERIC-II inverter. Furthermore, the common-mode behavior of which is not compromised. The CMV is maintained at constant which helps to suppress the leakage current.

3.2. LVRT Strategy
In this section, the control system should be responsive to the variable grid behavior, especially the voltage drops. Therefore, the grid-connected controller must instantaneously calculate the voltage drop and inject the reactive power required. When the voltage sag occurs, the PV system enters into LVRT operation; the system must remain connected to the grid for a specified period, in accordance with the new grid codes [17, 24]. Also, the grid should be supported by the PV system with the reactive power injection.

In order to provide LVRT capability with reactive power injection, the proper strategy is considered. By considering the overcurrent protection of PV inverters and the reactive current injection requirements under grid faults, for single-phase PV systems, the reactive power injection strategies can be summarized as 1) constant peak current strategy, 2) constant active current strategy, 3) constant average active power strategy. In order to get specific power in the LVRT condition, a constant power strategy can be used. During the LVRT operation, the required reactive power is calculated because the $V_q$ value is defined. Therefore, $Q_{\text{ref}}$ is obtained, while the active power $P_{\text{ref}}$ remains constant.

However, in this strategy, the reactive power required may cause an over-current operation. In this case, the currents can be written as follows:

$$\begin{align*}
I_d &= \frac{1}{V_q} I_N \\
I_q &= k(1-V_q)I_N 
\end{align*}$$

Where, $I_d$, $I_N$, and $I_q$ are the active current, the nominal current, and the reactive current, respectively.

4. THE OVERALL COMPARISON
In recent years, many studies on single-phase transformerless grid-connected PV inverters are presented. In this section, the features of the most usable transformerless grid-connected PV inverters are investigated. The main criteria of these inverters are compared with the proposed inverter that is presented in Table 2. One of the most significant issues in these types of inverters is leakage current. As mentioned in section II(A), leakage current has a direct relationship with the CMV. Therefore, the constant CMV in these types of inverters plays a very important role in suppressing leakage current. However, resisting or interrupting the leakage current path at zero output voltage level can also reduce the leakage current and no reactive power exchange between the filter inductor and the DC-link capacitor, which results in increased efficiency.

Therefore, the main reason for the recently proposed structures such as H5 [7], H5D [9], H6 [22], H6D1 [10], H6D2 [22], H7 [26], HERIC [12], HERIC 1 [25], HERIC 2 [25], HERIC 3 [25], etc. was to eliminate the leakage current by adding the switches to the base H-Bridge structure. In these structures, the leakage current is suppressed by different techniques. However, the leakage current cannot be effectively suppressed in different conditions (unity and non-unity power factor).

The proposed inverter utilizes two techniques such as having the CMV constant similar to H5D, HERIC, H6D2, and H7, as shown in Table 2, and also isolating the panel from the grid while generating zero output voltage level similar to H5, H5D, H6, H6D1, H6D2, and H7. Therefore, this solution severely suppresses leakage current and increases efficiency by preventing reactive power exchange at zero output voltage level between filter inductors and DC-link capacitors. However, these single-phase topologies are limited to three-level inverters. In PV grid-connected systems, the panels need to reach utility power levels. Therefore, it supports the possibility of using multilevel inverters for high power applications. Multilevel inverters have an advantage over two- and three-level inverters in high power and low power system, which can decrease the total harmonic distortion, voltage stress of $dv/dt$ on switches, EMI and increase the output waveform quality [27-29]. However, few papers have been presented concerning eliminating the leakage current for the single-phase cascaded multilevel inverters. The proposed structure is also able to generate a five-level voltage, while in cascaded H5 [16], cascaded H4 [16], H8 [13], and H6D2 [22] can provide the five-level output voltage. However, in the cascaded H4 [16], H8 [13], and H6D2 [22] at the five-level output voltage, the CMV does not remain constant, while in the proposed structure and Cascaded H5 at the five-level output voltage, the CMV remains constant. On the other hand, a rather large filter is used in the Cascaded H5 to create a constant CMV and a low leakage current, however, in the proposed inverter with the same number of switches along with
the simple and small size filter, due to the use of two techniques in the structure. The leakage current is also much lower than that of H8, H6D2, cascaded H4, and Cascaded H5. Another important issue in this type of inverters is the necessity of LVRT capability with reactive power injection. Some structures, such as H6, HERIC 1, HERIC 2, and HERIC 3, are generally not capable of injecting reactive power considering that severe current distortions will introduce more power losses, may trip the inverter overcurrent protection, and further may cause failures of the power devices. In some structures such as HERIC and H6D1, by adding the extra control unit [19, 21], the capability of reactive power injection without distorting the output current waveform is achieved. The cascaded H4, cascaded H5, H7, H8, and Proposed inverter, in a wide range of grid voltage levels, can provide required reactive power during LVRT operation. However, H5, H5D, and H6D2 are also capable of riding through the voltage sag within a voltage range > 0.5 p.u.

5. THE SIMULATION RESULTS

The simulation result is carried out by MATLAB/Simulink to validate the theoretical concepts. The proposed HERIC-II inverter is investigated in 1 kW. The dc input voltage is equal to 320V, and the specification of the grid is 220V/50Hz. Considering the switching frequency which is 10 kHz the size of the filter inductors is obtained $L_1=3.6\, \text{mH}$, $L_2=0.7\, \text{mH}$, also the value of the capacitor $C_1=2.3\, \mu\text{F}$, and the resistance $R_d=5\, \Omega$ is considered. Besides, the stray capacitance is illustrated by the capacitor $C_p=150\,\text{nF}$. Also, the DC-link capacitors have the same value as 600 µF.

In theory, it was claimed that the proposed HERIC-II inverter provides five-level and three-level voltage outputs, and in both cases, the value of the CMV constant and the amount of leakage current are negligible.

Therefore, as indicated in Fig. 9(a), the output voltage before LCL filter is three-level as +320, 0, -320V. In Fig. 9(b), the FFT analysis is presented. In this modulation, it can be seen that the harmonics have a significant amount at a frequency of twice the switching frequency. In this case, the effect of these harmonics can be significantly reduced by a small size filter. As shown in Fig. 9(c), the CMV is constant and equal to dc input voltage, which corresponds to Table 1. according to (15), also the $S_5$ role in the proposed structure causing to suppress the leakage current. As shown in Fig. 9(d), the amount of the leakage current is 0.05mA, so this is much less than VDE-0126-1-1. In Fig. 10(a), the output voltage before LCL filter is five-level as +320, +160, 0, -160, -320V. As illustrated in Fig. 10(b), the THD in five-level is 33.54%, and in three-level is 64.24%. The THD in five-level is considerably less than three levels, and this improves the quality of the output waveform. The notable point is that the CMV is constant at five levels, and the leakage current is approximately the same 0.05mA.

In Fig. 11, the performance of the proposed HERIC-II inverter is indicated in normal and LVRT conditions. In this study, the grid voltage is investigated in two ideal and non-ideal conditions, which are shown in Figs 11(a) and 11(b), respectively. The performance of the proposed inverter with the controller used in the two case studies is almost identical because of the use of SOGI and PR controller in the control system. The SOGI is an adaptive filter which filters out the harmonic contents of the grid voltage so that the harmonics have negligible effect on the control system performance.
When the voltage drop in the grid occurs (voltage sag 0.25 p.u), the inverter does not stay in synchronization. Therefore, $V_d$ and $V_q$ change (Fig. 8). Thus, the control system must be synchronized with the grid within a short time, and the amount of reactive power calculated from $V_q$ value that should be injected into the grid. As can be seen in Figs. 11(a), (b) and (c), the control system has a quick response due to the use of SOGI-QSG PLL. Regarding the average active power constant strategy at LVRT condition, the active power value remains constant during the voltage drop, and 375 Var reactive power is injected into the grid (Fig. 11(c)).

After the voltage drop has been compensated, the control system must adapt itself to the normal conditions again. So at 1.6s, as shown in Fig. 11(a), the spike in the current waveform can be seen and returned to normal operation in a short time. This spike is again due to changes in the amount of $V_d$ and $V_q$. The significant point is that the waveform of the injected current into the grid is similar in normal and LVRT mode, and the quality of the output current waveform does not change [19, 21].

![Fig. 10. The performance of the proposed HERIC-II inverter with Five-level output voltage (a) Five-level output voltage (V), (b) FFT analysis, (c) CMV (V), (e) leakage current (A)](image)

![Fig. 11. The performance of the proposed HERIC-II inverter in normal and LVRT conditions (voltage sag 0.25 p.u in 1.4<t<1.6) (a) voltage (V) and current (30xA) of the grid, (b) grid voltage (V) in non-ideal condition and grid current (30xA), (c) the active P (w), and reactive power Q (Var) deliver to grid, (d) the CMV (V), (e) the RMS leakage current (A).](image)

Therefore, as shown in Figs. 11(a), (b) and (c), the proposed inverter has reactive power injection capability. Another remarkable point is that CMV, and leakage current does not change in both condition, and their values are the same, as shown in Figs. 11(d)-(e).

### 6. Conclusion

In this paper, the single-phase transformerless grid-connected PV inverter so-called HERIC-II is presented. The inverter structure is based on the HERIC inverter with two additional switches. The design of the proposed inverter is focused on maintaining a constant
CMV to suppress the leakage current and provide the reactive power injection without a supplementary control unit. The proposed inverter can generate a three-level and five-level output voltage, which results in a small filter size comparing with the two-level output voltage. A comprehensive control system for the proposed inverter has been utilized to deliver active and reactive power to the grid and is used to synchronize advanced PLL with SOGI-QSG unit that has a more accurate performance and faster dynamic response than the conventional PLL. Finally, the simulation study is carried out by MATLAB/Simulink for a 1 kW grid-connected inverter, and the simulation results are entirely in compliance with the theoretical concepts, as shown in the previous section.

REFERENCES


[24] Reference technical rules for connecting users to the active and passive LV distribution companies of electricity, Comitato Elettrotecnico Italiano, Italy, 2011.


