Journal of Operation and Automation in Power Engineering
Vol. 9, No. 1, Apr. 2021, Pages: 49-59
http://joape.uma.ac.ir

Design of A Single-Phase Transformerless Grid-Connected PV Inverter Considering Reduced Leakage Current and LVRT Grid Codes

*F. Mohammadi[1], J. Milimonfared[1], H. Rastegar[1], M. Farhadi-Kangarlu[2, *]*

[1]*Department of Electrical Engineering, Amirkabir University of Technology, Tehran, Iran.*
[2] *Faculty of Electrical and Computer Engineering, Urmia University, Urmia, Iran*

Abstract- *A new single-phase transformerless grid-connected PV inverter is presented in this paper. Investigations in transformerless grid-connected PV inverters indicate the existence of the leakage current is directly related to the variable common-mode voltage (CMV), which is presented in detail. On the other hand, in recent years it has become mandatory for the transformerless grid-connected PV inverters to satisfy new grid-codes such as low-voltage ride-through (LVRT) capability via injecting reactive power during grid faults. Therefore, in this paper, the design of the proposed topology is based on retaining the constant CMV to suppress the leakage current and also to provide reactive power injection capability during grid faults. The control strategies for injecting reactive power in the LVRT condition are also examined. To validate the presented theoretical concepts, the performance and dynamic response of the proposed transformerless PV inverter are investigated by MATLAB/Simulink and the simulation results are presented and discussed.*

Keyword: Transformerless grid-connected PV inverter; Leakage current; Common-mode voltage (CMV); LVRT.

1. INTRODUCTION

With rising energy consumption in the world, subsequently, the production of energy is demanded using fossil fuels, which leads to environmental degradation factors, and especially the rising temperature of the earth and the melting of the polar ice. Therefore, the tendency to use renewable energies is much higher than in the past decades. Among the various kinds of renewable energies, there has been great interest in exploring PV systems [1, 2]. The PV systems have become a popular trend for its great flexibility in system installation and expansion. In general, PV systems are used such two configurations as stand-alone and grid-connected [3, 4]. In grid-connected PV systems, the energy-yielding and payback period are mainly depending on the initial cost and the efficiency of the entire system. Furthermore, small size, lightweight, compact structure, and cost-effective are the important factors in the grid-connected PV systems. Therefore, the use of the transformerless grid-connected PV systems is much more considered [5, 6].

Received: 08 Nov. 2019
Revised: 02 Mar. and 06 Apr. 2020
Accepted: 27 Apr. 2020
*Corresponding author:
E-mail: m.farhadi@urmia.ac.ir (M. Farhadi-Kangarlu)
DOI: 10.22098/joape.2021.6660.1494
Research Paper

In the transformerless PV systems, due to lack of the galvanic isolation between the PV panel and the grid, also, the variable CMV in the inverter, it is possible that flows the leakage current through the parasitic capacitor of the PV panels. The leakage current increases the system losses, reduced grid-connected current quality, induces the severe conducted and causes to intensify personnel safety issues. Therefore, the leakage current should be suppressed. In order to eliminate the leakage current and also to improve the efficiency and other features in the inverter, many research works have been accomplished [7-16]. In Ref. [7], the H5 inverter is presented. This structure is based on H-Bridge with an additional switch on the DC-side to prevent the exchange of reactive power between the DC-link capacitor and the filter inductors and also to separate the grid-connected inverter from the DC source at the zero voltage levels, which has a great effect on limiting the leakage current. In Ref. [9], the authors propose the H5-D structure. This inverter is based on the H5 inverter with an additional diode to remain constant the CMV, consequently suppressing the leakage current. In Ref. [10], the H6D1 inverter which is based on H6 inverter is presented. To keep the CMV constant, a diode has been added in parallel with the inverter leg. In Ref. [11], the improved grid-connected inverter topology so-called H6D2 is presented, which can meet the condition of eliminating common-mode leakage current. This

topology has the ability to provide three-level and 5-level output voltage. Half of the DC bus voltage is applied across the DC bus IGBTs and freewheeling diodes. Therefore, it causes the midpoint to be balanced. A new modification to the H-Bridge inverter is indicated in Ref. [12], called Highly Efficient Reliable Inverter Concept (HERIC) which is being commercialized by the Sunway company. A bypass branch has been added to the H-Bridge in the AC side with two IGBTs with free-wheeling diodes. Isolates the PV from the grid during the zero voltage states, also, the CMV remains constant, thus eliminating the leakage current. In Ref. [13], To reduce the leakage current, an improvement topology based on the H6D2 inverter is presented, along with a new modulation strategy, which can ensure that the stray capacitor voltage is free of high-frequency components with eight switches in the structure. In Ref. [14], the authors have investigated the leakage current in the cascaded H-Bridge inverter. In this paper, the leakage current path has been determined, and a new modulation has been designed to prevent leakage current. Then, a new filter for multi-level structure based on the H-Bridge has been proposed. The filter is designed based on placing the impedance in the leakage current path. In Ref. [15], a new modulation strategy is proposed to reduce the leakage current. In this strategy, it is tried to retain the CMV constant in different switching combinations. In Ref. [16], the authors have claimed that by cascading two inverters of the H5, a complimentary performance is achieved. According to the presented structure in this paper, the two H5 inverters are cascaded together, and a complicated filter is also designed for it. Due to the definition of the leakage current path and the value of the CMV in this structure, it requires a specific filter. One of the features of this paper is the constant CMV with the proposed modulation, which significantly reduces the amount of leakage current. However, in asymmetric mode, the amount of leakage current increases. Moreover, many international standards for grid-connected PV systems are announced and updated every year. One of the important standards for the grid-connected PV systems is low-voltage right-through (LVRT) with reactive power injection capability [17]. Several control methods for transformerless PV inverter topologies to provide the reactive power injection in LVRT condition have been proposed [18-20]. In Ref. [18], during LVRT condition, the PWM is switched from unipolar modulation to bipolar modulation. In this case, switching losses increase because of the higher voltage variation and the higher current ripple, yielding reduced efficiency. The authors present in Ref. [19] for two widely used inverter, H5, and HERIC, a new method to provide reactive power injection to improve the performance of the H5 and HERIC in LVRT condition. In this case, a new current path is provided in order to achieve zero-voltage state during the negative power region. Based on the analysis, modulation techniques are proposed which provides a bidirectional current path during the freewheeling period. As a result, reactive power control is realized in H5 and HERIC inverters without any modification on the inverter structures. In Ref. [20], the paper has introduced a control system and given a flexible solution for the PV inverters, used to generate a suitable zero-voltage state for providing LVRT capability with reactive power injection.

The proposed method is based on a reconfigurable PWM method, in which it is switched between two PWM methods in the two operation conditions (normal and LVRT). Therefore, an extra control unit is required to carry out the replacement PWM. In recent years, several research works have been presented leakage current solutions for popular topologies. Also, several researchers have worked on the LVRT strategy. However, an investigation that involves these features, such as LVRT capability and reduced leakage current techniques simultaneously, has not been conducted yet. Those aspects should be taken into consideration for the design and operation of transformerless PV inverters. Otherwise, they increase the maintenance cost and decrease the total efficiency. Hence, this paper proposes a new structure of the grid-tied transformerless PV inverter and design the control system with the consideration of such operating conditions. The multilevel inverter topology that has a low leakage current and provides the LVRT capability with reactive power injection in three and five levels of the output voltage. Also, the balance in the DC-link capacitors voltage is achieved without a complicated control method and only with proper modulation. Moreover, the proposed control system is flexible and provides a satisfactory operation under different conditions.

This paper is organized as follows: in section 2, the relation between leakage current and CMV is studied and the topology of the new transformerless grid-connected PV inverter along with its modulation and operation principle is presented. In section 3, the proposed control system and LVRT strategy with reactive power injection is presented. The comprehensive comparison study on the recently proposed inverters is presented in section 4. The simulation results of performance under the LVRT and

normal conditions are indicated in section 5. Finally, the conclusion is presented in section 6.

2. LEAKAGE CURRENT STUDY AND DESCRIBE PROPOSED TOPOLOGY

2.1. Leakage current study

In the transformerless PV systems, there is no isolation due to lack of a transformer, and there is a direct connection between the panels and the grid. In these conditions, due to the absence of a parasitic capacitor between the panel and the ground, a path to flow a leakage current is created. However, if the CMV, which is the voltage of the parasitic capacitor, is varying, the leakage current flows.

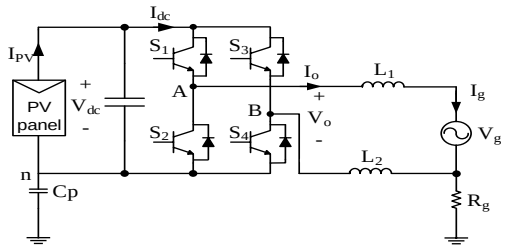


Fig. 1. Conventional H-Bridge grid-connected PV inverter

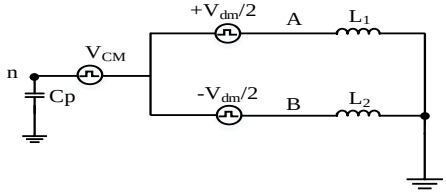


Fig. 2. The simplified equivalent circuit for analyzing leakage current

In damp environments or rainy days, the leakage currents could achieve high values and increase EMI because of the parasitic capacitor capacitance increase. In this section, the exact expression of the leakage current is calculated for H-Bridge inverter with the symmetric filter, as shown in Fig. 1. Due to the very high-frequency analysis, the grid and capacitor can be ignored. The CMV and differential voltage can be obtained from the voltage of the two midpoints, A and B, as shown in Fig. 1.

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} \tag{1}$$

$$V_{DMV} = V_{AN} - V_{BN} \tag{2}$$

By using Eq. (1) and Eq. (2), the following expression can be obtained.

$$V_{AN} = V_{CMV} + 0.5V_{DMV} \tag{3}$$

$$V_{BN} = V_{CMV} - 0.5V_{DMV} \tag{4}$$

Therefore, the equivalent circuit is simplified, as shown in Fig. 2. As you can see in Fig. 2, if the two inductors L_1 and L_2 are considered equal, the leakage current between the two parallel branches is equally divided. Therefore, the following equations can be written.

$$-V_c - V_{CMV} - 0.5V_{DMV} + V_L = 0 \tag{5}$$

$$-V_c - V_{CMV} + 0.5V_{DMV} + V_L = 0 \tag{6}$$

Using Eq. (5) and Eq. (6), the following expression can be achieved.

$$L\frac{di_{CMV}}{dt} = 2V_c + 2V_{CMV} \tag{7}$$

From Eq. (7), the following expression is derived.

$$L\frac{d^2 i_{CMV}(t)}{dt^2} = 2\frac{i_{CMV}(t)}{C} + 2\frac{dV_{CMV}(t)}{dt} \tag{8}$$

If the CMV is constant, the following equation from Eq. (8) is obtained.

$$L\frac{d^2 i_{CMV}(t)}{dt^2} = 2\frac{i_{CMV}(t)}{C} \tag{9}$$

Using Eq. (9) can be calculated i_{CMV} as follows:

$$\begin{aligned} &i_{CMV}(t) = Ae^{\sqrt{\frac{2}{LC}}t} + Be^{-\sqrt{\frac{2}{LC}}t} \\ &i_{CMV}(0) = 0 \rightarrow i_{CMV}(0) = A + B \rightarrow A = -B \\ &\frac{di_{CMV}(0)}{dt} = 0 \rightarrow \sqrt{\frac{2}{LC}}A - \sqrt{\frac{2}{LC}}B = 0 \rightarrow A = B \\ &A = B = 0 \rightarrow i_{CMV}(t) = 0 \end{aligned} \tag{10}$$

If the CMV varies. The following expression from Eq. (8) is achieved.

$$L\frac{d^2 i_{CMV}(t)}{dt^2} = 2\frac{i_{CMV}(t)}{C} + \frac{d(V_{AN}(t) + V_{BN}(t))}{dt} \tag{11}$$

Considering the fundamental harmonic of VAN and VBN ($V_{AN_{h1}}, V_{BN_{h1}}$), which are as follows, can be obtained the following equation using Eq. (11).

$$\begin{aligned} &V_{AN_{h1}} = \frac{4}{\pi}\sin(w+\alpha)t \\ &V_{BN_{h1}} = -\frac{4}{\pi}\sin(w+\alpha)t \\ &L\frac{d^2 i_{CMV}(t)}{dt^2} = \\ &2\frac{i_{CMV}(t)}{C} + \frac{4}{\pi}\left((w+\alpha)\cos(w+\alpha)t - (w+\alpha)\cos(w+\alpha)t\right) \end{aligned} \tag{12}$$

Therefore, the equation above can be achieved as follows.

$$i_{CMV}(t) = Ae^{\sqrt{\frac{2}{LC}}t} + Be^{-\sqrt{\frac{2}{LC}}t} + \sqrt{8LC} \times \frac{\sinh\sqrt{\frac{2}{LC}}t}{\pi}\left[(w+\alpha)\cos(w+\alpha)t - (w+\alpha)\cos(w+\alpha)t\right] \quad (13)$$

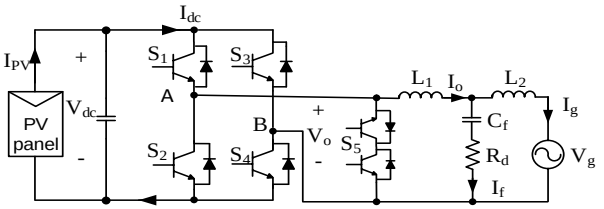


Fig. 3. The HERIC transformerless grid-connected PV inverter with LCL filter

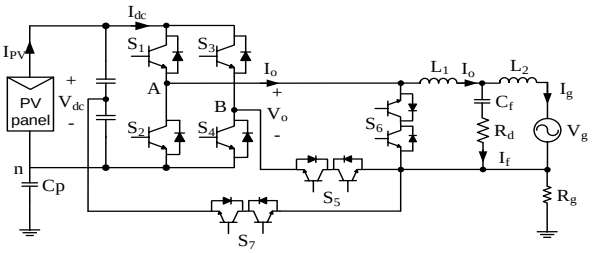


Fig. 4. The proposed HERIC-II transformerless grid-connected PV inverter with LCL filter

According to the study, if the filter does not exist, the leakage current depends only on the state of the CMV, thus, can be expressed as follows:

$$I_{CMV} = C\frac{dV_{CMV}}{dt} \quad (14)$$

In order to prevent the flow of the leakage current, the CMV must be retained constantly.

2.2. Description of the proposed topology and modulation

2.2.1. The proposed topology

In 2006, the Sunway presented the highly efficient and reliable inverter concept so-called HERIC, which is shown in Fig. 3. As shown in Fig. 4, the proposed structure is based on HERIC inverter, which is called HERIC-II.

The characteristics of HERIC inverter relative to the conventional H-Bridge inverter have the addition of a back-to-back switch on the grid side to create zero-level output voltage. This switch provides the zero level voltage so that the reactive power exchange between the DC-link capacitor and the filter inductors will be prevented. Another feature of the HERIC inverter is its switching modulation, which is switching S_1 to S_4 with a grid frequency and a back-to-back switch alone with high frequency. This improves inverter efficiency by reducing switching losses. On the other hand, the three-level output voltage improves the waveform quality, which reduces the size of the filter. Furthermore, the proposed HERIC-II inverter adds some features to the HERIC structure by adding two back-to-back switches, as shown in Fig. 4. One of the most important characteristics in the proposed HERC-II inverter is to isolate the panels from the grid during the zero voltage level due to the additional switch S_5, which blocks the leakage current path and the reactive exchange between the DC-link capacitor and the filter. Another feature is the creation of a constant CMV, according to (14), the leakage current in this condition is zero or negligible. In the proposed HERIC-II inverter, such as the HERIC inverter, switches S_1 to S_4 are switched with a grid frequency. Also, another feature of the inverter provided is the three-level and five-level output voltage due to the additional switch S_7. Therefore, as the number of voltage levels increases, the filter size decreases, and the design of a complex filter is not required. Besides, the LVRT standard for transformerless grid-connected PV systems has been mandatory in recent years. The grid-connected PV inverter during the severe voltage drop (voltage sag) in the grid should be connected to the grid for a definite time interval, and also can inject reactive power to support the grid. Therefore, attention to this point is quite significant in designing of the grid-connected inverter because the maintenance costs and energy losses may increase. The addition of two back-to-back switches (S_7, S_5) makes it possible to provide the LVRT standard to be satisfied with only the proposed modulation without the extra LVRT control unit, and the proposed HERIC-II inverter can have the capability of the reactive power injection to support the grid.

2.2.2. The proposed modulation

As mentioned in the previous section, the proposed HERIC-II inverter can have three-level and five-level output voltage. So, in this section, the five-level strategy will be shown. The three-level modulation is a subset of the five-level modulation. In the proposed modulation, the four carrier waves V_{c1}, V_{c2}, V_{c3}, and V_{c4} are considered with the modulation wave V_m, as shown in Fig. 5. The comparison of V_m with four-wave the gate signal S_1 to S_7 is generated. As shown in Fig. 5, the four switches S_1 to S_4 are switched with the grid frequency, each of which will turn on a half-cycle. Only S_5 to S_7 are switched at a high rate. Therefore, in this method of modulation, the decrease in switching losses can be achieved. As shown in Fig. 6, in the switch conduction modes, in each switching mode, the number of current path elements is less than or equal to three components, which also reduces conduction losses in the proposed inverter circuit. In Fig. 6 (a), S_1, S_4, and S_5 are

conducted, and the output voltage is equal to V_{dc}, and the V_{AN} and V_{BN} in this switching state is equal to V_{dc}, and zero, respectively. Therefore, CMV is equal to $V_{dc}/2$. The S_5 is turned off, and the S_7 turns on. In this case, the current path is provided to create a $V_{dc}/2$, as shown in Fig. 6(b). The notable point is that again, the CMV is equal to $V_{dc}/2$, and no change in the V_{AN} and V_{BN} voltages. In Fig. 6(c), the S_6 is on, and the S_5 is off, the output voltage level is zero. However, V_{AN} and V_{BN} voltage does not change because S_4 and S_1 remain on. In this case, the displacement of the CMV does not occur. In the negative half-cycle, as in Fig. 6(d) to 6(f), the same process is repeated. All switching combinations are presented in Table 1.

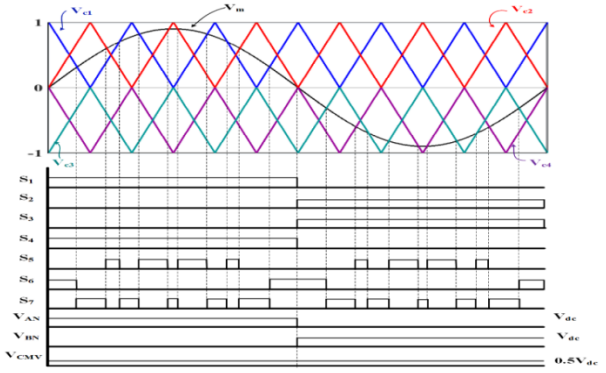


Fig. 5. The proposed modulation strategy

Table 1. All Switching Combinations

No.	On switches			V_{CMV}	Vo
1.	S_1, S_4, S_5			$V_{dc}/2$	V_{dc}
2.	S_1, S_4, S_7			$V_{dc}/2$	$V_{dc}/2$
3.	S_2, S_3, S_5			$V_{dc}/2$	$-V_{dc}$
4.	S_2, S_3, S_7			$V_{dc}/2$	$-V_{dc}/2$
5.	$V_g > 0$	S_1, S_4, S_6	$I_o > 0$	$V_{dc}/2$	0
			$I_o < 0$		
6.	$V_g < 0$	S_2, S_3, S_6	$I_o > 0$	$V_{dc}/2$	0
			$I_o < 0$		

As indicated in Table 1, under the normal condition (V_g>0, I_o>0 and V_g<0, I_o<0) of the grid, the proposed HERIC-II inverter has a CMV constant equal to half the DC-link voltage. However, the proposed HERIC-II inverter must be examined in the LVRT condition. For this purpose, it is assumed that the sever voltage sag has occurred in the grid voltage in positive half-cycle; therefore, the sign of the grid current I_o and the sign of the grid voltage V_g are apposite. Thus, under this condition, a negative power region (non-unity power factor) is created. In this case, the direction the grid current I_o is through the grid to the inverter at the zero voltage state. As shown in Fig. 7, there are also current paths to create a zero voltage level in Vg<0 and Vg>0. As seen in Fig. 6(a), if S_1, S_4, and S_5 are turned on at zero voltage level, the current passes through the freewheeling diode and the other switch (S6 package). Therefore, Vg>0 and Io<0 has the current path to create the zero voltage state. Thus, the operation of the proposed HERIC-II inverter in unity and non-unity power factor is the same as shown in Figs. 7(a)-(b). The same process occurs in the negative half-cycle and, as shown in Figs. 7(c)-(d), the current path is the same as normal operation. According to the above, it can be concluded that the proposed HERIC-II inverter has a reactive power injection capability because in both normal and LVRT conditions, the current path does not vary in different states. Therefore, dose not causing spike or distortion in the zero levels of the output voltage. Also, it can inject reactive power without affecting the quality of output current waveform [21].

3. CONTROL SYSTEM

3.1. Control Strategy

The control objective is to deliver a definite active and reactive power (P_{ref} , Q_{ref}) to the grid. P_{ref} is achieved from the MPPT unit and Q_{ref} is usually set to zero in normal operating condition. For this purpose, the grid voltage position must be available at any time. Therefore, to synchronize with the grid, it is necessary to estimate the amplitude and phase of the grid voltage. By using the Second-Order Generalized Integrator Quadrature Signal Generator (SOGI-QSG) that is the advanced method of the phase-locked loop (PLL) [22, 23], the orthogonal signals, V_α and V_β are generated. Further, applying the Park transformation ($\alpha\beta \rightarrow dq$) leads to the V_q signal is given the amplitude of the output voltage and the V_d signal that is representative of grid voltage phase is made equal to zero in the steady-state. By this action, the phase and amplitude of the grid voltage are determined at any time. As shown in Fig. 8, the transfer function $G_d(s)$ from V_g to V_α can be written as follows:

$$G_d(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{15}$$

Where, $\omega = \theta$ is the resonant frequency of the SOGI-QSG, and the transfer function $G_q(s)$ from V_g to V_β can be obtained as follows:

$$G_q(s) = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{16}$$

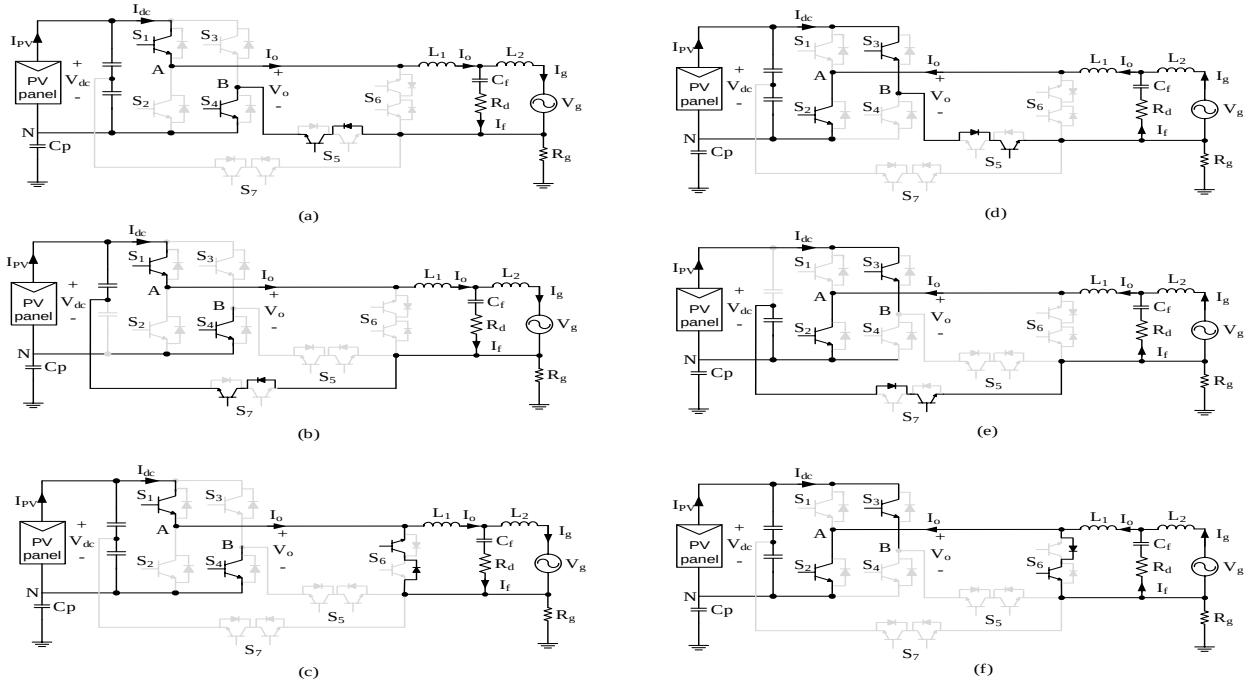


Fig. 6. Operation modes of the proposed HERIC-II inverter with proposed modulation

Vm>0: (a) S_1, S_4, S_5 : Vo=Vdc, (b) S_1, S_4, S_7 : Vo=Vdc/2, (c) S_1, S_4, S_6 : Vo=0, Vm<0: (d) S_2, S_3, S_5 : Vo=-Vdc , (e) S_2, S_3, S_7 : Vo= -Vdc/2, (f) S_2, S_3, S_6 : Vo=0

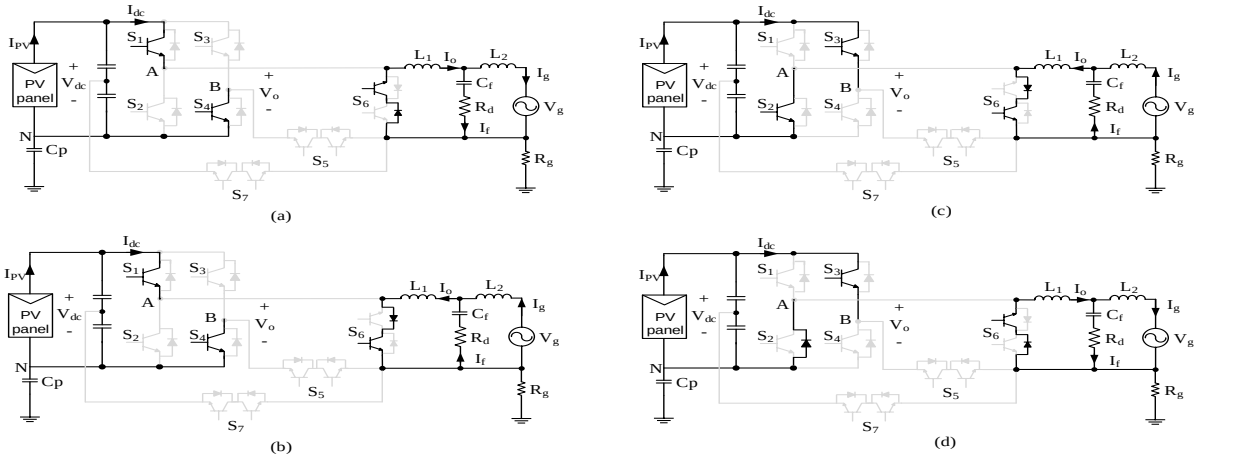


Fig. 7. Operation modes of the proposed HERIC-II inverter with proposed modulation

(a) Unity power factor (Vg>0, Io>0), (b) non-unity power factor (Vg>0, Io<0), (c) unity power factor (Vg<0, Io<0), (d) non-unity power factor (Vg<0, Io>0)

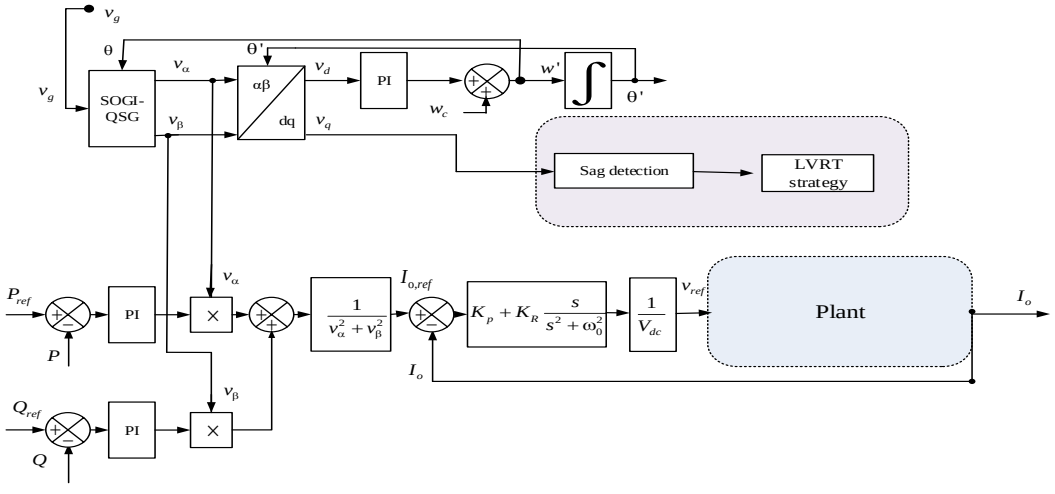


Fig. 8. The control system includes SOGI-QSG PLL, Sag detection and LVRT strategy, and PR controller

Table 2. The Comprehensive Comparison

Inverters	*Semiconductor Devices*		*CMV*	*LVRT Capability (Reactive power injection)*	*Loss Distributions (%)*	*Filter*		*Device Switching Frequency (f_s)*	*Output Voltage Levels*
	No. of IGBTs and Diodes	*No. of back to back IGBTs*				*C*	*L*		
H5 [7]	5/0	0	Variable	Yes (only when grid voltage level>0.5p.u)	$S_1 \sim S_5$ 100%	1	2	$S_{1\text{-}5}$: High	3
H5D [9]	5/1	0	Constant	Yes (only when grid voltage level>0.5p.u)	$S_1 \sim S_5$ 100%	1	2	$S_{1\text{-}5}$: High	3
Cascaded H5 [16]	10/0	0	Constant	Yes	$S_1 \sim S_5$ 50%; $S_6 \sim S_{10}$ 50%	2	4	$S_{1\text{-}10}$: High	3/5
Cascaded H4 [16]	8/0	0	Variable	Yes	$S_1 \sim S_4$ 50%; $S_5 \sim S_8$ 50%	1	2	$S_{1\text{-}8}$: High	3/5
HERIC [12]	4/0	1	Constant	Yes (by additional control unit) [19, 21]	$S_1 \sim S_4$ 73%; S_5 27%	1	2	$S_{1\text{-}4}$: Grid Freq. S_5: High	3
HERIC 1 [25]	7/2	0	Variable	No	S_1 & S_4 16%; S_2 & S_3 16%; $S_5 \sim S_7$ 68%	1	2	$S_{1\text{-}7}$: High	3
HERIC 2 [25]	5/0	1	Variable	No	S_1 & S_4 16%; S_2 & S_3 16%; $S_5 \sim S_7$ 68%	1	2	$S_{1\text{-}7}$: High	3
HERIC 3 [25]	6/4	0	Variable	No	S_1 & S_4 16%; S_2 & S_3 16%; $S_5 \sim S_7$ 68%	1	2	$S_{1\text{-}7}$: High	3
H7 [26]	7/0	0	Constant	Yes	S_3 & S_4 26%; S_1 & S_2 32%; $S_5 \sim S_7$ 42%			$S_{1\text{-}7}$: High	3
H8 [13]	8/0	0	3-levels: Constant. 5-levels: Variable.	Yes	$S_5 \sim S_8$ 73%; $S_1 \sim S_4$ 27%	1	2	$S_{1\text{-}4}$: Grid Freq. $S_{5\text{-}8}$: High	3/5
H6 [22]	6/0	0	Variable	No	S_1 & S_4 25%; S_2 & S_3 25%; S_5 & S_6 50%	1	2	$S_{1\text{-}6}$: High	3
H6D1 [10]	6/1	0	Variable	Yes (by additional control unit) [21]	S_5 & S_6 73%; $S_1 \sim S_4$ 27%	1	2	$S_{1\text{-}4}$: Grid Freq. $S_{5,6}$: High	3
H6D2 [22]	6/2	0	3-levels: Constant. 5-levels: Variable.	Yes (only when grid voltage level>0.5p.u)	S_3 & S_4 26%; S_1 & S_2 32%; S_5 & S_6 42%	1	2	$S_{1\text{-}6}$: High	3/5
Proposed Inverter (HERIC-II)	4/0	3	3-levels: Constant. 5-levels: constant.	Yes	$S_5 \sim S_7$ 73%; $S_1 \sim S_4$ 27%	1	2	$S_{1\text{-}4}$: Grid Freq. $S_{5\text{-}7}$: High	3/5

The components V_α and V_β are generated, which are further transferred into DC components V_d and V_q using the park transformation. The output of the PI controller is added with the nominal frequency ω_c to form the estimated frequency θ, which is then integrated to obtain the estimated phase angle θ'. Note that the estimated frequency θ is fed-back to SOGI-QSG so that it is able to select the component at the right frequency. When the phase is locked, v_d =0. As a result, the frequency, the phase and the amplitude of signal V_g are all available. The injected grid current reference can be produced by regulating the DC-link voltage and reactive power to add inner current control loop to shape the grid current in normal operation mode. For the current control loop, the Proportional-Resonant (PR) current controller is used. The PR controller with harmonic compensators presents an acceptable performance in terms of accurate tracking and fast dynamic response. The transfer function of this current controller can be obtained as follows:

$$G_I(s) = k_p + k_R \frac{s}{s^2 + \omega_o^2} + \sum_{h=3,5,7} \frac{k_{Rh} s}{s^2 + (h\omega_o)^2} \quad (17)$$

Where, k_p is the proportional gain, k_R is the fundamental resonant control gain, k_{Rh} is the control gain for the h-order resonant controller and ω_o is the grid fundamental frequency.

The output of the current controller divided by the DC-link voltage is the reference voltage (V_{ref}) for inverter modulation. Then the reference voltage (V_{ref}) is compared with triangular carrier waves to generate the gate signals of the inverter. Therefore, under normal conditions, with the reference waveform and the desired switching combinations, the proposed inverter will operate at the unity power factor. However, if there is a decrease in the grid voltage due to the phase and amplitude change of the grid voltage, taking into

account the appropriate method in LVRT operation, which is presented in the next section, reactive power injection provides without the additional control unit. Based on the analysis, the proposed inverter with the modulation technique provides current paths during the freewheeling period. As a result, reactive power injection is accomplished in the proposed HERIC-II inverter. Furthermore, the common-mode behavior of which is not compromised. The CMV is maintained at constant which helps to suppress the leakage current.

3.2. LVRT Strategy

In this section, the control system should be responsive to the variable grid behavior, especially the voltage drops. Therefore, the grid-connected controller must instantaneously calculate the voltage drop and inject the reactive power required. When the voltage sag occurs, the PV system enters into LVRT operation; the system must remain connected to the grid for a specified period, in accordance with the new grid codes [17, 24]. Also, the grid should be supported by the PV system with the reactive power injection.

In order to provide LVRT capability with reactive power injection, the proper strategy is considered. By considering the overcurrent protection of PV inverters and the reactive current injection requirements under grid faults, for single-phase PV systems, the reactive power injection strategies can be summarized as 1) constant peak current strategy, 2) constant active current strategy, 3) constant average active power strategy. In order to get specific power in the LVRT condition, a constant power strategy can be used. During the LVRT operation, the required reactive power is calculated because the V_q value is defined. Therefore, Q_{ref} is obtained, while the active power P_{ref} remains constant. However, in this strategy, the reactive power required may cause an over-current operation. in this case, the currents can be written as follows:

$$\begin{cases} I_d = \dfrac{1}{V_g} I_N \\ I_q = k(1-V_g) I_N \end{cases} \tag{18}$$

Where, I_d , I_N , and I_q are the active current, the nominal current, and the reactive current, respectively.

4. THE OVERALL COMPARISON

In recent years, many studies on single-phase transformerless grid-connected PV inverters are presented. In this section, the features of the most usable transformerless grid-connected PV inverters are investigated. The main criteria of these inverters are compared with the proposed inverter that is presented in Table 2. One of the most significant issues in these types of inverters is leakage current. As mentioned in section II(A), leakage current has a direct relationship with the CMV. Therefore, the constant CMV in these types of inverters plays a very important role in suppressing leakage current. However, resisting or interrupting the leakage current path at zero output voltage level can also reduce the leakage current and no reactive power exchange between the filter inductor and the DC-link capacitor, which results in increased efficiency. Therefore, the main reason for the recently proposed structures such as H5 [7], H5D [9], H6 [22], H6D1 [10], H6D2 [22], H7 [26], HERIC [12], HERIC 1 [25], HERIC 2 [25], HERIC 3 [25], etc. was to eliminate the leakage current by adding the switches to the base H-Bridge structure. In these structures, the leakage current is suppressed by different techniques. However, the leakage current cannot be effectively suppressed in different conditions (unity and non-unity power factor). The proposed inverter utilizes two techniques such as having the CMV constant similar to H5D, HERIC, H6D2, and H7, as shown in Table 2, and also isolating the panel from the grid while generating zero output voltage level similar to H5, H5D, H6, H6D1, H6D2, and H7. Therefore, this solution severely suppresses leakage current and increases efficiency by preventing reactive power exchange at zero output voltage level between filter inductors and DC-link capacitors. However, these single-phase topologies are limited to three-level inverters. In PV grid-connected systems, the panels need to reach utility power levels. Therefore, it supports the possibility of using multilevel inverters for high power applications. Multilevel inverters have an advantage over two- and three-level inverters in high power and low power system, which can decrease the total harmonic distortion, voltage stress of dv/dt on switches, EMI and increase the output waveform quality [27-29]. However, few papers have been presented concerning eliminating the leakage current for the single-phase cascaded multilevel inverters. The proposed structure is also able to generate a five-level voltage, while in cascaded H5 [16], cascaded H4 [16], H8 [13], and H6D2 [22] can provide the five-level output voltage. However, in the cascaded H4 [16], H8 [13], and H6D2 [22] at the five-level output voltage, the CMV does not remain constant, while in the proposed structure and Cascaded H5 at the five-level output voltage, the CMV remains constant. On the other hand, a rather large filter is used in the Cascaded H5 to create a constant CMV and a low leakage current, however, in the proposed inverter with the same number of switches along with

the simple and small size filter, due to the use of two techniques in the structure. The leakage current is also much lower than that of H8, H6D2, cascaded H4, and Cascaded H5. Another important issue in this type of inverters is the necessity of LVRT capability with reactive power injection. Some structures, such as H6, HERIC 1, HERIC 2, and HERIC 3, are generally not capable of injecting reactive power considering that severe current distortions will introduce more power losses, may trip the inverter overcurrent protection, and further may cause failures of the power devices. In some structures such as HERIC and H6D1, by adding the extra control unit [19, 21], the capability of reactive power injection without distorting the output current waveform is achieved. The cascaded H4, cascaded H5, H7, H8, and Proposed inverter, in a wide range of grid voltage levels, can provide required reactive power during LVRT operation. However, H5, H5D, and H6D2 are also capable of riding through the voltage sag within a voltage range > 0.5 p.u.

5. The Simulation Results

The simulation result is carried out by MATLAB/Simulink to validate the theoretical concepts. The proposed HERIC-II inverter is investigated in 1 kW. The dc input voltage is equal to 320V, and the specification of the grid is 220V/50Hz. Considering the switching frequency which is 10 kHz the size of the filter inductors is obtained L_1 =3.6 mH, L_2 =0.7 mH, also the value of the capacitor C_f =2.3 µF, and the resistance R_d=5 Ω is considered. Besides, the stray capacitance is illustrated by the capacitor Cp=150nF. Also, the DC-link capacitors have the same value as 600 µF. In theory, it was claimed that the proposed HERIC-II inverter provides five-level and three-level voltage outputs, and in both cases, the value of the CMV constant and the amount of leakage current are negligible.

Therefore, as indicated in Fig. 9(a), the output voltage before LCL filter is three-level as +320, 0, -320V. In Fig. 9(b), the FFT analysis is presented. In this modulation, it can be seen that the harmonics have a significant amount at a frequency of twice the switching frequency. In this case, the effect of these harmonics can be significantly reduced by a small size filter. As shown in Fig. 9(c), the CMV is constant and equal to dc input voltage, which corresponds to Table 1. according to (15), also the S_5 role in the proposed structure causing to suppress the leakage current. As shown in Fig. 9(d), the amount of the leakage current is 0.05mA, so this is much less than VDE-0126-1-1. In Fig. 10(a), the output voltage before LCL filter is five-level as +320, +160, 0, -160, -320V. As illustrated in Fig. 10(b), the THD in five-level is 33.54%, and in three-level is 64.24%. The THD in five-level is considerably less than three levels, and this improves the quality of the output waveform. The notable point is that the CMV is constant at five levels, and the leakage current is approximately the same 0.05mA.

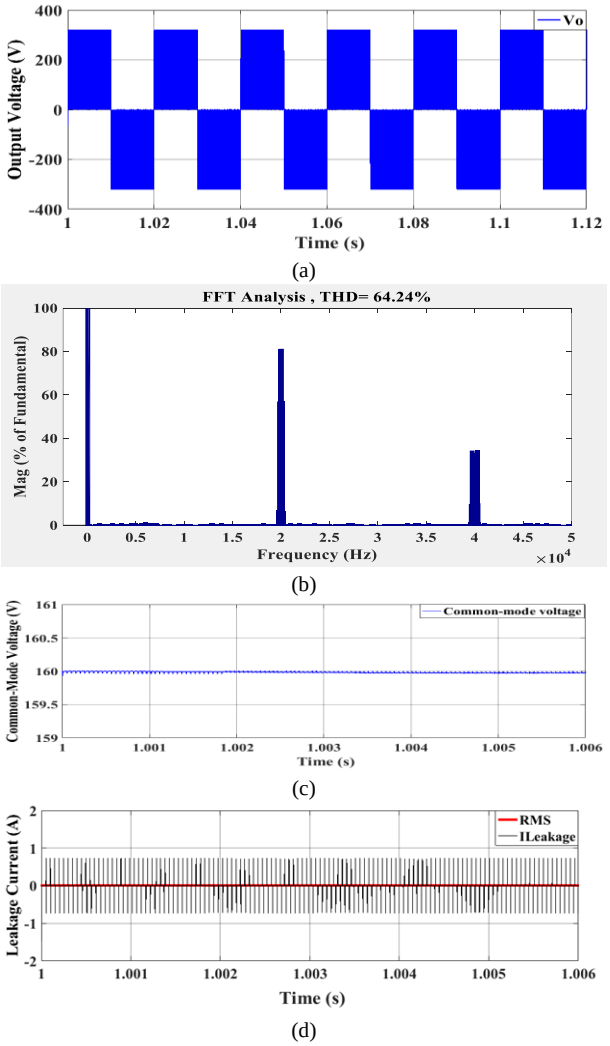
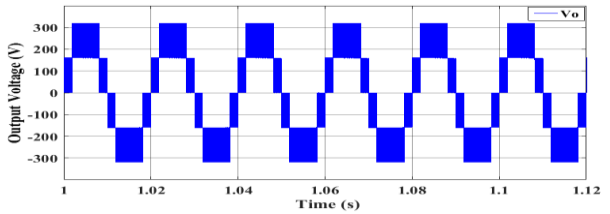


Fig. 9. The performance of the proposed HERIC-II inverter with a three-level output voltage (a) three-level output voltage (V), (b) FFT analysis, (c) CMV (V), (c) leakage current (A)

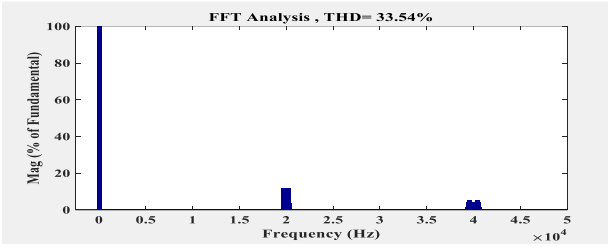
In Fig. 11, the performance of the proposed HERIC-II inverter is indicated in normal and LVRT conditions. In this study, the grid voltage is investigated in two ideal and non-ideal conditions, which are shown in Figs 11(a) and 11(b), respectively. The performance of the proposed inverter with the controller used in the two case studies is almost identical because of the use of SOGI and PR controller in the control system. The SOGI is an adaptive filter which filters out the harmonic contents of the grid voltage so that the harmonics have negligible effect on the control system performance.

When the voltage drop in the grid occurs (voltage sag 0.25 p.u), the inverter does not stay in synchronization. Therefore, V_d and V_q change (Fig. 8). Thus, the control system must be synchronized with the grid within a short time, and the amount of reactive power calculated from V_q value that should be injected into the grid. As can be seen in Figs. 11(a), (b) and (c), the control system has a quick response due to the use of SOGI-QSG PLL. Regarding the average active power constant strategy at LVRT condition, the active power value remains constant during the voltage drop, and 375 Var reactive power is injected into the grid (Fig. 11(c)).

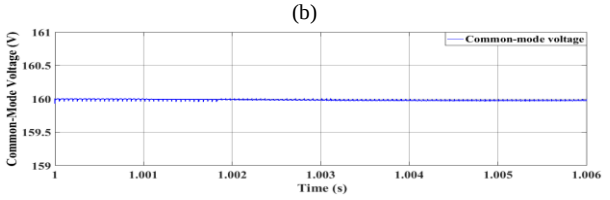
After the voltage drop has been compensated, the control system must adapt itself to the normal conditions again. So at 1.6s, as shown in Fig. 11(a), the spike in the current waveform can be seen and returned to normal operation in a short time. This spike is again due to changes in the amount of V_d and V_q. The significant point is that the waveform of the injected current into the grid is similar in normal and LVRT mode, and the quality of the output current waveform does not change [19, 21].



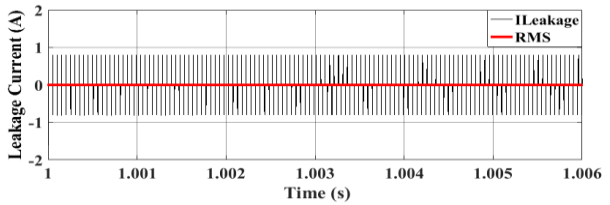
(a)



(b)

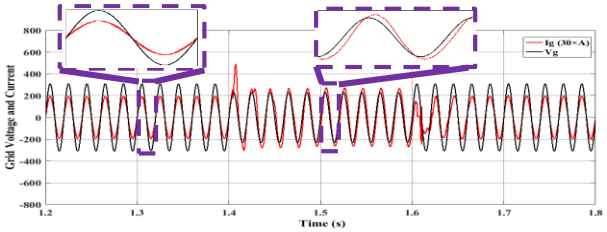


(c)

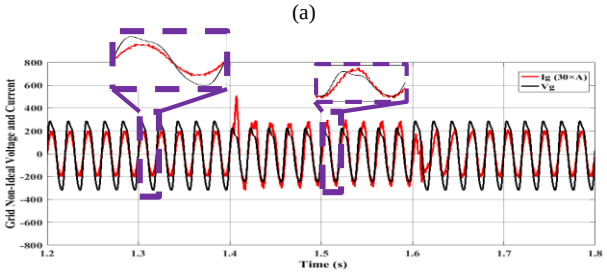


(d)

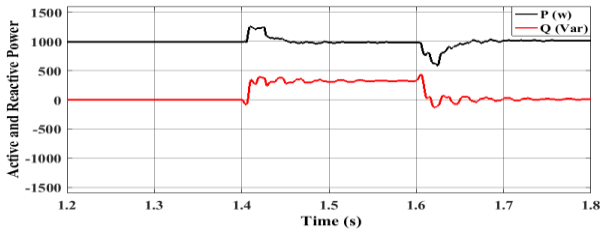
Fig. 10. The performance of the proposed HERIC-II inverter with Five-level output voltage (a) Five-level output voltage (V), (b) FFT analysis, (c) CMV (V), (c) leakage current (A)



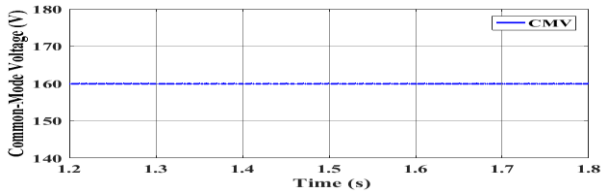
(a)



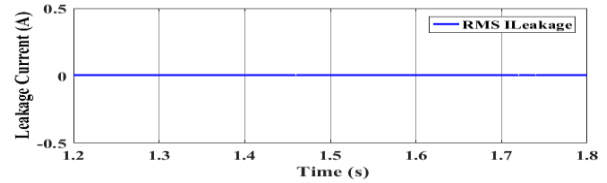
(b)



(c)



(d)



(e)

Fig. 11. The performance of the proposed HERIC-II inverter in normal and LVRT conditions (voltage sag 0.25 p.u in 1.4<t<1.6) (a) voltage (V) and current (30×A) of the grid, (b) grid voltage (V) in non-ideal condition and grid current (30×A), (c) the active P (w), and reactive power Q (Var) deliver to grid, (d) the CMV (V), (e) the RMS leakage current (A).

Therefore, as shown in Figs. 11(a), (b) and (c), the proposed inverter has reactive power injection capability. Another remarkable point is that CMV, and leakage current does not change in both condition, and their values are the same, as shown in Figs. 11(d)-(e).

6. CONCLUSION

In this paper, the single-phase transformerless grid-connected PV inverter so-called HERIC-II is presented. The inverter structure is based on the HERIC inverter with two additional switches. The design of the proposed inverter is focused on maintaining a constant

CMV to suppress the leakage current and provide the reactive power injection without a supplementary control unit. The proposed inverter can generate a three-level and five-level output voltage, which results in a small filter size comparing with the two-level output voltage. A comprehensive control system for the proposed inverter has been utilized to deliver active and reactive power to the grid and is used to synchronize advanced PLL with SOGI-QSG unit that has a more accurate performance and faster dynamic response than the conventional PLL. Finally, the simulation study is carried out by MATLAB/Simulink for a 1 kW grid-connected inverter, and the simulation results are entirely in compliance with the theoretical concepts, as shown in the previous section.

REFERENCES

[1] Trends 2018 in photovoltaic applications: Survey report of selected IEA countries between 1992 and 2017, Report IEA PVPS T1-34:2018.

[2] A. Yazdankhah and R. Kazemzadeh, "Power management in a utility connected micro-grid with multiple renewable energy sources", *J. Oper. Autom. Power Eng.*, vol. 5, pp. 1-10, 2017.

[3] K. Kovanen, "Photovoltaics and power distribution", *Renewable Energy Focus*, vol. 14, pp. 20-21, 2013.

[4] M. Islam, S. Mekhilef and M. Hasan, "Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review", *Renewable Sustainable Energy Rev.*, vol. 45, pp. 69-86, 2015.

[5] Y. Gu et al., "Transformerless inverter with virtual DC bus concept for cost-effective grid-connected PV power systems", *IEEE Trans. Power Electron.*, vol. 28, pp. 793-805, 2013.

[6] M. Khan et al., "Transformerless inverter topologies for single-phase photovoltaic systems: a comparative review", *IEEE J. Emerging Sel. Top. Power Electron.*, 2019.

[7] T. Remus, M. Liserre and Pedro Rodriguez, "Grid converters for photovoltaic and wind power systems", vol. 29, John Wiley & Sons, 2011.

[8] T. Freddy, N. Rahim, W. Hew and H. Che, "Comparison and analysis of single-phase transformerless grid-connected PV inverters", *IEEE Trans. Power Electron.*, vol. 29, pp. 5358-5369, 2014.

[9] H. Li et al., "An improved H5 topology with low common-mode current for transformerless PV grid-connected inverter", *IEEE Trans. Power Electron.*, vol. 34, pp. 1254-1265, 2019.

[10] R. Gonzalez et al., "High-efficiency transformerless single-phase photovoltaic inverter", *12th Int. Power Electron. Motion Control Conf.*, pp. 1895-1900, 2006.

[11] W. Yu, J. Lai, H. Qian and C. Hutchens, "High-efficiency MOSFETInverter with H6-type configuration for photovoltaic nonisolated ac-module applications", *IEEE Trans. Power Electron.*, vol. 26, pp. 1253-60, 2011.

[12] B. Yang, W. Li, Y. Gu, W. Cui and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system", *IEEE Trans. Power Electron*., vol. 27, pp. 752-762, 2012.

[13] M. Kangarlu, E. Babaei and F. Blaabjerg, "An LCL-filtered Single-phase multilevel inverter for grid integration of PV systems", *J. Oper. Autom. Power Eng.*, vol. 4, pp. 54-65, 2016.

[14] Y. Zhou and H. Li, "Analysis and suppression of leakage current in cascaded-multilevel-inverter-based PV systems", *IEEE Trans. Power Electron.*, vol. 29, pp. 5265-77, 2014.

[15] G. Vazquez et al., "A modulation strategy for single-phase HB-CMI to reduce leakage ground current in transformer-less PV applications", 3*9th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 210-215, 2013.

[16] X. Guo and X. Jia, "Hardware-based cascaded topology and modulation strategy with leakage current reduction for transformerless PV systems", *IEEE Trans. Ind. Electron.*, vol. 63, pp. 7823-7832, 2016.

[17] Y. Yang et al., "Low-voltage ride-through of single-phase transformerless photovoltaic inverters", *IEEE Trans. Ind. Appl.*, vol. 50, pp. 1942-52, 2014.

[18] T. Wu, C. Kuo, K. Sun and H. Hsieh, "Combined unipolar and bipolar PWM for current distortion improvement during power compensation", *IEEE Trans. Power Electron*., vol. 29, pp. 1702-1709, 2014.

[19] T. Freddy, J. Lee, H. Moon, K. Lee and N. Rahim, "Modulation technique for single-phase transformerless photovoltaic inverters with reactive power capability", *IEEE Trans. Ind. Electron.*, vol. 64, pp. 6989-99, 2017.

[20] M. Kangarlu and F. Mohammadi, "Performance improvement of single-phase transformerless grid-connected PV inverters regarding common-mode voltage (CMV) and LVRT", *J. Oper. Autom. Power Eng.*, vol. 7, pp. 1-15, 2019.

[21] M. Kangarlu and F. Mohammadi, "Performance comparison of single-phase transformerless grid-connected PV inverters", *9th Annu. Power Electron., Drives Syst. Technol. Conf.*, pp. 71-76, 2018.

[22] T. Remus, M. Liserre and Pedro Rodriguez, "Grid converters for photovoltaic and wind power systems", vol. 29. John Wiley & Sons, 2011.

[23] Y. Yang, F. Blaabjerg and Z. Zou, "Benchmarking of grid fault modes in single-phase grid-connected photovoltaic systems", *IEEE Trans. Ind. Appl.*, vol. 49, pp. 2167-2176, 2013.

[24] Reference technical rules for connecting users to the active and passive LV distribution companies of electricity, *Comitato Elettrotecnico Italiano, Italy, 2011.*

[25] W. Li et al., "Topology review and derivation methodology of single-phase transformerless photovoltaic inverters for leakage current suppression", *IEEE Trans. Ind. Electron.*, vol. 62, pp. 4537-51, 2015.

[26] E. Akpınar, A. Balıkcı, E. Durbaba and B. T. Azizoğlu, "Single-phase transformerless photovoltaic inverter with suppressing resonance in improved H6", *IEEE Trans. Power Electron*., vol. 34, pp. 8304-16, 2019.

[27] E. Babaei, M. Kangarlu and M. Hosseinzadeh, "Asymmetrical multilevel converter topology with reduced number of components", *IET Power Electron.*, vol. 6, pp. 1188-1196, 2013.

[28] S. Hosseini, M. Kangarlu and A. Sadigh, "A new topology for multilevel current source inverter with reduced number of switches", *Int. Conf. Electr. Electron, Eng.*, pp. 273-277, 2009.

[29] E. Babaei, S. Laali, and M. Sharifian, "Reduction the number of power electronic devices of a cascaded multilevel inverter based on new general topology", *J. Oper. Autom. Power Eng.* vol. 2, pp. 81-90, 2014.