

A Detailed Model of a Half Bridge IGBT Power Module Based on the Analytical Calculation and Measurement for EMC Study

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Abstract- The parasitic parameters of an IGBT power module cause various problems, especially for electromagnetic compatibility (EMC) concerns. The high-variations in voltage and current produced by the inductances/capacitances near switches in the transient process are the main sources of high-frequency electromagnetic interference (EMI). To overcome the problems, the parasitic parameters of the module should be accurately characterized. In this paper, a precise detailed model of a commercial half-bridge IGBT module is presented. It includes the parasitic inductances of leads, bond wires, DBC plates, and the parasitic capacitances of the module and IGBTs. The new simplified analytical equations to calculate the partial inductance and parasitic capacitance are proposed and compared with ANSYS Q3D results. To evaluate the accuracy of the model, all the parameters are also derived from a two-port measurement-based parasitic extraction method. The results show an acceptable match between the simulated and experimental values. Finally, the proposed model is implemented by state-space dynamic coupling in ANSYS Simplorer circuit simulator, and a double-pulse test circuit is used to verify the model. By comparing the simulated current and voltage waveforms with experiment, it is proved that the proposed model is applicable to simulate the switching transients for EMC study.

Keyword: Electromagnetic compatibility (EMC), IGBT detailed model, Measurement-based modeling, Parasitic Impedance, Switching transient simulation.

1. INTRODUCTION

Electromagnetic compatibility (EMC) is a major challenge in the design of the modern power electronic converters used in new aircrafts, PV systems, etc. [1-3]. The common-mode electromagnetic interference (EMI) in some power converters is generated by switching which can be regarded using reconfigurable PWM methods [4]. However, the main source of the EMI in power electronic converters is switching transients with high dv/dt or/and di/dt slew-rate. It is more critical when the parasitic inductances of the device package are relatively high. The parasitic inductances close to the semiconductor device including the parasitic inductances inside the power module (PM) play a key role to control the emissions. Since the switching transients induce voltage spikes on these inductances and the energy stored in them may resonate with the stray capacitances, leading to under-damped high-frequency oscillations [1, 5-8]. Traditionally, inserting

the passive EMI filters at the output/input side of a converter is a common technique to pass a test against the relevant EMC standards. Unluckily, the EMI filters are one of the largest units in the power converters which usually represent roughly 30% cost and volume of a converter [9]. However, some efforts were studied to minimize the filter volume by integrating the components [10], optimum design of the component rating [11], etc. In these works, it was necessary to prepare a detailed model of the system especially the parasitic element model. Moreover, in some other works, besides using the external EMI filter, the emissions were restricted from their source. In Ref. [12], a detailed measurement-based SPICE model of a power inverter including parasitic inductances was presented. Based on the model, the structures responsible for resonances were identified and possible improvements were determined to reduce the EMI noise. Authors in Ref. [13] have used an additional auxiliary switch to prepare the ZVS condition in their DC-DC bidirectional converter to reduce the EMI. In Ref. [14], a design procedure of acceptable stray inductance using the detailed model of the PM was proposed which limited the over-voltage during turn-off operation. A novel low-inductance packaging structure for multichip phase-leg SiC MOSFET module to suppress the voltage overshoots was presented in Ref.

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[15]. Generally, the restriction of the parasitic inductances inside the PM including power loop inductance or gate loop inductance leading to reduce the transient voltage/current oscillations and consequently, reduce the conducted EMI noise as addressed in the several papers as in Refs. [1, 16, 17]. As a result, to model and mitigate the emissions, the parasitic inductance of the PM must be accurately characterized.

The basic approaches to characterize the parasitic inductances of the power devices can be divided into two categories in the literature. One category consisting the analytical numerical modeling or calculation based approaches. The closed-form formulas to calculate the partial self-inductances and the mutual inductance of the rectangular cross-section conductors have been proposed in the literature [18-20] and the analytical calculations of some parasitic parameters of PM have been reported in Refs. [21-22]. In Ref. [23] the analytical calculation of the equivalent circuit parameters of large synchronous generator is presented based on winding-function method. Since the direct analytical inductance calculation for more complex modules is not applicable, the major efforts in this category are based on solving Maxwell's equations by finite element analysis (FEA) or partial element equivalent circuit (PEEC) method [15, 24-26]. The well-known ANSYS Q3D extractor software tool is usually used in this category which provides the frequency-dependent parasitic model of the device [27]. This model can be imported to the circuit simulators such as LTSpice, ANSYS Simplorer, etc. and then a frequency-dependent parasitic model-based circuit schematic of the PM for the system time-domain simulation could be constructed as used in Refs. [25, 26]. As a drawback, the exact internal geometry of the module and the material information must be accurately known to calculate the stray inductances and capacitances, while these data are not easily available. Moreover, this approach has disadvantages of poor convergence and long computation time when the physical structure of module becomes more complex. Recently, an improved behavior model for IGBT module is derived by datasheet and measurement in Ref. [28]. The model is used two continuous functions to solve the convergence problem in the circuit simulation.

The second category is the measurement-based approach. The parasitic inductance of the device is determined directly by the measurement. The time-domain reflectometry (TDR) method based on transmission line theory, had been employed to extract the device parasitic elements [29-31]. The method

requires complicated test setup and software thus the adoption is limited in practice. Measuring the parasitic inductance using an impedance analyzer (IA) or a vector network analyzer (VNA) is a straightforward method and brings the frequency domain impedance measurement (Z -parameter) between terminals of the module. A multi-step inductance and structural capacitance extraction method was proposed in Ref. [32] to characterize an IGBT module packaging using an IA. A compact model of a SiC-MOSFET considering the mutual inductance of the leads was presented in Ref. [33]. The measuring accuracy relies on the calibration of the probe impedance, especially for the low inductance measurement. Recently, a custom measurement methodology is proposed that reduces the systematic and stochastic errors by utilizing a particular probe fixture [34]. A characterization technique based on two-port network parameters (S -parameter) using a VNA was introduced in Ref. [35]. This technique includes 5 steps two-port S -parameters measurements for the half-bridge PM and brings more accuracy than conventional one-port measurements. This method is chosen in this paper to extract the model parameters.

In this paper, a detailed model of a commercial half-bridge IGBT module is presented which is useful for EMI simulation. Since, it properly simulates the switching transients. The proposed model is precise and the parameters are extracted by both analytical calculation and measurement methods. It includes the parasitic inductances and resistances of the leads, direct bonded copper (DBC) plates, bond wires, and also the stray capacitances of the module and IGBTs. To calculate the parasitic inductance values, a 3D physical layout of the PM under test is performed. Based on the formulas for calculating the parasitic inductances of the rectangular cross-section conductors and the thin conductors, the precise simplified equations are proposed that bring the partial self-inductance values of one of the module leads and DBC plates. Moreover, the analytical calculation of the parasitic capacitances of the module is driven which. The module geometry is then imported to ANSYS Q3D extractor to calculate all parasitic inductance and capacitance values of the proposed model and consequently, a frequency-dependent multi-port RLC model of the module is attained. Comparing the Q3D results with their calculated values verifies the simulation. The measurement-based parameter extraction of the model is also performed in this paper. The implemented methodology based on the extraction procedure presented in Ref. [35] is described and the measured

results are presented. These values are compared with the Q3D results which show a good agreement. Finally, the proposed model is implemented by Q3D state-space dynamic coupling in ANSYS Simplorer circuit simulator. ANSYS Simplorer’s built-in semiconductor device characterization tool uses the device manufacturer’s datasheet data to characterize the physical model of the IGBT. To clarify the benefits of the proposed model, the switching transient waveforms of the IGBT module under test are evaluated by experiment and the time-domain simulation of the double-pulsed test (DPT) circuit in ANSYS Simplorer. The results show an acceptable match between the simulated and experimental waveforms.

2. PM LAYOUT ANALYSIS

A commercial wire-bonded 1200V 100A half-bridge PM (LUH100G120 from LS company) is selected in this paper to explain the proposed model. Fig. 1(a) shows the geometry of the module which is unpacked for 3D physical modeling and drawn in Solid-Works. The module size is 30mm×90mm×32mm. The selected PM has two IGBTs and two anti-parallel diodes with a half-bridge configuration. They are mounted on two symmetrical DBC substrates. Fig. 1(b) shows the layout of the DBC substrates when the module pins are removed. There are one IGBT chip (11mm×12mm) and one anti-parallel diode chip (8mm×8mm) on each DBC substrate which are mounted on the copper traces. The electrical connections between the traces and two substrates are provided by the multiple aluminum bond-wires. Therefore, the current handling capability is increased, and also the parasitic inductance of the current path is decreased. The module has 3 power pins to prepare the DC+, DC- and AC power terminals, and 2 pairs of control pins (G_1, E_1, G_2, E_2) to provide the Gate-Emitter signal of the IGBTs. The pin dies are shown in Fig. 1(b) with yellow rectangles.

Fig. 1(c) shows the simplified equivalent circuit of the module consisting of the parasitic resistances and inductances of the pins, DBC substrates, the stray capacitances of the switches, and parasitic capacitance of the module. When the PM is used in the half-bridge inverter topology, two power current paths are considered. One path is from the DC+ terminal to the AC terminal which is assigned with red lines in Fig. 1(b) and Fig. 1(c). The current is followed from the DC+ pin and DBC substrates through the traces and bond wires and finally reached to AC pin. The parasitic impedances of this path are shown in Fig. 1(c) which are assumed with four lump inductances $L_{P3}, L_{DC+}, L_{AC+},$ and L_{P1} and

three resistances of the current path $R_{P3}, R_{AC+},$ and R_{P1} . L_{P3} and L_{P1} are the parasitic inductances, and R_{P3} and R_{P1} are the conductive resistance of DC+ and AC pins, respectively. The L_{DC+} and L_{AC+} are the overall parasitic inductances of the current paths within the DBC plates shown in Fig. 1(b) with a red line. As can be seen from Fig. 1(b), this current path is the longest path in DBC substrate. Therefore, R_{AC+} is considered to model the conductive resistance of this path and other resistances in DBC substrates are ignored for simplification. The other current path is from the AC terminal to DC-terminal. This path is shown with blue lines in Fig. 1(b) and Fig. 1(c).

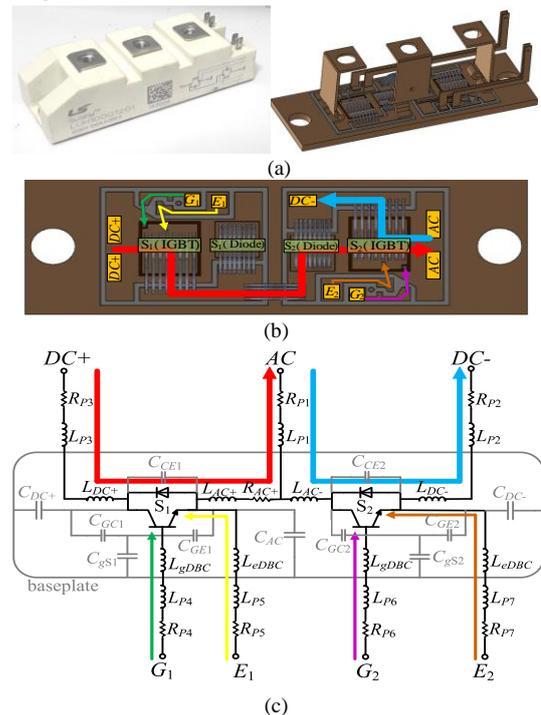


Fig. 1. The selected commercial wire bonded power module (a) Module with its internal structure (b) the layout of the DBC substrate when the module pins are removed with the current and signal paths (c) the module equivalent circuit consist of the parasitic impedances and the current and signal paths

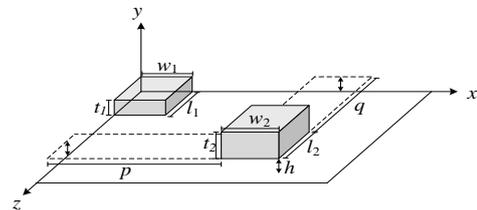


Fig. 2. Three-dimensional description of rectangular conductors

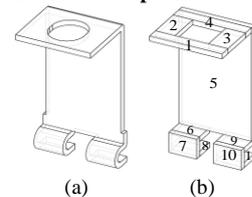


Fig. 3. Simplified geometry of pin 1 to calculated the total partial inductance (a) layout of the pin 1 (b) the considered simplified model with the rectangular parts

The parasitic impedance of this path is modeled with L_{P1} , R_{P1} , L_{AC} , L_{DC} , L_{P2} , and R_{P2} in Fig. 1(c), where L_{P2} and R_{P2} are the parasitic impedances of DC- pin, and L_{AC} and L_{DC} are the overall parasitic inductances of the current paths shown in Fig. 1(b) with a blue line. The parasitic impedances of the IGBT gate-emitter path are modeled with four lump inductances and two resistances, e.g. for S_1 , L_{P4} and L_{P5} are parasitic inductances and R_{P4} and R_{P5} are parasitic resistances of the G_1 and E_1 pins, and L_{gDBC} and L_{eDBC} are the total parasitic inductance of gate and emitter paths in DBC substrate which are shown in Fig. 1(b) with green and yellow lines. The stray capacitances of the IGBT devices are also considered in Fig. 1(c), including C_{CE1} , C_{GC1} , C_{GE1} , C_{CE2} , C_{GC2} , and C_{GE2} . Five capacitances including C_{DC+} , C_{AC} , C_{DC-} , C_{gS1} , and C_{gS2} are the parasitic capacitances of the module. They are present due to the capacitive coupling between DBC copper plates and mounting baseplate which can be connected to the ground, as shown in Fig. 1(c). The other parasitic impedances e.g. the mutual inductances, the capacitance between pins, etc. are ignored in this paper for simplification.

3. THREE-DIMENSIONAL NUMERIC MODELING

3.1. Inductance Calculation

In this section, the theoretical methods to calculate the parasitic inductances of the pins, bond wires, and DBC traces are developed then the well-known ANSYS tool, Q3D Extractor, is used to extract the inductances of the considered equivalent circuit shown in Fig. 1(c). As shown in Fig. 1(a), the pins are the conductors with rectangular cross-sections. The equation is presented in Ref. [20] to calculate the self-partial inductance of the rectangular conductors. For instance, the self-partial inductance of conductor 1, L_{sp1} , shown in Fig. 2 is:

$$\begin{aligned} \frac{L_{sp1}}{l_1} = & \frac{2\mu}{\pi} \left\{ \frac{\omega^2}{24u} \left[\ln\left(\frac{1+A_2}{\omega}\right) - A_5 \right] + \frac{1}{24u\omega} \left[\ln(\omega + A_2) - A_6 \right] \right. \\ & + \frac{\omega^2}{60u} (A_4 - A_3) + \frac{\omega^2}{24} \left[\ln\left(\frac{u+A_3}{\omega}\right) - A_7 \right] + \frac{\omega^2}{60u} (\omega - A_2) \\ & + \frac{1}{20u} (A_2 - A_4) + \frac{u}{4} A_5 - \frac{u^2}{6\omega} \tan^{-1}\left(\frac{\omega}{uA_4}\right) \\ & + \frac{u}{4\omega} A_6 - \frac{\omega}{6} \tan^{-1}\left(\frac{u}{\omega A_4}\right) + \frac{A_7}{4} - \frac{1}{6\omega} \tan^{-1}\left(\frac{u\omega}{A_4}\right) \\ & + \frac{1}{24\omega^2} \left[\ln(u + A_1) - A_7 \right] + \frac{u}{20\omega^2} (A_1 - A_4) \\ & + \frac{1}{60\omega^2 u} (1 - A_2) + \frac{1}{60\omega^2 u} (A_4 - A_1) + \frac{u}{20} (A_3 - A_4) \\ & + \frac{u^3}{24\omega^2} \left[\ln\left(\frac{1+A_1}{u}\right) - A_5 \right] + \frac{u^3}{24\omega} \left[\ln\left(\frac{\omega+A_3}{u}\right) - A_6 \right] \\ & \left. + \frac{u^3}{60\omega^2} \left[(A_4 - A_1) + (u - A_5) \right] \right\} \end{aligned} \quad (1)$$

where $u=l_1/w_1$ and $\omega=t_1/w_1$ are the normalized parameters where w_1 , t_1 , and l_1 are the conductor dimensions, and:

$$\begin{aligned} A_1 = \sqrt{1+u^2}, A_2 = \sqrt{1+\omega^2}, A_3 = \sqrt{u^2+\omega^2}, A_4 = \sqrt{1+u^2+\omega^2} \\ A_5 = \ln\left(\frac{1+A_4}{A_3}\right), A_6 = \ln\left(\frac{\omega+A_4}{A_1}\right), A_7 = \ln\left(\frac{u+A_4}{A_2}\right) \end{aligned}$$

The other equation describing the mutual inductance of the two adjacent rectangular conductors M_{12} , shown in Fig. 2, is presented in Ref. [19], as:

$$M_{12} = \frac{\mu}{4\pi} \frac{1}{t_1 w_1 t_2 w_2} \left[\left[\left[f(x, y, z) \binom{p-w_1}{(p+w_2)} \binom{h-t_1}{(h+t_2)} \binom{q-t_1}{(q+t_2)} \right] \binom{x}{(x)} \binom{y}{(y)} \binom{z}{(z)} \right] \binom{m_1, m_3}{m_2, m_4} \binom{n_1, n_3}{n_2, n_4} \binom{s_1, s_3}{s_2, s_4} \right] \quad (2)$$

where:

$$\left[\left[\left[f(x, y, z) \binom{m_1, m_3}{m_2, m_4} \binom{n_1, n_3}{n_2, n_4} \binom{s_1, s_3}{s_2, s_4} \right] \right] \right] = \sum_{i=1}^4 \sum_{j=1}^4 \sum_{k=1}^4 (-1)^{i+j+k+1} f(m_i, n_j, s_k)$$

and:

$$\begin{aligned} f(x, y, z) = & \left(\frac{y^2 z^2}{4} - \frac{y^4}{24} - \frac{z^4}{24} \right) x \ln \frac{x + \sqrt{x^2 + y^2 + z^2}}{\sqrt{y^2 + z^2}} \\ & + \left(\frac{x^2 z^2}{4} - \frac{x^4}{24} - \frac{z^4}{24} \right) y \ln \frac{y + \sqrt{x^2 + y^2 + z^2}}{\sqrt{x^2 + z^2}} \\ & + \left(\frac{x^2 y^2}{4} - \frac{x^4}{24} - \frac{y^4}{24} \right) z \ln \frac{z + \sqrt{x^2 + y^2 + z^2}}{\sqrt{x^2 + y^2}} \\ & + \frac{1}{60} (x^4 + y^4 + z^4 - 3x^2 y^2 - 3y^2 z^2 - 3x^2 z^2) \sqrt{x^2 + y^2 + z^2} \\ & + \frac{xyz^3}{6} \tan^{-1} \frac{xy}{z\sqrt{x^2 + y^2 + z^2}} + \frac{xy^3z}{6} \tan^{-1} \frac{xz}{y\sqrt{x^2 + y^2 + z^2}} \\ & + \frac{x^3yz}{6} \tan^{-1} \frac{yz}{x\sqrt{x^2 + y^2 + z^2}} \end{aligned}$$

To calculate the inductance of a pin, the pin structure can be simplified as series/parallel connections of the rectangular parts. Fig. 3(a) shows the layout of pin 1 and Fig. 3(b) shows its simplified model with rectangular parts. It is supposed that the current flows from part 1 to the paralleled parts 8 and 11. Ignoring some mutual inductances between parts, the total inductance of this pin L_{P1} can be expressed as:

$$\begin{aligned} L_{P1} = & L_1 + (L_2 \| L_3) + L_4 + L_5 + [(L_6 + L_7 + L_8) \| (L_9 + L_{10} + L_{11})] \\ & \cong L_1 + (L_2 \| L_3) + L_4 + L_5 + [(L_6 \| L_9) + (L_7 \| L_{10}) + (L_8 \| L_{11})] \end{aligned} \quad (3)$$

where L_i is the self-partial inductance of the i -th part and M_{ij} is the mutual inductance between the i -th and j -th part. For mutually coupled inductors in parallel, the total inductance can be obtained from (4):

$$L_T = \frac{L_a L_b - M_{ab}^2}{L_a + L_b + 2M_{ab}} \quad (4)$$

For $L_a = L_b$, it gives:

$$L_T = \frac{L_a L_a - M_{ab}^2}{L_a + L_a + 2M_{ab}} = \frac{1}{2} (L_a + M_{ab}) \quad (5)$$

It can be seen from Fig. 3(b) that $L_2=L_3$, $L_6=L_9$, $L_7=L_{10}$, and $L_8=L_{11}$. Therefore, the inductance of pin 1 from (3) can be rewritten as:

$$\begin{aligned} L_{P1} \cong & L_1 + (L_2 \| L_3) + L_4 + L_5 + [(L_6 \| L_9) + (L_7 \| L_{10}) + (L_8 \| L_{11})] \\ = & L_1 + 0.5(L_2 + |M_{2,3}|) + L_4 + L_5 \\ & + [0.5(L_6 + |M_{6,9}|) + 0.5(L_7 + |M_{7,10}|) + 0.5(L_8 + |M_{8,11}|)] \end{aligned} \quad (6)$$

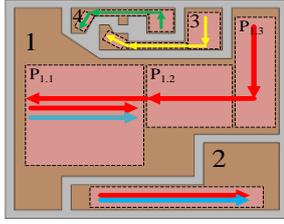


Fig. 4. DBC substrate top view consist of four copper plates and their major current paths

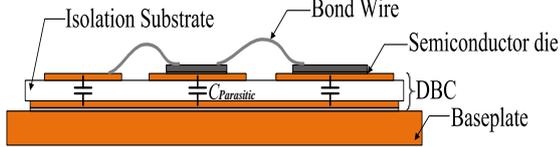


Fig. 5. Schematic showing the parasitic capacitances of an IGBT power module

Table 1. Calculated Inductances Refer to Pin 1

	Dimension (mm)	Inductance (nH)
$L_1 = L_4$	$l = 2, t = 1, w = 13$	0.166
$L_2 = L_3$	$l = 6, t = 1, w = 3.5$	2.008
L_5	$l = 22.5, t = 1, w = 13$	8.577
$L_6 = L_9$	$l = 3.5, t = 1, w = 5$	0.747
$L_7 = L_{10}$	$l = 2, t = 1, w = 5$	0.295
$L_8 = L_{11}$	$l = 3.5, t = 1, w = 5$	0.747
$M_{2,3}$	$p = 9.5, q = 0, h = 0$	0.374
$M_{6,9}$	$p = 8, q = 0, h = 0$	0.161
$M_{7,10}$	$p = 8, q = 0, h = 0$	0.053
$M_{8,11}$	$p = 8, q = 0, h = 0$	0.161
Total Inductance L_{P1} from (6)	-	10.916

Table 2. Calculated Inductances of the DBC Copper Plates

	Dimension of sections ($l \times w$) (mm)	Inductance of sections (nH)	Total Inductance (nH)
Plate 1	P1.1: 12.605 × 12.008	3.839	13.239
	P1.2: 9.187 × 7.445	3.026	
	P1.3: 13.150 × 4.262	6.373	
Plate 2	P2.1: 18.434 × 2.509	11.91	11.91
Plate 3	P3.1: 4.278 × 3.467	1.409	6.875
	P3.2: 6.575 × 0.720	4.524	
	P3.3: 2.341 × 1.215	0.941	
Plate 4	P4.1: 2.642 × 2.657	0.783	5.151
	P4.2: 5.449 × 0.706	3.573	
	P4.3: 2.101 × 1.260	0.794	

The inductances L_i and M_{ij} in (6) can be calculated using (1) and (2), respectively. The MATLAB program is developed to attain L_{P1} from (6), using dimensions of the parts. It should be noted that, to calculate the mutual inductance, the L'opital's rule is used to evaluate the limit of the indeterminate form 0/0 in (2). Table 1 shows the calculated values. For the other pins, similar approaches can be used to obtain the self-partial inductances.

Fig. 4 shows a DBC substrate of the module. It consists of four copper plates which are named from 1 to 4 in the figure. From Fig. 1(b), the main power currents flow from the $DC+$ to AC pins and from the AC to $DC-$ pins through the copper plates which are assigned with the red and blue lines in Fig. 1 and Fig. 4, respectively. The major amount of these currents passes

throughout the pink rectangular sections of the plate 1 and 2 which are shown in Fig. 4. Therefore, to simplify the calculation, only these parts of the plates are considered and the total inductance of one plate is obtained by the sum of the inductances of its sections. Similarly, for the signal pins, the equivalent passes are shown in Fig. 4 in plates 3 and 4 with yellow and green lines, respectively. As the thickness of the plates is relatively low, they can be considered as the thin conductor. From Fig. 2, when $t_1 \approx 0$ the partial self-inductance of a thin conductor is calculated by [19]:

$$\frac{L_{SP}}{l_1} = \frac{\mu_0}{2\pi} \left[\ln(u + \sqrt{u^2 + 1}) + u \ln\left(\frac{1}{u} + \sqrt{\left(\frac{1}{u}\right)^2 + 1}\right) + \frac{1}{3} \left(u^2 + \frac{1}{u} - \frac{(u^2 + 1)^{3/2}}{u} \right) \right] \quad (7)$$

where $u = l_1/w_1$. Table 2 shows calculated self-partial inductances of the DBC copper plates using dimensions.

3.2. Parasitic Capacitance Calculation

The parasitic capacitances of the module should be accurately characterized. Since, they can provide the coupling paths between the system and the common ground. Some of these parasitic capacitances get charged or discharged during the high dv/dt in switching transients which generate the severe current spikes and give rise to the switching losses as well as common-mode EMI issues [36]. Fig. 5 shows the schematic view of the parasitic capacitances. From Fig. 4, there are four copper plates on each DBC substrate of the IGBT module under study. Therefore, four parasitic capacitances can be introduced relative to each copper plate. These capacitors can be estimated based on the planar capacitance equation (8) as:

$$C_{P_i} = \frac{\epsilon_r \epsilon_0 A_i}{d}, \quad i = \{1, 2, 3, 4\} \quad (8)$$

Where ϵ_r is the relative permittivity of the isolation substrate which is 9.8 for Al_2O_3 Ceramic in our module, A_i is the area of i -th copper plate shown in Fig. 4, and d is the distance between copper plates and the baseplate which is 0.635 mm for our module. Four parasitic capacitances C_{P1} , C_{P2} , C_{P3} , and C_{P4} introduced by the plates are presented in Table 3. As can be seen from Fig. 1(b) and Fig. 1(c), the parasitic capacitances of the module are related to plates capacitances as described in (9) based on wire-bonding connections between plates:

$$C_{DC+} = C_{P1}, \quad C_{AC} = C_{P1} \parallel C_{P2} \parallel C_{P3}, \quad C_{DC-} = C_{P2} \parallel C_{P3} \quad (9)$$

$$C_{gS1} = C_{gS2} = C_{P4}$$

The parasitic capacitance values of module and the calculated inductances from Table 1 and Table 2 are compared with the simulated values which are obtained in the following section.

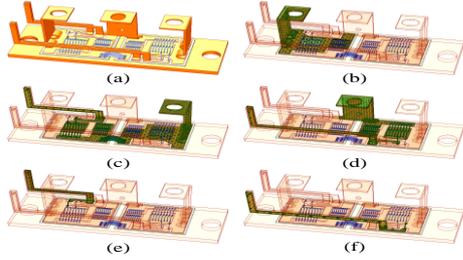


Fig. 6. Power module ANSYS Q3D simulation (a) imported geometry (b) DC+ conducting net (c) AC conducting net (d) DC-conducting net (e) S₁ gate conducting net (f) S₂ gate conducting net

3.3. Software Parasitic Extraction

In this section, the parasitic extraction simulation of the module is performed using well-known software ANSYS Q3D. This software tool calculates *R*, *L*, and *C* matrices by a quasi-static 3D EM solver. The resulted matrices can be used to generate an equivalent circuit model, allowing a circuit-electromagnetic coupled modeling. The Q3D model containing frequency-dependent EM behavior can be linked dynamically to the ANSYS circuit simulator tool, ANSYS Simplorer, for the time-domain simulation. In our case study, the module geometry is drawn and imported in Q3D which is shown in Fig. 6(a). To perform the parasitic extraction simulation, the conducting nets containing proper ports, known as *sink* or *source*, should be assigned [27]. The module is containing four isolated nets. Fig. 6(b) shows the DC+ net which links the DC+ pin to the S₁ collector and the cathode of its parallel diode. The AC and DC-nets are shown in Fig. 6(c) and Fig. 6(d), respectively. Moreover, two other nets are assigned for gate signals of the IGBTs which are shown in Fig. 6(e) and Fig. 6(f). After determining desired nets and their relative *sink* and *source* terminals, the frequency sweep should be performed to calculate the parasitic impedances of the module. The maximum frequency of the frequency sweep should be specified by the rise time of the time domain signal [26]. From the module datasheet values, each IGBT of the module has a rise time of 51 ns. It is assumed that the five samples within the rise time duration are required to fully capture the signal. Therefore, the considered maximum frequency is attained by:

$$F_{max} = \frac{1}{51/5 \text{ ns}} = 100\text{MHz} \tag{10}$$

The simulation is performed using this maximum frequency. The inductance between terminals of a conducting net can be obtained from software. Therefore, the terminals within a net are considered to calculate the parasitic inductances of the module shown in Fig. 1(c). Moreover, the capacitances between nets are also obtained from simulation. In our case study, the parasitic capacitances of the module are consisting the

capacitance between the assigned nets shown in Fig. 6 and the baseplate net. The calculated values of the self-partial inductance of pin 1 from Table 1, the self-partial inductances of the DBC plates from Table 2, and the parasitic capacitances of the module are compared with their simulated values at the frequency of *F*_{max} as shown in Table 4. The maximum absolute difference is below 8% which verifies the simulation results.

Fig. 7 shows the obtained simulation results of the parasitic inductances and resistances of the module over the frequency range. The results are plotted for the inductances and resistances of the equivalent circuit shown in Fig. 1(c). With the values of these impedances, the equivalent lumped circuit of the module can be built and simulated using circuit simulators such as LTSpice, Saber, ANSYS Simplorer, etc. As can be shown from Fig. 7, the resistance values are increased while the inductance values are decreased over the frequency. This is because of the skin effect in high frequencies [19]. The challenge is to specify the frequency of interest to generate the equivalent circuit. In some works, the switching frequency or fall/rise time of the semiconductor device is used [37]. It should be noted that ANSYS provides automatic coupling between the electric and electromagnetic domains in Simplorer as an equivalent circuit or state-space model which preserves the circuit-electromagnetic couple model [27]. Using the state-space model in Simplorer provides the frequency-dependent values of the parasitic parameters. Therefore, the problem of selecting the right modeling frequency can be skipped. In this paper, ANSYS Simplorer is used for test circuit simulation, but before that in the following section, the experimental parasitic inductance extraction based on two-port S-parameter measurements is presented as the measurement verification of the Q3D simulation results.

Table 3. Calculated Parasitic Capacitances of the DBC plates

<i>C</i> _{P1} (pF) (A ₁ =433mm ²)	<i>C</i> _{P2} (pF) (A ₂ =106mm ²)	<i>C</i> _{P3} (pF) (A ₃ =33.25mm ²)	<i>C</i> _{P4} (pF) (A ₄ =26.7mm ²)
59.086	14.464	4.537	3.643

Table 4. Simulation Results of the Self-Partial Inductances and Parasitic Capacitances Compared to the Theoretical Calculations

	Theoretical Calculation	Simulation	Absolute Diff. (%)
Pin 1 Inductance	10.916 nH (Table 1)	10.081 nH	7.64
DBC Inductance	Plate1: 13.239nH (Table 2)	12.785 nH	3.42
	Plate2: 11.910nH (Table 2)	12.329 nH	3.51
	Plate3: 6.875nH (Table 2)	6.988 nH	1.64
	Plate4: 5.151nH (Table 2)	5.041 nH	2.13
Parasitic Capacitance	<i>C</i> _{DC+} = 59.086pF (from (9))	58.256 pF	1.40
	<i>C</i> _{AC} = 77.088pF (from (9))	81.611 pF	5.86
	<i>C</i> _{DC-} = 19.001pF (from (9))	19.511 pF	2.68
	<i>C</i> _{gS1} = 3.643pF (from (9))	3.524 pF	3.26
	<i>C</i> _{gS2} = 3.643pF (from (9))	3.624 pF	0.52

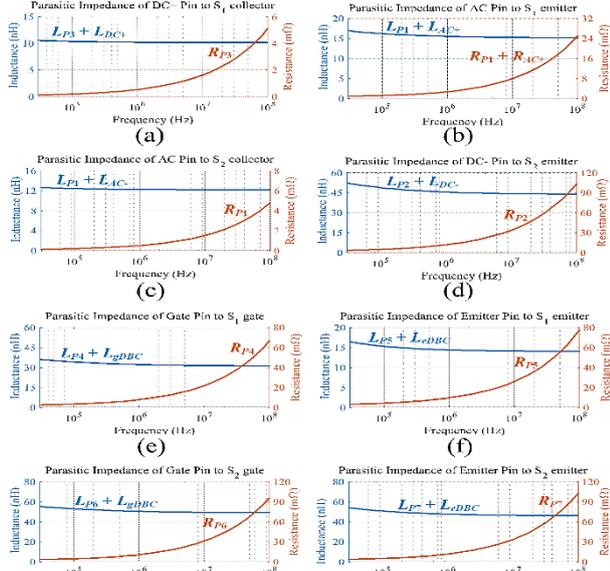


Fig. 7. Q3D extraction results of the parasitic inductances and resistances of the module related to the equivalent circuit shown in Fig. 1(c) over the frequency range

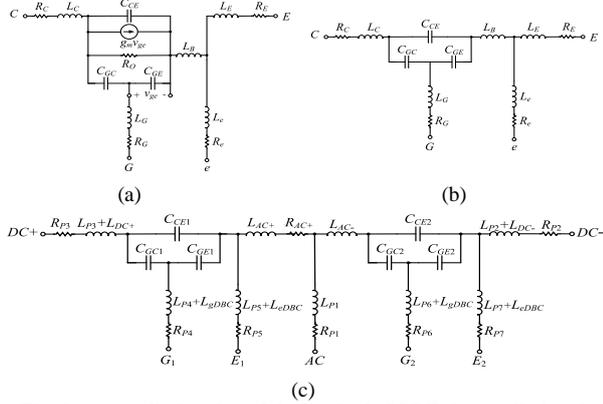


Fig. 8. (a) small-signal model of a single IGBT (b) small-signal model of a single IGBT under zero biasing condition (c) small-signal equivalent circuit of a dual packed IGBT module under zero biasing condition

4. MEASUREMENT-BASED PARASITIC IMPEDANCE EXTRACTION

The methodologies to measure the parasitic impedances of the IGBT/MOSFET modules are presented in the literature. One approach is based on utilizing a VNA which brings Z-parameters of the device under test. From Fig. 1, the module is consisting of seven physical pins which can be considered as the measurement ports. In this paper, an accurate technique presented in Reference [35] is used to characterize the module which prepares only 5 steps two-port VNA measurements to attain all parasitic impedances of the module. The theoretical background and measurement results are presented in the following.

4.1. Two-port Parasitic Extraction Approach

The small-signal model of a single IGBT based on a MOSFET model including emitter signal pin is shown in Fig. 8(a) where the parasitic elements of bone wires

and/or the electric terminals are shown in addition to the intrinsic IGBT itself [38]. The collector current is modeled as gate-emitter voltage-controlled current source $g_m v_{ge}$. The parameters of the model are [35]:

$$g_m = \sqrt{\frac{2k'W I_C}{L}} \quad (11)$$

$$R_o = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{V_A}{I_C} \quad (12)$$

where W and L are the width and length of the MOSFET channel, respectively and V_A denotes the Early voltage. Note that this model is valid only for the operation in the active region. Therefore, under zero biasing condition (i.e. $I_C=0$) the active parameters can be eliminated ($g_m=0$ and $R_o=\infty$). From this treatment, the small-signal equivalent circuit under zero biasing condition is attained as shown in Fig. 8(b). For a dual packed IGBT module, a similar approach yields the small-signal equivalent circuit. Fig. 8(c) shows the model including internal and package parasitic impedances under zero biasing conditions. This model is the same as the model presented in Fig. 1(c). Fig. 9(a) shows the setup configuration to extract the model parameters of a single IGBT equivalent circuit under zero biasing condition using two-port VNA. From the figure, the collector and emitter pins are connected to port 1 and port2, respectively. The gate pin is connected to the ground of the VNA. This two-port network has four Z-parameters Z_{11} , Z_{12} , Z_{21} , and Z_{22} which all are in the form of a second-order RLC circuit with a series combination of the individual inductances, capacitances, and resistances. Therefore, the values of all parasitic impedances can be extracted from the resulted impedance plots of this measurement using impedance fitting methods. Fig. 9(b) shows the magnitude and phase plots of a typical RLC series circuit. The impedance magnitude has its minimum value at the self-resonant frequency (SRF) where the impedance phase is 0° . The resistive component can be determined at this frequency. The low-frequency impedance is dominated by the capacitor while the high-frequency impedance is dominated by the inductor. However, the capacitance and inductance values can be determined using impedance magnitudes at low and high frequencies, respectively. Using this impedance fitting method yields the parameters of the circuit shown in Fig. 9(a). For the capacitors it gives:

$$Z_{11(\text{low})} = \frac{V_1}{I_1} \Big|_{I_2=0} = \frac{X_{C_{GE}}(X_{C_{CE}} + X_{C_{GC}})}{X_{C_{GE}} + X_{C_{GC}} + X_{C_{CE}}} \quad (13)$$

$$Z_{12(\text{low})} = Z_{21(\text{low})} = \frac{V_1}{I_2} \Big|_{I_1=0} = \frac{V_2}{I_1} \Big|_{I_2=0} = \frac{X_{C_{GE}} \times X_{C_{GC}}}{X_{C_{GE}} + X_{C_{GC}} + X_{C_{CE}}} \quad (14)$$

$$Z_{22(\text{low})} = \frac{V_2}{I_2} \Big|_{I_1=0} = \frac{X_{C_{GC}}(X_{C_{CE}} + X_{C_{GE}})}{X_{C_{GE}} + X_{C_{GC}} + X_{C_{CE}}} \quad (15)$$

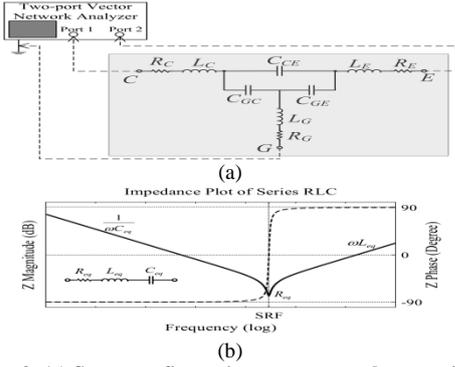


Fig. 9. (a) Setup configuration to measure the parasitic impedances of a discrete IGBT under zero biasing condition via two-port vector network analyzer (b) Magnitude and phase plots of a typical second-order RLC series circuit

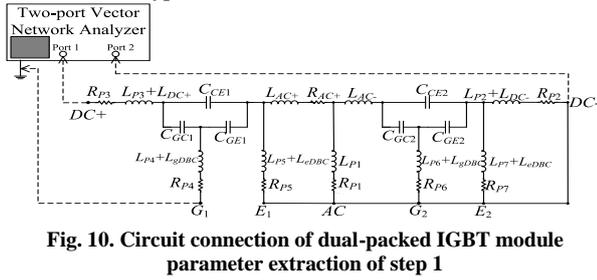


Fig. 10. Circuit connection of dual-packed IGBT module parameter extraction of step 1

Therefore, C_{GS} , C_{GD} , and C_{DS} can be extracted from Eqns. (13) to (15). Similarly, the inductance values and resistance values are extracted using frequency impedance at high frequency and SRF, respectively, as:

$$Z_{11(\text{high})} = \frac{V_1}{I_1} \Big|_{I_2=0} = X_{L_E} + X_{L_G} \quad (16)$$

$$Z_{12(\text{high})} = Z_{21(\text{high})} = \frac{V_1}{I_2} \Big|_{I_1=0} = \frac{V_2}{I_1} \Big|_{I_2=0} = X_{L_G} \quad (17)$$

$$Z_{22(\text{high})} = \frac{V_2}{I_2} \Big|_{I_1=0} = X_{L_C} + X_{L_G} \quad (18)$$

$$Z_{11(\text{SRF})} = \frac{V_1}{I_1} \Big|_{I_2=0} = X_{R_E} + X_{R_G} \quad (19)$$

$$Z_{12(\text{SRF})} = Z_{21(\text{SRF})} = \frac{V_1}{I_2} \Big|_{I_1=0} = \frac{V_2}{I_1} \Big|_{I_2=0} = X_{R_G} \quad (20)$$

$$Z_{22(\text{SRF})} = \frac{V_2}{I_2} \Big|_{I_1=0} = X_{R_C} + X_{R_G} \quad (21)$$

It should be noted that two-port VNA yields S -parameters instead of Z -parameters. For each frequency the conversion between S -parameters to Z -parameters is done using Eqns. (22) to (25):

$$Z_{11} = \left[\frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \right] Z_0 \quad (22)$$

$$Z_{12} = \left[\frac{2S_{12}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \right] Z_0 \quad (23)$$

$$Z_{21} = \left[\frac{2S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \right] Z_0 \quad (24)$$

$$Z_{22} = \left[\frac{(1 + S_{22})(1 - S_{11}) + S_{12}S_{21}}{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}} \right] Z_0 \quad (25)$$

where Z_0 is the reference impedance (50Ω). In summary, for discrete devices after measuring the S -parameters and converting to Z -parameters, the value of parasitic impedances shown in Fig. 9(a) are extracted from Eqns. (16) to (21). Similarly, for dual packed IGBT device a characterization technique is proposed in Ref. [35]. We adopted this technique to extract the parameters of our model shown in Fig. 8(c). The extraction is consisting of 5 step measurements as the following:

Step 1: Port 1 of the VNA includes the terminal $DC+$, Port 2 of the VNA is consisting the terminals $DC-$, E_2 , G_2 , AC , and E_1 together, while the ground port of VNA is connected to terminal G_1 . The inductances $L_{p3}+L_{DC+}$ and $L_{p4}+L_{gDBC}$ and the capacitances C_{CE1} , C_{GC1} , and C_{GE1} are extracted in this step as shown in Fig. 10.

Step 2: Port 1 of the VNA includes the terminal $DC+$ and G_1 together, Port 2 of the VNA is consisting the terminal $DC-$, E_2 , G_2 , and AC together, while the ground port of VNA is connected to terminal E_1 . The inductance $L_{p5}+L_{eDBC}$ is extracted in this step.

Step 3: Port 1 of the VNA includes the terminal $DC+$, G_1 , and E_1 together, Port 2 of the VNA is consisting the terminal $DC-$, E_2 , and G_2 together, while the ground port of VNA is connected to terminal AC . The inductances $L_{p1}+L_{AC+}$ and $L_{p1}+L_{AC-}$ are extracted in this step.

Step 4: Port 1 of the VNA includes the terminal $DC+$, G_1 , E_1 , and AC together, Port 2 of the VNA is consisting the terminal $DC-$ and E_2 together, while the ground port of VNA is connected to terminal G_2 . The inductance $L_{p6}+L_{gDBC}$ and the capacitances C_{CE2} , C_{GC2} , and C_{GE2} are extracted in this step.

Step 5: Port 1 of the VNA includes the terminal $DC+$, G_1 , E_1 , AC , and G_2 together, Port 2 of the VNA is consisting the terminal $DC-$, while the ground port of VNA is connected to terminal E_2 . The inductances $L_{p2}+L_{DC-}$ and $L_{p7}+L_{eDBC}$ are extracted in this step.

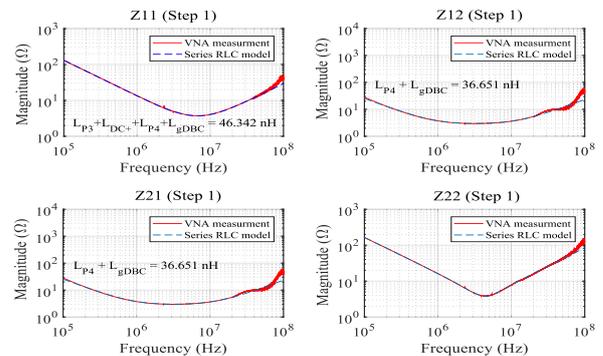


Fig. 11. Converted Z -parameters of the experimental measurements with their series RLC model in step1, the result inductances are $L_{p4}+L_{gDBC} = 36.651$ nH and $L_{p3}+L_{DC+} = 9.691$ nH

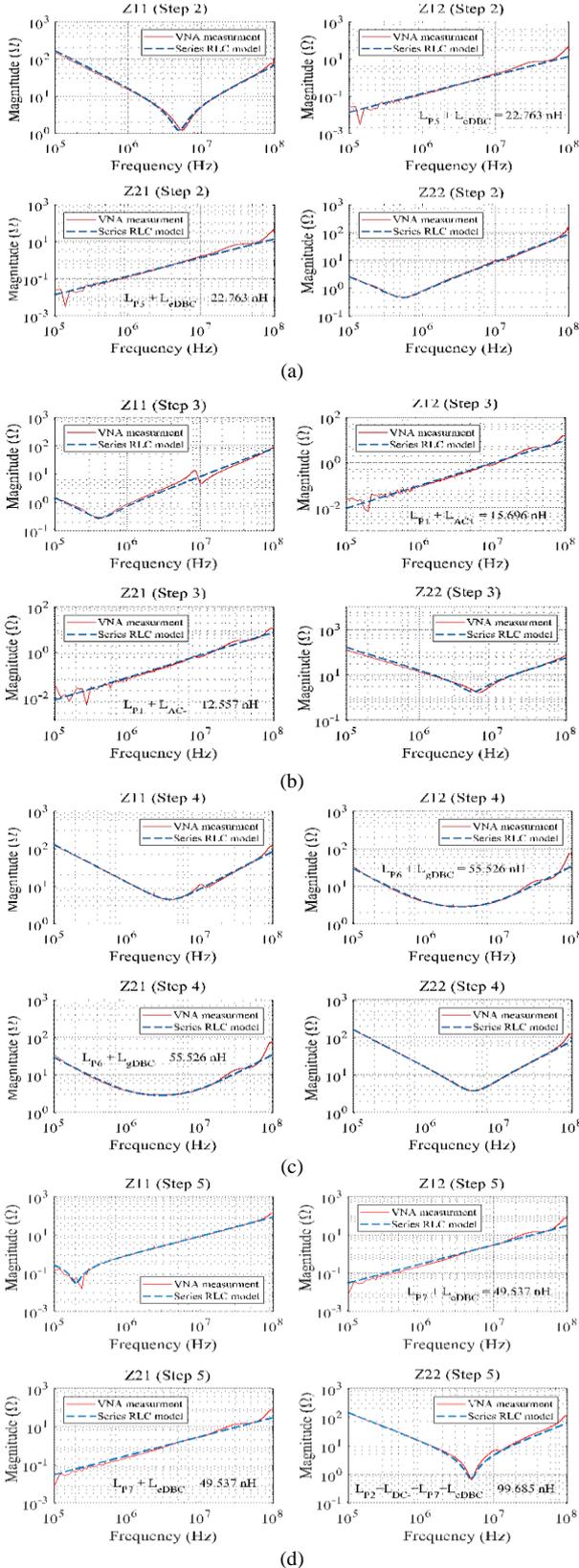


Fig. 12. Converted Z-parameters of the experimental measurements with their series RLC model in (a) step2, the result inductance is $L_{P5}+L_{gDBC} = 22.763$ nH (b) step 3, the result inductances are $L_{P1}+L_{AC+} = 15.696$ nH and $L_{P1}+L_{AC-} = 12.557$ nH (c) step4, the result inductance is $L_{P6}+L_{gDBC} = 55.526$ nH (d) step5, the result inductances are $L_{P7}+L_{gDBC} = 49.537$ nH and $L_{P2}+L_{DC-} = 50.148$ nH

Table 5. Experimental Measurements Compared to the Simulation Results

Inductances	Measured (nH)	simulation (nH)	Absolute Difference
$L_{P4}+L_{gDBC}$	36.651	35.963	1.8%
$L_{P3}+L_{DC+}$	9.691	10.572	9%
$L_{P5}+L_{gDBC}$	22.763	16.481	27.5%
$L_{P1}+L_{AC+}$	15.696	16.937	7.9%
$L_{P1}+L_{AC-}$	12.557	12.653	0.7%
$L_{P6}+L_{gDBC}$	55.526	55.507	0.03%
$L_{P7}+L_{gDBC}$	49.537	53.881	8.7%
$L_{P2}+L_{DC-}$	50.148	52.571	4.8%

Table 6. Measured Capacitances of the Module

Step of Measurement	Step 1			Step 4		
Capacitances	C_{GE1}	C_{GC1}	C_{CE1}	C_{GE2}	C_{GC2}	C_{CE2}
Measured (nF)	9.649	7.560	2.944	9.827	7.587	3.092

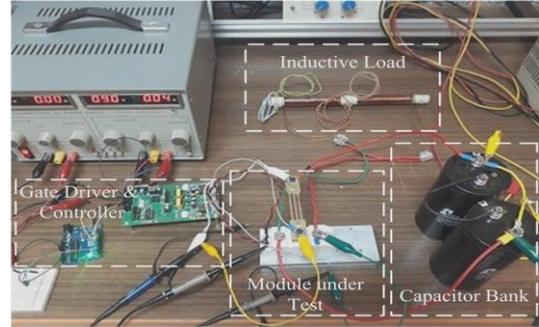
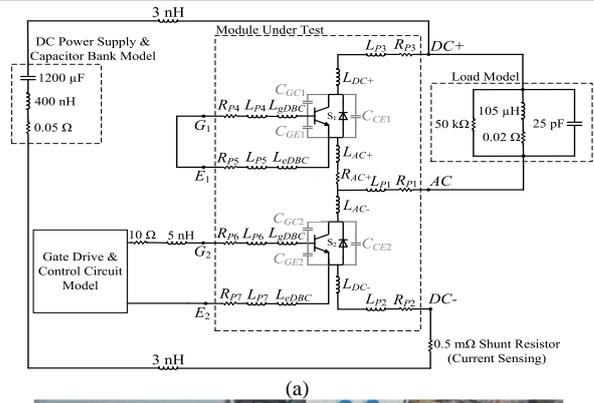


Fig. 13. (a) Schematic circuit diagram of the module under double-pulse test (b) Fabricated laboratory test setup

The measurements are done for our case study in all steps using two-port measurement with the Agilent N9917A-210 vector network analyzer and the resulted S-parameters are converted to the Z-parameters. It should be noted that, measuring impedance, especially for low impedance measurement, is sensitive to the probe impedance, device calibration, etc. In our measurement the VNA and its probes are calibrated using Agilent standard mechanical short-open-load calibration kit. Fig. 11 shows the converted Z-parameters of step 1 with their related RLC series model. Based on above discussion, the result inductances are $L_{P4}+L_{gDBC} = 36.651$ nH and $L_{P3}+L_{DC+} = 9.691$ nH in this step. These measured values can be compared with the extracted values from the Q3D simulation shown in Fig. 7 at low frequency. From Fig.

7(e) $L_{P4}+L_{gDBC} = 35.963$ nH and from Fig. 7(a) $L_{P3}+L_{DC+} = 10.572$ nH which are relatively close to their measured values. Fig. 12 shows the converted Z-parameters of the measurements in step 2 to step 5 with their series RLC model. The result inductances of each step are calculated from the fitted RLC model and written in the figure. The comparison between the measured inductances and the simulated ones are illustrated in Table 5. Except for one inductance ($L_{P5}+L_{eDBC}$, it may be caused by some unwanted measurement errors), others have an absolute difference below 10% which shows the good accuracy of the simulation results presented in section 3.2. In other words, the inductance values shown in Table 5 are the experimental verification of the simulation results shown in Fig. 7. Table 6 represents the measured capacitances in step 1 and step 4. Since two IGBT chipsets in the module are the same, the measured capacitances are closed to each other. This verifies the measurement results.

5. DOUBLED-PLUS TEST VALIDATION OF THE MODEL

The dynamic performance of the model is verified by an inductive load double-pulse test measurement. Fig. 13(a) shows the schematic circuit diagram of the measurement setup. The module under test is marked with a dashed line box. The gate-emitter pins of the low side IGBT are connected to the driver and control circuit to be pulsed, while the gate-emitter pins of the high side IGBT are short-circuited. The double-plus-switching test is done in a range of collector current of about 40A with an inductive load. The inductive load is a hand-made air-core inductor. The equivalent circuit of this load is constructed with a parallel LCR model based on the measured impedance data. The impedance model of the DC link capacitor bank and power supply is also given based on the measured impedance data in the form of a series LCR model which includes the stray inductance of the DC power supply. Two small inductances of 3 nH are considered as the stray inductances of the wires. The resistance of 10 Ω is the outer gate resistance, and the inductance of 5 nH is the inductance of the wiring between the gate driver board and the module signal pins. To capture collector current, a shunt-resistor 150A-75mV is connected in series between the capacitors and the module under test. Fig. 13(b) shows fabricated laboratory test setup. The control signals are prepared by a micro-controller board. All parts of measuring setup are assigned in the figure. The experiments are done by discharging charged capacitor bank (around 500v DC) to an air-core inductor.

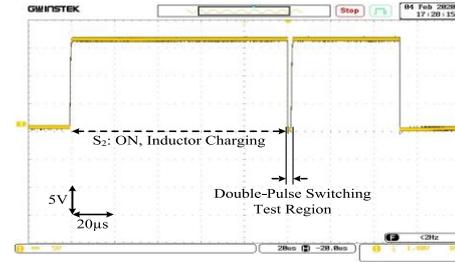


Fig. 14. Implemented gate-emitter signal of low-side IGBT of the module under test

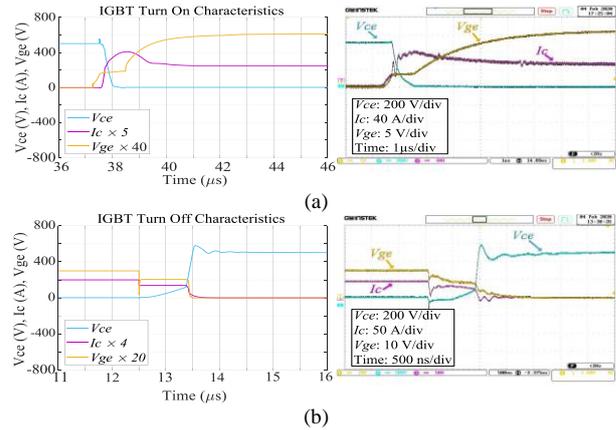


Fig. 15. Transient waveform characteristics of the IGBT under double-pulse test (a) Turn-on characteristics, left: Simplorer simulation result and right: experimental result (b) Turn-off characteristics, left: Simplorer simulation result and right: experimental result

Fig. 14 shows the implemented gate-emitter signal of the low-side IGBT of the module under test. In the first section, the stored energies in capacitors are transferred to the inductor by turning on the IGBT S_2 , which causes the inductor to be charged and its current goes up. When the inductor current reaches a certain value (around 50A in our experiment), the characteristics of the IGBT under test are attained by double-pulse switching of S_2 . To compare the transient response of the module during switching turn-on and turn-off, ANSYS Simplorer simulations are performed. A frequency-dependent model of the module packaging described in section 3 is imported to Simplorer from Q3D Extractor as Q3D state-space dynamic coupling. It provides the frequency-dependent values of the parasitic parameters. Therefore, the problem of selecting the right modeling frequency is skipped. ANSYS Simplorer's built-in semiconductor device characterization tool uses the device manufacturer's datasheet data to characterize the physical model of the IGBT. This tool offers three different IGBT models: Average IGBT, Basic Dynamic IGBT, and Advanced Dynamic IGBT [27]. The Advanced Dynamic model is selected in this work since it includes the modeling of a tail current in IGBT turn-off and the effects of different input capacitances [39]. Fig. 15 shows the transient waveform characteristics of the module from simulation and measurement. From

Fig. 15(a), the simulated turn-on waveforms of V_{ce} is closed to its measured waveform. The turn-on delay times are obtained 102 ns and 93 ns from simulation and experiment, respectively. The rise time of both simulation and experiment is around 50 ns. Fig. 15(b) shows the turn-off characteristics of the module. The waveforms show good agreement between simulation and experiment in both transient and steady-state. The calculated turn-off delay times are 763 ns and 796 ns from simulation and experimental results, respectively.

6. CONCLUSIONS

This paper has presented a detailed model for a half-bridge IGBT power module. The model was consisting of the parasitic inductances of the leads, direct bonded copper (DBC) plates, bond wires, and also the parasitic capacitances of the module and stray capacitances of IGBTs. Based on the formulas for calculating the parasitic inductances of the rectangular cross-section conductors and the thin conductors, the simplified equations have been proposed that bring the partial self-inductance values of one of the module leads and DBC plates. Moreover, the parasitic capacitances of the module are calculated by planar capacitance equations. The module geometry was then imported to ANSYS Q3D extractor to calculate all parasitic parameters of the proposed model and consequently, a frequency-dependent multi-port RLC model of the module was attained. Comparing the Q3D results with their calculated values has shown a maximum difference below 8%. The measurement-based parameter extraction of the model was also performed in this paper. The implemented methodology is based on the extraction procedure presented in Ref. [35]. The method was introduced and the measured results were presented. These values are compared with the Q3D results. Except for one inductance ($L_{P5}+L_{eDBC}$, which may be caused by some unwanted measurement errors), others had an absolute difference below 10% which showed good accuracy. Finally, the proposed model was implemented by state-space dynamic coupling in ANSYS Simplorer circuit simulator. To clarify the benefits of the proposed model, the switching transient waveforms of the IGBT module under test were evaluated by experiment and the time-domain simulation in a double-pulse test circuit. The turn-on delay times, rise time and turn-off delay times had been evaluated in both simulation and experiment, which were close to each other. By comparing the current and voltage waveforms with experiment, it is proved that the proposed model is applicable to simulate the switching transients, and can be used in converter EMI simulation.

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