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Research Paper

A Topology of Non-Isolated Soft Switched DC-DC Converter for Renewable Energy Applications

Nasim Bagheri[*, 1], *Behrouz Tousi*[1], *and Saed Mahmoud Alilou*[2]

[1] *Faculty of Electrical and Computer Engineering, Urmia University, Urmia, Iran.*
[2] *Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran.*

Abstract— *This research offers a high step-up DC-DC converter using a two- winding coupled inductor and voltage multiplier circuit (VMC) including diodes and capacitors for renewable energy (RE) usages such as photovoltaic (PV) and fuel cell (FC). The advantages of this converter are: 1) High voltage gain with small duty cycle of the switch, 2) low voltage stress across switch/diodes, 3) Low number of components, 4) Lower volume and cost, 5) simple structure with only one power switch, 6) small current ripple of the input, 7) zero voltage and current (ZVS and ZCS) of the diodes, 8) improved efficiency, and 9) common grounding of the input and output. Due to the coupled inductor usage, the voltage gain is more flexible, and it can be enhanced by adjusting two different parameters: the turns ratio (N) of the coupled inductor and the duty cycle (D) of the switch. Furthermore, the voltage stresses of the semiconductors are decreased by increasing N. VMC is the other element for the power switch's voltage stress reduction. The suggested topology could be an appropriate option for RE usage because of the small current ripple of the input and modified efficiency.*

Keywords—Renewable energy, DC-DC converter, high step-up, non-isolated, coupled inductor, soft switching.

NOMENCLATURE

C_1	VMC capacitor
C_2	VMC capacitor
C_3	VMC capacitor
C_o	Output capacitor
D_1	VMC diode
D_2	VMC diode
D_o	Output diode
I_o	The current of output port
L_k	Leakage inductance
L_m	Magnetizing inductance
L_{in}	Input inductor
P_{out}	Load power
R_o	The load of output port
V_C	The capacitor voltage
V_D	Current of low voltage port
V_o	The voltage of output port
V_s	The voltage of switch
$V_{Forward}$	Forward voltage of diodes
V_{Lin}	The voltage of inductor L_{in}
V_{Lm}	The voltage of inductor L_m
V_{high}	Voltage of high voltage port
ΔP	Total loss of proposed converter
$\Delta P^{Conduction}$	Conduction loss of switches
$\Delta P^{Switching}$	Switching loss of switch
i_C	The capacitor current
i_D	Current of diode
i_S	The switch's current
i_{Lin}	The inductor L_{in} current
i_{Lm}	The inductor L_m current
r_{DS-on}	On-state resistance of switch
t_r	Rise time
f_s	Switching frequency
t_f	Fall time
D	Duty cycle
ESR	Equivalent series resistance
N	Turns ratio number
RMS	Root mean square
S	Power switch

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*Corresponding author:
E-mail: bagherinasim@yahoo.com (N. Bagheri)
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1. INTRODUCTION

Renewable energy (RE) resources have provided new perspectives for science and industry [1, 2]. The increase in air pollution and global warming as well as the reduction of fuel cell resources, have led humanity to use green energies, such as wind energy, PV, etc. The use of power electronics has been essentially applicable to using these types of energy resources. PV systems are vital sources that have been used extensively in recent years [3]. PVs have solved various obstacles such as climate change, global warming, air pollution, and other related environmental concerns [4]. RE technologies are identified as the most desirable alternative to fossil fuels. PV and FC are the two primary RE sources [5]. Nonetheless, the voltage of RE

sources is extremely low and variable and cannot be connected to the load. Consequently, the high step-up converters should be utilized to enhance the DC voltage of these sources [6]. Due to static voltage gain and simple structure, the conventional high-gain DC-DC topology could be a suitable option. This topology can be used to produce high voltage gain with a high-duty cycle [7]. Despite this, this topology includes drawbacks like electromagnetic interference (EMI) problems, diode reverse-recovery problems, and high-power losses [8]. Also, it suffers from high peak voltages across the semiconductors. Therefore, high-rated semiconductors are needed, which intensifies the switching losses [9]. Additionally, the maximum gain of this converter is five [10]. The quadratic boost structure is another option, which uses only one switch. The output voltage of this topology has a quadratic relation with the output voltage of the traditional boost structure. The normalized peak voltage of its switch is equal to one [11, 12]. Therefore, a high-voltage power switch should be selected. The coupled inductor-based topologies are suitable alternatives for obtaining a high output voltage by modifying the turns ratio [13, 14]. Nevertheless, the leakage inductance of the coupled inductor tends to high voltage spike on the power switch and a higher loss. The switched-capacitor (SC) method can be utilized for obtaining high output voltage. But, in such structures, various power switches are applied. Some benefits of these topologies are high voltage gain, a small input current ripple, and reduced peak voltage across the switch. Using the switched-inductor /capacitor/ active network, a high voltage gain DC-DC converter is suggested in [15]. This topology has two high losses MOSFETs. Also, it presents a high voltage gain with reduced peak voltages. In [16], a non-isolated structure based on VMC is presented. The benefits of this structure are high voltage gain, reduced voltage stresses of the semiconductors, high efficiency, and small input current ripple. In [17], a boost topology is recommended. This structure uses one power switch. In [18], a buck-boost structure with three switches is suggested. The voltage stress of the switch is equal to the output voltage. So, it isn't suitable for high-voltage usage. The other disadvantages of this converter are high losses. In [19], a buck-boost topology consisting of K-Y and traditional step-down topology with two power MOSFET is suggested. It also has high power losses and low efficiency. In [20], a high-voltage multi-phase non-isolated topology is recommended. This converter benefits from low voltage stress and reduced losses. In [21], a high voltage gain non-isolated topology with two power switches is suggested. This topology uses the switched-inductor and switched-capacitor. In [22], based on the Cockcroft-Walton VM, a high-voltage gain converter is recommended which employs two high-rated power switches and diodes. A coupled-inductor-based ultra-step-up DC-DC converter using the interleaved technique and having soft-switching capability is introduced in [23]. This structure utilizes a larger number of components and it does not share a common ground between the input and output ports. The converter based on a coupled-inductor and voltage multiplier cell is given in [24] in which the voltage gain is not considerable. Another high voltage gain DC-DC converter is presented in [25] which utilizes high component counts especially the passive elements. This case leads to an increase in the volume and size of the converter.

In this article, a non-isolated DC-DC converter is proposed for RE usages such as PV and FC by utilizing a coupled inductor and VMC. The voltage gain of this topology is flexible and it can be enhanced by adjusting the coupled inductor turns ratio (N). On the other hand, the voltage stress of the switch is reduced by increasing N. The significant advantages of the suggested converter are as follows:

1- High voltage gain, 2- Reduced peak voltage on semiconductors, 3- Input current with small ripple, 4- Soft switching including ZVS and ZCS, 5- High efficiency, 6- Low components count, and 7- common grounding of the input and output. To show the enactment of the suggested structure, the steady-state, operational modes, and efficiency study, along with a comparison assessment with further works are provided. Also, a laboratory scale of the converter is built to verify the reality of the mathematical examination. The remainder of the paper is arranged as follows:

Section 2) Recommended converter's topology and operation modes, Section 3) Steady-state study, Section 4) Design of the capacitors and inductors, Section 5) Coupled inductor design, Section 6) Efficiency investigation, Section 7) Comparison with other similar topologies, Section 8) Experimental results, Section 9) Conclusion.

2. RECOMMENDED CONVERTER'S STRUCTURE AND OPERATIONAL MODES

The schematic of the presented topology is demonstrated in Fig. 1. One MOSFET (S), three power diodes (D_1, D_2, and D_o), four capacitors ($C_1 \sim C_0$), and two magnetic cores (L_{in} and coupled inductor) are included in this converter. The used coupled inductor consists of two winding (n_1 and n_2). Also, the coupled inductor is modeled as an ideal transformer with a turns ratio equal to N=n_2/n_1, magnetizing (L_m), and leakage (L_k) inductances. Due to the series connection of L_{in} with input voltage V_{in}, the input current ripple is low which is proper for RE usage. Diode D_1 and capacitor C_1 form the passive voltage clamp and decrease the peak voltage of S. D_2 is the regenerative diode, C_1 and C_3 are the voltage multiplier capacitors, D_o and C_o, and R_o are the output diode, capacitor, and load resistance, respectively. S_o, the presented converter has 10 components. The voltage and current waveforms are pictured in Fig. 2. There are three modes in each period (T_s=1/f_s). One mode occurs in the ON-state of S and two modes are related to the OFF-state of S. In the rest of this section, the operation modes are analyzed.

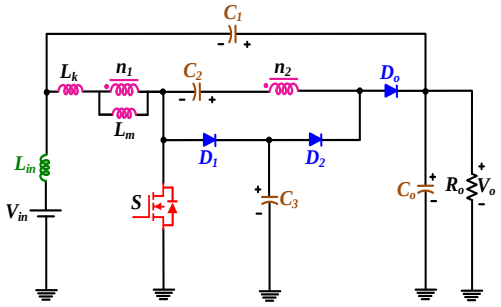


Fig. 1. The schematic of the suggested topology.

Mode 1: At the start of this mode, S is turned ON by applying the gate PWM pulse. L_{in} and the primary side of the coupled inductor are charged by V_{in}. Thus, i_{Lin} and i_{Lm} are increased linearly. D_1 and D_o are reverse biased and only D_2 is directly biased. It is noticeable that, at $t = t_0$, D_2 is turned ON at the ZVS situation. C_2 is charged by the coupled inductor secondary winding and D_3 by diode D_2. Capacitor C_o is discharged to C_1 and R_o. The equivalent circuit of this mode is illustrated in Fig. 3-(a). The following relations are obtained in mode 1:

$$V_{L_{in}} + V_{L_m} + V_{L_k} = V_{in}, \tag{1}$$

$$V_o = V_{in} + V_{C_1} - V_{L_{in}}, \tag{2}$$

$$i_{L_k} = i_{C_1} + i_{in},, \tag{3}$$

$$i_S = i_{L_k} + i_{C_2}, \tag{4}$$

$$i_{C_3} = -i_{D_2} = -i_{C_2}, \tag{5}$$

$$i_{C_o} = -\left(i_o + i_{C_1}\right). \tag{6}$$

Mode 2: At $t = t_1$, S is turned OFF. D_1 and D_o are directly biased and D_2 is turned OFF. At this time, D_o is tuned ON at ZVS situation. L_{in} and L_m are demagnetizing and their current is decreased linearly. The energy stored in C_2, C_1, and the secondary side of the coupled inductor is completely transmitted to R_o. Also, C_3 is charged by the primary side of the coupled inductor. This mode finishes when D_1 is reverse-biased in the ZCS situation. Because of the ZCS turning OFF, the reverse recovery of D_1 is diminished. The schematic circuit of mode 2 is illustrated in Fig. 3-(b). Relations (7)-(11) are determined in this mode:

$$V_{L_{in}} + V_{L_m} + V_{L_k} = V_{in} - V_{C_3}, \tag{7}$$

$$V_o = V_{C_3} + V_{C_2} - V_{n_2}, \tag{8}$$

$$i_{in} = i_{L_k} - i_{C_1}, \tag{9}$$

$$i_{L_k} = i_{D_1} - i_{C2} == i_{C3} - i_{C2}, \tag{10}$$

$$i_{D_o} + i_{C_1} = i_o + i_{C_o}. \tag{11}$$

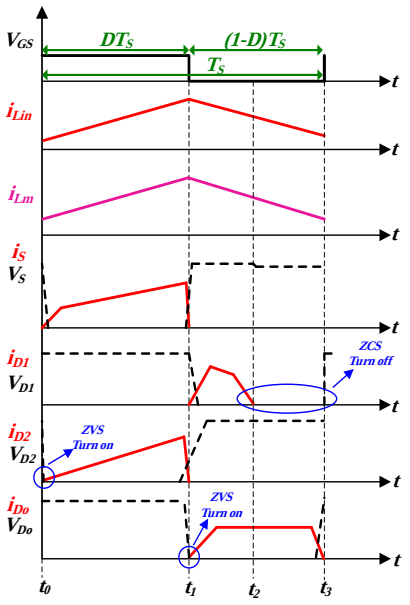


Fig. 2. The main waveforms of the suggested topology.

Mode 3: During this mode, only diode D_o is turned ON and the remainder of the switch/diodes are turned OFF. Because in one mode of each T_s, only one semiconductor is conducted, the conduction loss of the presented converter is reduced and the efficiency is improved. The currents of L_{in} and L_m are still decreased. Thus, according to the transformer currents low, the current of the secondary side of the coupled inductor is increased. Additionally, capacitors C_1 and C_2 are discharged. However, C_o is charged and the current of C_3 is constant. The configuration of this mode is shown in Fig. 3-(c), and the subsequent equation is acquired:

$$i_{C_2} = -i_{L_k} = -i_{D_o}. \tag{12}$$

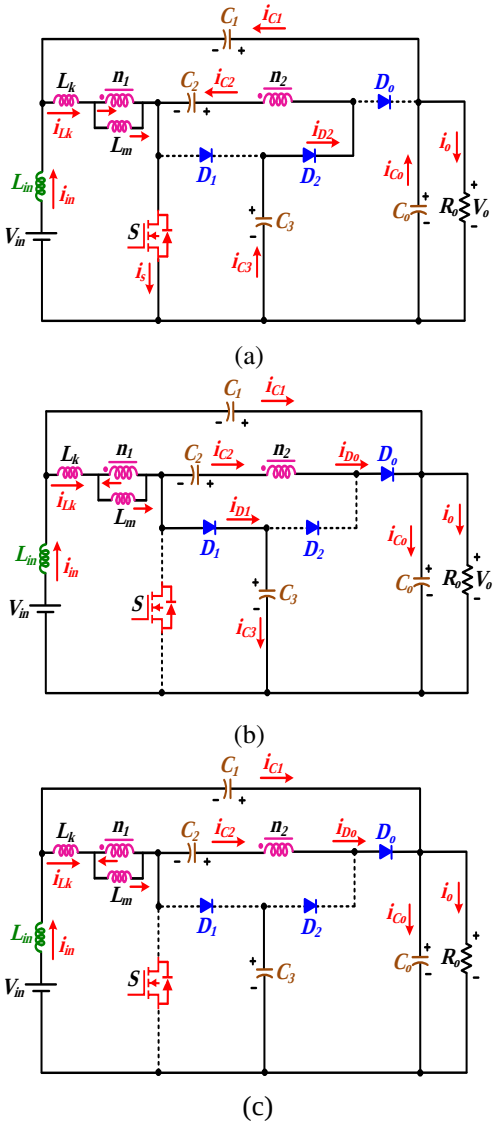


Fig. 3. The equivalent circuit of the proposed converter in each mode, (a) Mode 1, (b) Mode 2, and (c) Mode 3.

3. Steady-State Study

This part introduces the steady-state investigation of the presented topology. In this regard, the voltage gain, voltage, and current calculation. The following hypotheses are used for the simplification of the analysis:

1) Entire semiconductor elements are ideal and lossless,
2) V_{in} and the voltage of all capacitors are steady and invariable,
3) The leakage inductance (L_k) of the coupled inductor is ignored.

3.1. Voltage gain (M)

Using the volt-second balance law for L_{in} and L_m, the following equations for capacitor voltages can be expressed:

$$V_{C_3} = \frac{1}{1-D} V_{in}. \tag{13}$$

Considering the circuit of mode 1, V_{C2} is obtained:

$$V_{C_2} = NV_{in} + V_{C_3} = \frac{(1-D)N+1}{1-D} V_{in}. \tag{14}$$

Also, V_{C1} is calculated as follows:

$$V_{C_1} = V_{C_2} - (1+N)\, V_{L_m} = V_{C_2} + \frac{(1+N)D}{1-D} V_{in} = \frac{D+N+1}{1-D} V_{in}. \tag{15}$$

Finally, the output voltage and voltage gain (M) are achieved versus input voltage, duty cycle, and turns ratio as Eq. (16):

$$V_o = V_{C_1} + V_{in} = \frac{N+2}{1-D} V_{in} \quad \Rightarrow \quad M = \frac{V_o}{V_{in}} = \frac{N+2}{1-D}. \tag{16}$$

3.2. Voltage stress

The blocking voltage of diode D_1 can be calculated at mode 1 during its OFF state:

$$V_{D_1} = V_{C_3} = \frac{1}{1-D} V_{in} \quad \Rightarrow \quad \frac{V_{D_1}}{V_o} = \frac{1}{N+2}. \tag{17}$$

The peak voltages of D_2 and D_o are achieved as:

$$V_{L_{in}} + V_{L_m} + V_{L_k} = V_{in}, \tag{18}$$

$$V_{D_2} = -V_{C_3} + V_o = \frac{N+1}{1-D} V_{in} \quad \Rightarrow \quad \frac{V_{D_2}}{V_o} = \frac{N+1}{N+2}. \tag{19}$$

According to Eqs. (18) and (19), the peak voltages of D_2 and D_o are equal. The maximum peak voltage on switch S is obtained at mode 2, which is equal to V_{D1}:

$$V_{SW} = V_{D_1} = V_{C_3} = \frac{1}{1-D} V_{in} \quad \Rightarrow \quad \frac{V_{SW}}{V_o} = \frac{1}{N+2}. \tag{20}$$

Figs. 4-(a) and 4-(b) depict the voltage gain (M) and voltage stresses versus D and N. The voltage gain is improved with rising D and N. Hence, the voltage gain can be modified by two independent parameters. The normalized peak voltage of S and D_1 is reduced by increasing N.

3.3. Current stress

The currents of the used components are determined according to the equations of section 2. The diodes' average current is identical to I_o.

$$I_{D_1} = I_{D_2} = I_{D_3} = I_{D_o} = I_o, \tag{21}$$

$$i_{D_1} = \frac{(2N+1)\, I_o}{1-D}, \tag{22}$$

$$i_{D_2} = \frac{I_o}{D}, \tag{23}$$

$$i_{D_o} = \frac{I_o}{1-D}. \tag{24}$$

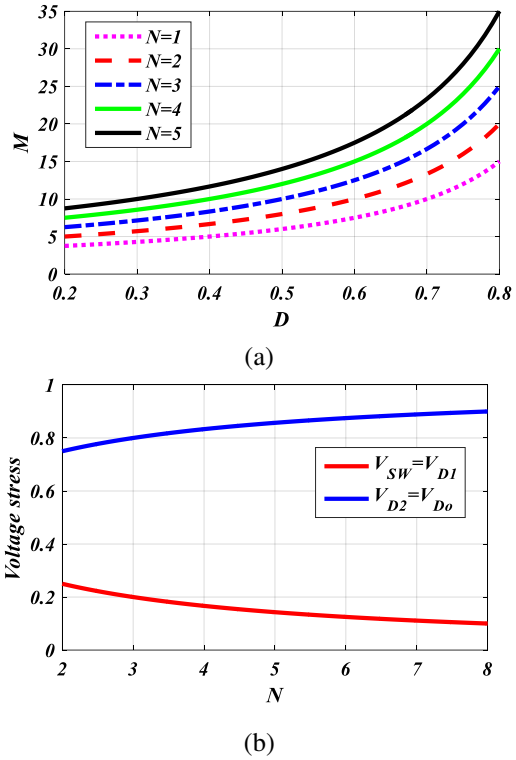


Fig. 4. The voltage gain (M) and voltages stress study, (a) M in terms of D and N, (b) Voltage stresses in terms of N and D=0.6.

Considering Fig. 1, the average current of the input port and magnetizing current are equal:

$$I_{L_m} = I_{in} = \frac{N+2}{1-D} I_o. \tag{25}$$

The average current of S is as Eq. (26):

$$I_{SW} = \left(\frac{N+2}{1-D} - 1\right) I_o = \frac{N+D+1}{1-D} I_o. \tag{26}$$

Hence, the peak current of the switch is achieved as:

$$i_{SW} = \frac{1+D+N}{(1-D)\, D} I_o. \tag{27}$$

The root mean square (RMS) currents of the elements are calculated for efficiency study, which are presented as follows:

$$I_{n_1}^{RMS} = \sqrt{\frac{D(N+1)^2 + (1-D)}{(1-D)^2}}\, I_o, \tag{28}$$

$$I_{n_2}^{RMS} = \sqrt{\frac{1}{D\,(1-D)}}\, I_o, \tag{29}$$

$$I_{D_1}^{RMS} = \frac{2N+1}{\sqrt{1-D}}\, I_o, \tag{30}$$

$$I_{D_2}^{RMS} = \frac{1}{\sqrt{D}}\, I_o, \tag{31}$$

$$I_{D_o}^{RMS} = \frac{1}{\sqrt{1-D}}\, I_o, \tag{32}$$

$$I_{SW}^{RMS} = \frac{N+D+1}{\sqrt{D}\,(1-D)}\,I_o, \tag{33}$$

$$I_{C_1}^{RMS} = \frac{\sqrt{N^2D+(1+N)^2\,(1-D)}}{(1-D)}\,I_o, \tag{34}$$

$$I_{C_2}^{RMS} = I_{n_2}^{RMS} = \sqrt{\frac{1}{D\,(1-D)}}\,I_o, \tag{35}$$

$$I_{C_3}^{RMS} = \sqrt{\frac{(1-D)+(2N+1)^2D}{D\,(1-D)}}I_o, \tag{36}$$

$$I_{C_o}^{RMS} = \frac{\sqrt{(1-D+N)^2D+(N-1+D)^2\,(1-D)}}{(1-D)}\,I_o. \tag{37}$$

4. Design of the Capacitors and Inductors

Section 4 presents the design procedure of the used capacitors and inductors. For this work, the obtained voltages and currents of C_1, C_2, C_3, C_o, L_{in}, and L_m are used.

4.1. Capacitors

The voltage and current of a capacitor can be expressed versus each other as Eq. (38):

$$i_C = C\frac{dV_C}{dt}. \tag{38}$$

Using Eq. (38) and considering Eq. (39), the minimum value of each capacitor can be determined:

$$\Delta V_C \geq 2\%V_C. \tag{39}$$

According to Eqs. (40)-(43), the minimum value of the capacitors is a function of D, f_s, N, and output load ($R_o = V_o/I_o$). By increasing of f_s and R_o, the values of the capacitors are reduced and as a result, the cost and volume of these elements are decreased.

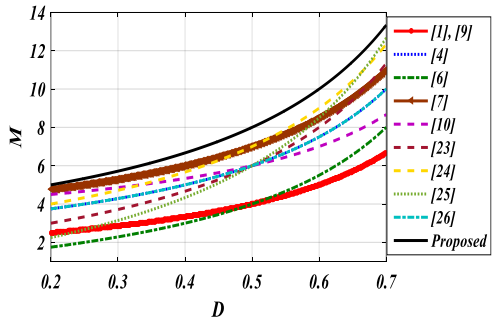


Fig. 5. Voltage gain (M) comparison for N=2.

$$C_1 \geq \frac{D\,(N+2)\,I_o}{2\%f_s\,(D+N+1)\,(1-D)\,V_o}, \tag{40}$$

$$C_2 \geq \frac{(N+2)\,I_o}{2\%f_s\,(1+N\,(1-D))\,V_o}, \tag{41}$$

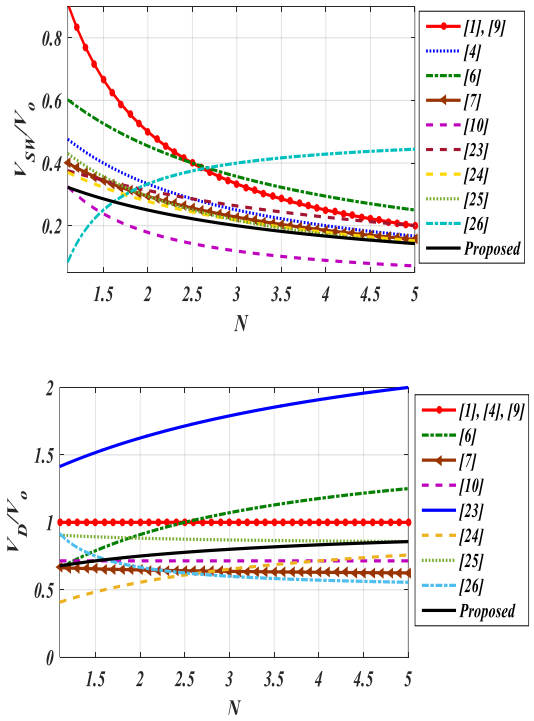


Fig. 6. Peak voltage comparison, (a) Normalized peak voltage stress of switches (V_{SW}/V_o), (b) Normalized peak voltage of diodes (V_D/V_o) for D=0.6.

$$C_3 \geq \frac{D\,(2N+1)\,(N+2)\,I_o}{2\%f_s\,(1-D)\,V_o}, \tag{42}$$

$$C_o \geq \frac{D\,(N+D-1)\,I_o}{2\%f_s\,(1-D)\,V_o}. \tag{43}$$

4.2. Inductors

The relationship between the current and voltage of an inductor can be expressed as Eq. (44):

$$V_L = L\frac{di_L}{dt}. \tag{44}$$

Using Eqs. (44) and (45), the minimum value of L_{in} and L_m can be assumed as:

$$\Delta i_L \geq 20\%I_L. \tag{45}$$

The minimum values of the used inductors are obtained as Eqs. (46) and (47):

$$L_{in} = \frac{V_{in}D}{f_s\Delta i_{L_{in}}}, \tag{46}$$

$$L_m \geq \frac{V_{in}D}{20\%f_sI_{L_m}} = \frac{D(1-D)^2V_o}{20\%f_s(N+2)^2I_o}. \tag{47}$$

Considering equation Eq. (47), it is obvious that the minimum value of L_m is increased by increasing the output load.

5. EFFICIENCY ANALYSIS

Section 5 presents the efficiency analysis of the suggested structure based on the RMS currents. Eq. (48) is the efficiency relation and it is a function of the input power (P_{in}), output power (P_{out}), and total losses (ΔP).

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{in} + \Delta P}. \tag{48}$$

The total loss is presented in Eq. (49). ΔP^{Switch} is the total losses of S, ΔP^{Diodes} is the total losses of the diodes, $\Delta P^{Inductors}$ is the magnetic devices' total losses, and $\Delta P^{Capacitors}$ is the capacitors' total losses.

$$\Delta P = \Delta P^{Switch} + \Delta P^{Diodes} + \Delta P^{Inductors} + \Delta P^{Capacitors}. \tag{49}$$

ΔP^{Switch} includes switching ($\Delta P^{Switching}$) and conduction ($\Delta P^{Conduction}$) losses and obtained as Eq. (50):

$$\Delta P^{Switch} = \Delta P^{Switching} + \Delta P^{Conduction} = \tfrac{1}{2} V_{SW} I_{SW} f_s (t_{rise} + t_{fall}) + r_{DS} \left(I_{SW}^{RMS}\right)^2. \tag{50}$$

Where V_{SW} and I_{SW} are the average voltage and current, I_{SW}^{RMS} is the RMS current, r_{DS} is the On-state resistance, and t_{rise} and t_{fall} are the power switch's rise and fall times. Also, ΔP^{Diodes} includes forward ($\Delta P^{Forward}$) and conduction ($\Delta P^{Conduction}$) losses of all diodes are calculated as Eq. (51):

$$\Delta P^{Diodes} = \Delta P^{Forward} + \Delta P^{Conduction} = V_{Forward} (I_{D_1} + I_{D_2} + I_{D_o}) + r_{D1} (I_{D_1}^{RMS})^2 + r_{D2} (I_{D_2}^{RMS})^2 + r_{Do} (I_{D_3}^{RMS})^2. \tag{51}$$

Where $V_{Forward}$ is the forward voltage and r_{Do} is the diode resistance. Finally, the inductors and capacitors losses are expressed based on their ESR and RMS currents as Eqs. (52) and (53), respectively.

$$\Delta P^{Inductors} = r_{L_{in}} \left(I_{L_{in}}^{RMS}\right)^2 + r_{n_1} \left(I_{n_1}^{RMS}\right)^2 + r_{n_2} \left(I_{n_1}^{RMS}\right)^2, \tag{52}$$

$$\Delta P^{Capacitors} = r_{C_1} \left(I_{C_1}^{RMS}\right)^2 + r_{C_2} \left(I_{C_2}^{RMS}\right)^2 + r_{C_3} \left(I_{C_3}^{RMS}\right)^2 + r_{C_o} \left(I_{C_o}^{RMS}\right)^2. \tag{53}$$

6. COUPLED INDUCTOR DESIGN

The coupled inductor design is fully discussed in this section by considering the critical factor in designing the coupled inductor. The related equations for designing the size of the core, turn ratio, and wire size are completely discussed in [26]. The coupled inductor is designed related to the maximum current of magnetizing inductances. Therefore, the magnetizing inductance should be defined. The maximum current of magnetizing inductance current is equal to:

$$I_{M,\max} = I_M + \Delta i_M. \tag{54}$$

The root mean square (RMS) of the winding current of the coupled inductor can be obtained as follows:

$$I_{tot} = i_{Lk1} + \frac{n_2}{n_1} i_{Lk2}. \tag{55}$$

In order to design the coupled inductor in detail the following steps are utilized [26]:

- Determine core size ($k_g \geq \frac{\rho {L_M}^2 I_{tot} {I_{M,\max}}^2 \times 10^8}{{B_{\max}}^2 P_{cu} k_u}$)
- Determine the air gaps are neglected
- Determine the winding number of the first side of the coupled inductor ($n_1 = \frac{L_M I_{M,\max} \times 10^4}{B_{\max} A_c}$)
- Determine the winding number of the second side of the coupled inductor ($n_2 = \frac{n_1}{2}$)
- Evaluate fraction of window area allocated each winding ($a_1 = \frac{n_1 I_1}{I_{tot}}$, $a_2 = \frac{n_2 I_2}{n_1 I_{tot}}$)
- Evaluate the wire size ($A_{w1} \leq \frac{a_1 k_g W_A}{n_1}$, $A_{w2} \leq \frac{a_2 k_g W_A}{n_2}$)

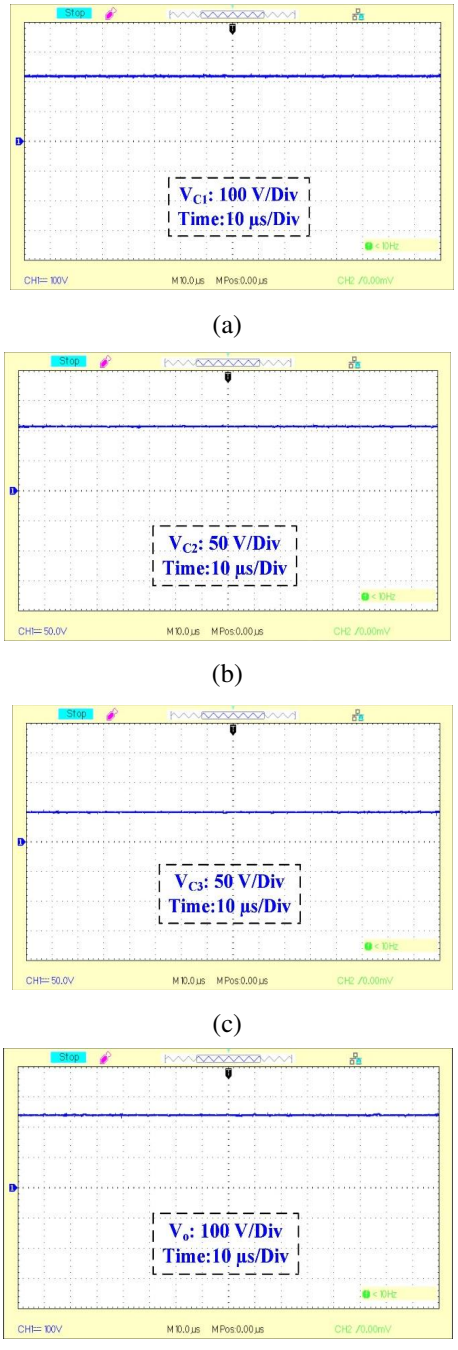
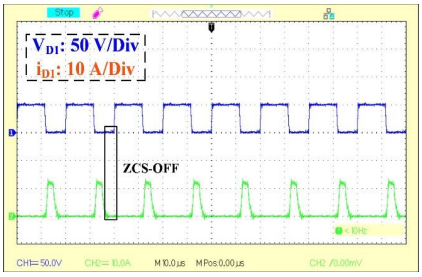
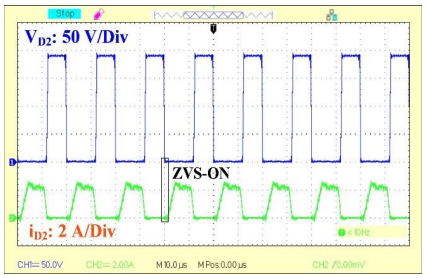


Fig. 7. The measurement voltage of (a) V_{c1}, (b) V_{c2}, (c) V_{c3}, and (d) V_o.

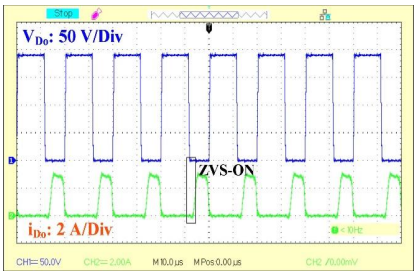
It has to be mentioned that in order to design the coupled inductor, the EPCOS B66344 (Ferrite core EE60) model is utilized. The magnetizing inductance (L_m) is chosen at 200 μH. For the coupled inductor with $L_m = 200$ μH, the number of the first side of the coupled inductor winding is 25 turns, and the number of the



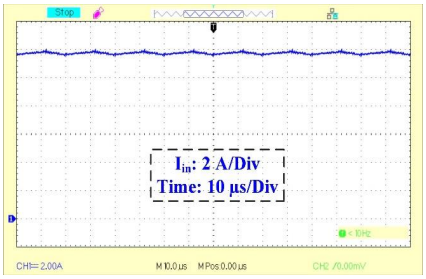
(a)



(b)



(c)



(d)

Fig. 8. The measurement voltages (a) V_{D1} & i_{D1} (b) V_{D2} & i_{D2} (c) V_{Do} & i_{Do} and (d) input current.

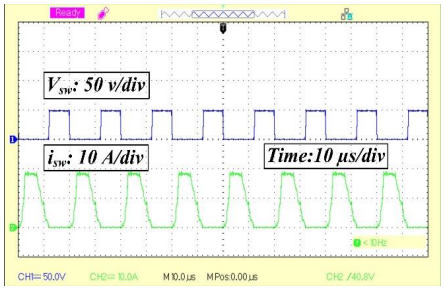
second side of the coupled inductor winding is 75 turns. Regarding Eq. (22), if we consider the coupling coefficient about 0.98 and $L_m = 100$ μH in the experimental result, the leakage inductance (L_k) can be calculated as follows:

$$K = \frac{L_m}{L_m + L_k}. \tag{56}$$

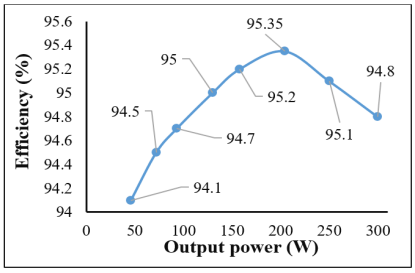
By solving Eq. (56), the leakage inductance (L_k) is obtained about 2 μH Extreme care has been taken in the design of the coupled inductor to have a low leakage inductance.

7. Comparison Survey

The comparison between the presented converter and other similar works are presented in terms of soft switching, input current ripple, efficiency at $P_o = 200$ W, voltage gain, normalized



(a)



(b)

Fig. 9. (a) The measurement voltage and current of S, and (b) the efficiency waveform for different load values.

peak voltage stress across semiconductors (V_{SW}/V_o and V_D/V_o), count of used elements like switches, diodes, capacitors, inductors, and coupled inductors are considered. Table 1 gives the summary of this comparison. The converters in [9], [10], [27], and [28] have more switches than the other converters. The structures in [4], [10], and [29] have a lower number of magnetic cores. The number of diodes in [6], [10], and [27–30] are higher than the other converters, and the structures in [1] and [7] used a low number of capacitors. Furthermore, the elements count in [27] is seventeen and it is more than the other introduced topologies in Table 1. The voltage gain of the converters is shown in Fig. 5 versus different D and N equal to 2. The recommended converter's voltage conversion ratio is higher for the same value of N and $0.2 < D < 0.7$. The normalized peak voltage stress across semiconductors is shown in Figs. 6 (a) and (b). According to this figure, the converter in [10] has lower V_{SW}/V_o than the recommended topology. However, this converter does not soft switching feature and it suffers from the input current with high ripple. For $N < 2$, the proposed converter and [10] have an almost equal V_{SW}/V_o. For $N > 1$, The normalized maximum peak voltage of diodes (V_D/V_o) of the converter in [7], [10], and [28] is lower than the presented topology. However, these topologies have higher input current ripple and lower voltage gain than the proposed converter. Based on this section, the suggested topology has a soft switching feature, low input current ripple, high voltage gain, and higher efficiency, which these benefits make it a proper option for RE applications like PV systems.

8. Experimental Results

To confirm the mathematical investigations, the suggested structure has been implemented. The basic specifications of the devices and the main parameter values are exhibited in Table 2. The laboratory waveforms of the suggested topology are depicted in Fig. 7-9. The voltage across C_1, C_2, and C_3 and also $V - o$ are shown in Figs. 7 (a)–7 (d). The voltage of C_1 is 220 V, which verifies Eq. (15). Figs. 7-(b) and 7-(c) shows V_{C2} and V_{C3}, respectively which are about 107 V and 50 V, respectively. These obtained values for capacitors C_2 and C_3 confirm the relationships (14) and (13). The input voltage (V_{in}) is equal to 20 V and enhanced to almost 240 V with low ripple.

Table 1. Summary of the Comparison.

Structures	Num. components					Num. of components	Gain (M)	Max volt. on switches	Max volt. on diodes	Soft Switching	Ripple of I_{in}	Eff [%] at 200 W
	C	CI	L	D	SW							
[1]	two	one	one	two	one	seven	N/(1-D)	1/N	1	Yes	small	95.9
[4]	three	one	-	three	one	eight	(1+N)/(1-D)	1/(1+N)	1	×	large	95.5
[6]	three	one	one	four	one	ten	(1+ND)/(1-D)	1/(1+ND)	N/(1+ND)	×	large	92.7
[7]	two	one	one	two	one	seven	(N+2-D)/(1-D)	1/(N+2-D)	(ND+1)/(N+2-D)	×	large	93.6
[9]	three	one	one	two	two	nine	N/(1-D)	1/N	1	Yes	small	95.5
[10]	three	one	-	five	two	eleven	N(2-D)/(1-D)	1/((2-D)2N)	1/(2-D)	×	large	92.9
[27]	five	one	one	eight	two	seventeen	(2+ND)/(1-D)	1/(2+ND)	(2+n(1+D))/(2+ND)	Yes	large	94.55
[28]	four	two	-	four	two	twelve	(1+N+D)/(1-D)	1/(1+N+D)	N/(1+N+D)	Yes	large	94.7
[29]	four	one	-	four	one	ten	(1+2ND)/(1-D)	1/(1+2ND)	(1+N)/(1+2ND)	Yes	large	-
[30]	four	one	one	three	one	ten	(2N-1)/((N-1)(1-D))	(N-1)/(2N-1)	N/(2N-1)	Yes	small	95.2
Suggested	four	one	one	three	one	ten	(2+N)/(1-D)	1/(2+N)	(1+N)/(2+N)	Yes	small	95.45

Table 2. The specification of the used elements.

Element	Specification
Switch	S: IRFP260N, $R_{DS(ON)}$= 0.04 Ω
Diodes	D1: MUR2060 D_2 and D_o: MUR1560
Capacitors	C_1: 200 V/ 220 μF C_2: 200 V/ 220 μF C_3: 200 V/ 220 μF C_o: 400V/ 470 μF
Input inductor	100 μH, r_L=10 $m\Omega$ Ferrite core EE60
Coupled inductor	L_m=200 μH Ferrite core EE60 Primary resistance = 70 $m\Omega$ Secondary resistance= 100 $m\Omega$
Parameters	Value
P_o	230 W
V_{in}	20 V
V_o	240 V
N	3
f_s	50 kHz
D	0.6

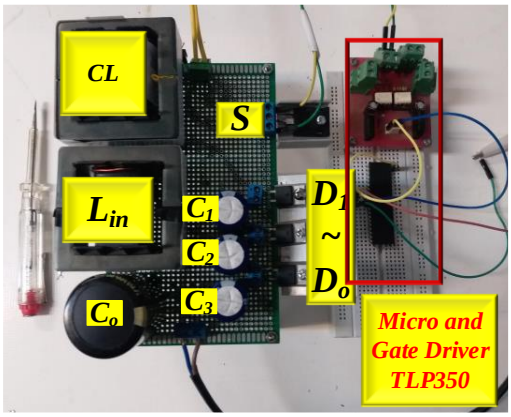


Fig. 10. The experimental prototype.

The laboratory result of the voltage and current of D_1, D_2, and D_o and also the drain–source voltage of the switch (VDS) is depicted in Figs. 8 (a) – 8 (d). The voltage of diode D_1 is 50 V and the current is 12 A. In this figure, it is clear that diode D_1 is softly switched off and the loss related to the reverse recovery of D_1 is decreased. Other soft-switching conditions occur when the diode D_2 is turned on. From Fig. 8-(b), D_2 is directly biased in the ZVS situation which improves the converter efficiency. The voltage of D_2 is 190 V and its current is 2.5 A. The voltage and current of D_o are depicted in Fig. 8-(c), which are almost 190 V and 4 A. From this figure, it can be seen that D_o is directly biased ZVS as D_2. The input current waveform is demonstrated in Fig. 8-(d). It is clear that the input current ripple is low. V_{DS} of the switch is shown in Fig. 9-(a), which is approximately 50 V. From Fig. 9-(a), the voltage stress of the switch is approximately a quarter of V_o. considering the experimental results, it can be achieved that the waveforms obtained from the laboratory test confirm the theoretical survey and mathematical calculations.Fig. 9-(b) depicts the experimental power efficiency. This figure is obtained by the parameters $f_s = 50$ kHz, N=3, and D=0.6. At $P_o = 200$ W, the highest efficiency is around 95.45%. Furthermore, the efficiency at output power =300 W is around 94.8%.

As a consequence of the technical assessment, steady-state computation, and prototype testing results, the proposed topology can be suitable for RE generation. The experimental prototype of the suggested converter is shown in Fig. 10.

9. Conclusion

This article offered a novel high-voltage gain topology using a coupled inductor and VMC for RE systems like PV and FC. This structure has a flexible voltage gain and it can be enhanced by adjusting the N and D of the switch. Also, the voltage stress of the power switch is decreased by increasing N. Totally, the benefits of the suggested converter are: 1) High voltage gain, 2) Reduced peak voltage of semiconductors, 3) input current with low ripple, 4) Soft switching: ZVS and ZCS, 5) high efficiency, 6) low components count, and 7) common grounding of the input and output. To demonstrate the usefulness of the recommended converter, the operational modes, steady-state, and efficiency study, along with a comparison study are presented. Finally, an experimental prototype with 95.2 % efficiency in $P_o = 230$ W, $V_{in} = 20$ V, and $V_o = 240$ V is built.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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