Journal of Operation and Automation in Power Engineering

vol. XX, no. XX, Dec. 2022, Pages: XXXX (Proofed)

http://joape.uma.ac.ir

Analysis and Implementation of a High Step-Up DC-DC Converter Integrating a Hybrid Voltage Multiplier Cell and a Coupled Inductor

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Abstract— *This research introduces a modified design for non-isolated DC-DC converters with a high voltage gain using the design concepts of a coupled inductor (CI) and a hybrid voltage multiplier cell. It is attainable to further increase the output gain without requiring a higher duty cycle or a large turn ratio of CI. This means that the power switch won't be under too much voltage stress. The suggested converter's important features are low maximum voltage across all semiconductor components, considerable efficiency, and a substantial voltage conversion ratio. In addition, the suggested topology includes diodes with soft switching conditions, which allows for a reduction in reverse recovery losses and an improvement in system efficiency. The proposed topology includes input current continuity, a single power switch, and a common ground between the source and the load. Operating analysis, theoretical definitions, efficiency investigation, and a literature review of comparable structures have been considered to demonstrate the proposed structure's functionality. An experimental prototype has also been established, featuring 115V output voltage, 20V input voltage, and 40kHz switching frequency, to facilitate the assessment of the proposed converter's efficacy.*

Keywords—Non-isolated DC-DC converter, high voltage gain, hybrid voltage multiplier cell, coupled inductor.

1. INTRODUCTION

1.1. Research background

In reply to the pressing issues of energy shortage and pollution, renewable energy sources (RESs), such as electric vehicles (EVs), wind turbines, photovoltaics, and supercapacitor power conversions, have grown increasingly in recent times [1, 2]. Typically, the low voltages produced by these energy systems cannot be directly linked to the high-voltage DC bus. Therefore, to increase the voltage supplied to the post-stage DC bus, a high voltage gain DC-DC converter must be used to enhance the lower output voltage. Important considerations for designing such converters include converter volume, input current ripple, efficiency, and voltage gain [3].

Generally, improving the duty cycle of traditional boost converters should theoretically allow them to generate a limitless output voltage. Nevertheless, these converters are impacted by component parasitic characteristics and cannot meet their theoretical voltage conversion capacity at the maximum duty cycle; hence, the duty cycle can't be exceedingly high [4]. Moreover, problems with the output diode might arise when the duty ratio is increased, diminishing efficiency, limiting the switching frequency, and even resulting in electromagnetic interference (EMI). This situation highlights the critical need to develop modified high voltage gain DC-DC converters with dependable efficiency [5].

Since they can adjust any required transformer turns ratio, employing high-frequency transformers in coupled inductors (CIs) and isolated DC-DC converters is a method to supply high voltage gain. Nevertheless, there is a downside to incorporating magnetic components, which is the increased bulk and expense. Another issue is that the leakage inductance causes voltage spikes on semiconductors [6]. To solve this problem, snubber circuits are usually needed, which makes the system more complicated and expensive and increases the total power loss [7].

Typically, to provide a greater voltage gain, the integration of magnetic coupling and voltage multiplier cells (VMCs) is utilized in the topologies design. Diodes and capacitors are common components in these converters, which allow them to have a high-performance circuit with a straightforward and inexpensive topology. However, utilizing numerous active and passive elements can complicate the power and control aspects [8]. Cascading [9] and interleaving [10] are two other typical boosting methods that make use of switched capacitors. Cascading is a solution that doesn't need a novel circuit design. However, this technique increases semiconductor use, reducing efficiency and power density. In spite of its many advantages, interleaving also has challenges related to control and the complexities of the converter [3].

1.2. Literature review

The wide range of uses for DC-DC converters has led to the introduction of several topologies, each with its own set of characteristics, in recent years. While most review papers have concentrated on categorizing and deriving voltage-increasing approaches, the paper in [11] intends to assess the converters from different topological and operational perspectives and then rank them according to their usefulness in specific applications. In addition, this article suggests several new merit converters to serve as a useful benchmark for research comparing power electronic converters. Another review article is dedicated to documenting the latest advancements in EV charging systems, focusing on the topologies of DC-DC converters employed by on-board and off-board systems [12]. This research study categorizes DC-DC converters into two types and delves into the difficulties and new directions in EV charging that researchers may want to

Received: 12 May 2024
Revised: 10 Jun. 2024
Accepted: 14 Jun. 2024
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DOI: 10.22098/joape.2024.15060.2149
Research Paper

investigate further. In [13], the authors explain an interleaved boost converter incorporating a bifold Dickson voltage multiplier. This topology is ideal for connecting low-voltage devices to high-voltage distribution buses and other purposes requiring a high voltage gain conversion ratio. The suggested converter's first stage consists of an interleaved boost stage with two inductors controlled by two low-side active switches. The second stage, the VMC stage, consists mostly of diodes and capacitors that enhance the total voltage gain. Despite this, the price and power loss are inflated due to the excessive number of components utilized. The converters described in [14, 15] include a VMC and CI in their circuit. Both the high number of components and the ripple in the input current are issues with these topologies. To reduce input current ripple, a bidirectional converter with soft-switching capability is introduced in [16]. However, this design suffers from a low voltage conversion ratio and decreased efficiency at high power rates. A two-winding CI is used to increase the voltage gain in a paper. The suggested design minimizes conduction power losses with a single power switch [17]. The soft-switching capability of diodes, which may enhance efficiency, is another notable advantage of this topology. A novel DC-DC converter that exhibits impressive step-up capability is examined and described in [18]. The suggested converter ideally combines the CIs, VMCs, and series capacitor approaches to achieve high voltage gain with minimal voltage stress. In this topology, the VMC does double duty as an energy absorber and contributor to voltage gain. Moreover, the nonlinear characteristics of DC-DC converters cause the output voltage to fluctuate continuously, making the device very sensitive to changes in the circuit. In contrast, a closed-loop control system using a robust controller is the best approach when utilizing such converters since, in many cases, the output voltage stability is crucial. Two unique methods were presented in [19, 20] to enhance the DC-DC converters' dynamic responsiveness by using innovative and hybrid controllers instead of the traditional PID controller.

1.3. Present research aims

To achieve a high voltage conversion ratio topology, this article suggests a modified DC-DC converter that combines two boosting stages, a hybrid voltage multiplier cell (HVMC) and a CI, with soft-switching capabilities. The merits of this converter include low maximum voltage across all semiconductor components, impressive voltage gain, continuous input current, and minimal power loss. Some benefits of the proposed topology are as follows:

- Using a CI in conjunction with an HVMC produces a significant voltage gain.
- The suggested converter has the advantages of the quadratic boost converter, including its common ground feature and non-pulsating input current, which makes it a desirable choice for connecting with RESs by simplifying the grounding scheme, increasing total efficiency, and minimizing the EMI and leakage current.
- Due to the lower voltage stress compared to the output voltage, semiconductors with lower parasitic characteristics can be used.
- The diodes' soft-switching features and the presence of a single power switch in the proposed design increase overall efficiency.

The suggested converter's features have been assessed by comparing it with similar converters. Outcomes show that the proposed design performs better than similar references, especially when comparing voltage gain, where the converter offers the best stepping-up capability.

The rest of this study is summarized as follows: Section 2 details the suggested converter's functional concept, switching states, and topology. Section 3 of the paper presents the steady-state investigation of the converter. The methodology used in the design process and the efficiency, loss analysis by considering parasitic elements are explained in Sections 4 and 5, respectively. Section 6 provides specifics on the experimental results and comparative study findings. The concluding statements are then presented in Section 7.

2. Theoretical Analysis

2.1. Suggested topology

Based on what is shown in Fig. 1, the presented converter comprises boosting stages, an HVMC, and a CI. The PWM signal also allows for more convenient operation in the suggested converter due to having a single power switch. Moreover, the switch is centrally located near the input source, so it undergoes low-voltage stress. In addition to the CI and the switch, the proposed circuit includes two inductors, four capacitors, and four power diodes. The two CI windings with a turn ratio of $n = N_2/N_1$ are charged concurrently while the switch is biased forward and discharged in succession when the power switch is reverse-biased. Also, the inductor L_1 maintains the input current constant and ripple to a minimum in this topology.

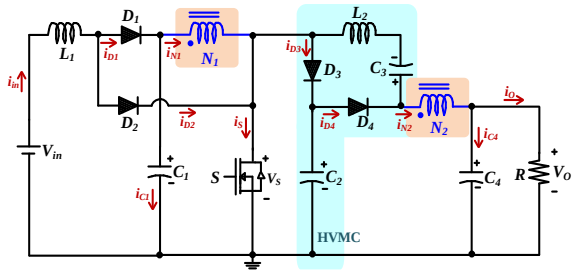

Fig. 1. Suggested converter's equivalent circuit.

2.2. CCM operating concept

Fig. 2 shows the main waveforms that resemble the two modes of the converter's functioning in CCM. In addition, Fig. 3 shows the suggested topology's equivalent circuits based on the operating states. A simple analysis of the topology can be accomplished by using the following assumptions:

- There is no ripple in the current passing through the magnetizing inductor (L_m).
- The parasitic characteristics among the inductive and capacitive components are ignored.
- Every component used in the switching process is ideal.
- Large enough capacitors allow us to ignore voltage ripple.

This section will therefore concentrate on the two switching modes, supported by Figs. 2 and 3.

A) First mode ($t_0 \leq t \leq t_1$):

The signal from the gating pulse causes switch S to start turning on at time $t = t_0$. Unlike the forward-biased diode D_2, the others diodes are biased in the opposite direction. At this moment, energy is kept in the primary N_1 and secondary N_2 sides of the CI, as well as in the inductor L_1, simply because both are charged. Meanwhile, the inductor L_2 is discharging. Additionally, capacitors C_1 and C_4 have been discharged, and capacitor C_3 has been charged. The voltage of capacitor C_2 is equally unaffected. The mode finishes after the current i_S simply drops to zero. In accordance with the circuit shown in Fig. 3-(a), the subsequent formulas are provided:

$$\begin{cases} V_{L1} = V_{in} \\ V_{N1} = V_{C1} \\ V_{L2} = V_{C3} - V_{C4} - V_{N2} \\ V_O = V_{C4} \end{cases} \quad (1)$$

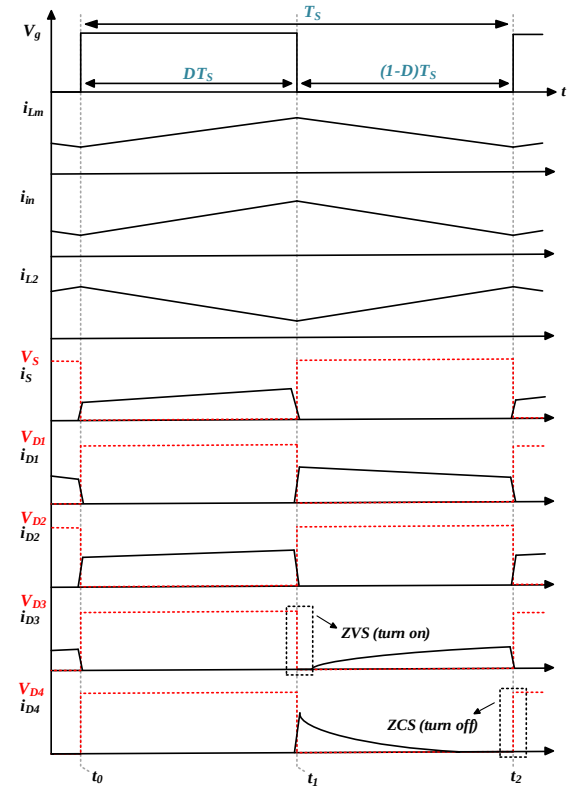

Fig. 2. Crucial CCM waveforms of the proposed converter.

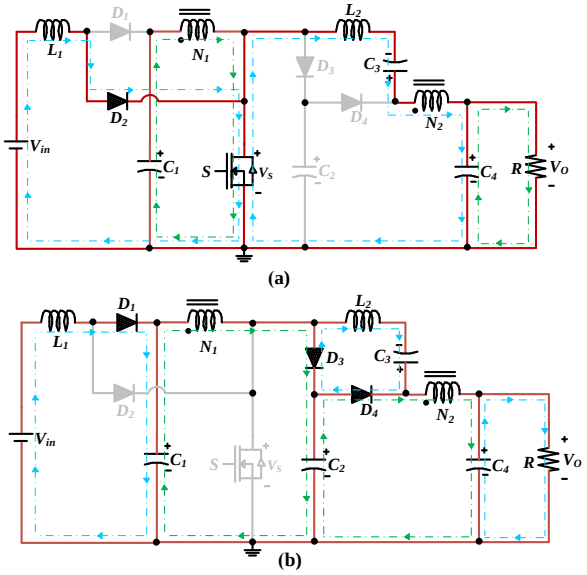

Fig. 3. Operation modes of the recommended converter during CCM: (a) First mode $[t_0 - t_1]$ (b) Second mode $[t_1 - t_2]$.

B) Second mode ($t_1 \leq t \leq t_2$):

power switch is switched off, the second period begins at $t = t_1$. In this operational mode, diodes D_1, D_3, and D_4 are turned on while diode D_2 is turned off. Magnetizing inductor L_m and inductor L_1 are simultaneously discharged. However, the L_2 inductor is also charging at the moment. Capacitor C_3 is draining while C_1 and C_4 are charging, in contrast to the first operating mode. This switching condition stops once the power switch is turned on. Fig. 3-(b) and the accompanying equations depict this mode for the suggested circuit:

$$\begin{cases} V_{L1} = V_{in} - V_{C1} \\ V_{N1} = V_{C1} - V_{C2} \\ V_{L2} = V_{C3} \\ V_{N2} = V_{C4} - V_{C2} \\ V_O = V_{C4} \end{cases} \tag{2}$$

2.3. DCM operating concept

Three different operating intervals are available to the converter in this mode; the first two are identical to those in the CCM. The third mode involves turning off all semiconductor components and bringing the input current to zero. A visual representation of the relevant circuit during this time frame is shown in Fig. 4. Based on investigations, it can be inferred that only capacitor C_4 is responsible for providing power to the load. Changes in the system's input current behavior will inevitably impact the equations about the proposed converter compared to the CCM mode. We will address these equations in the following section.

3. Analysis of Steady-State Conditions

3.1. Voltage gain of the CCM

By solving Eqs. (1) and (2) using the KVL and voltage-second balance methods, the capacitors' voltage and facilitate the steady-state analysis in this operating mode can be found. This leads us to the following conclusions about inductor L_1:

$$\begin{cases} \int_0^{DT_S} V_{L1} dt + \int_{DT_S}^{T_S} V_{L1} dt = 0 \\ V_{C1} = \frac{V_{in}}{1-D} \end{cases} \tag{3}$$

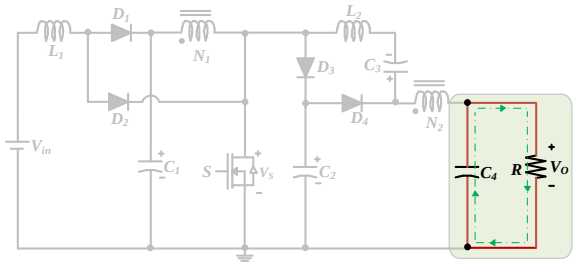

Fig. 4. Equivalent circuit of the converter in DCM's third mode.

Additionally, the following are relevant for determining the voltages of capacitors C_2 and C_3:

$$\begin{cases} \int_0^{DT_S} V_{N1} dt + \int_{DT_S}^{T_S} V_{N1} dt = 0 \\ V_{C2} = \frac{V_{in}}{(1-D)^2} \end{cases} \tag{4}$$

$$\begin{cases} \int_0^{DT_S} V_{L2} dt + \int_{DT_S}^{T_S} V_{L2} dt = 0 \\ V_{C3} = V_O D + \frac{nDV_{in}}{1-D} \end{cases} \tag{5}$$

As a result, using the equations obtained from the studied time intervals, the proposed topology's voltage gain is as follows:

$$M_{CCM} = \frac{V_O}{V_{in}} = \frac{nD+1}{(1-D)^2} \tag{6}$$

Fig. 5 shows the ideal output voltage gain for different duty cycles and CI turn ratios (n). This allows for measuring the converter voltage gain over various changes. It is clear that the

converter can produce an extraordinarily high output voltage gain even when the duty cycles are lowered, which transforms the device into a high step-up converter. When the value of n is more than two, and the value of D is within the range of 0.6 to 0.8, the output voltage gain rises substantially. On the other hand, the converter's inefficiency will be revealed when it is used at greater duty cycles.

3.2. Voltage stresses in CCM

To represent the voltage stress over the capacitors as a function of the output voltage, the following equations can be used:

$$\begin{cases} V_{C1} = \frac{1-D}{nD+1} V_O \\ V_{C2} = \frac{1}{nD+1} V_O \\ V_{C3} = \frac{(n+1)D}{nD+1} V_O \end{cases} \tag{7}$$

According to these equations, the significant variables influencing the voltage stress on the capacitors are the duty cycle and n. Also, the voltage stresses discussed are significantly less than the output voltage. In addition, the following formula may be used to calculate the voltage stress over semiconductors:

$$\begin{cases} V_S = \frac{V_O}{nD+1} \\ V_{D1} = \frac{1-D}{nD+1} V_O \\ V_{D2} = \frac{D}{nD+1} V_O \\ V_{D3} = \frac{V_O}{nD+1} \\ V_{D4} = \frac{(n-1)D+1}{nD+1} V_O \end{cases} \tag{8}$$

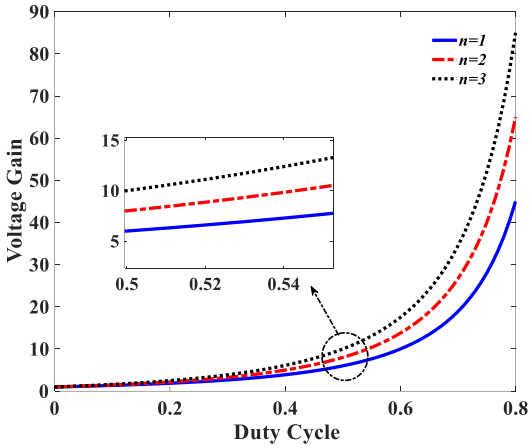

Fig. 5. Voltage gain waveform in various configurations (depending on changes in D and n).

It is evident that a significant disparity exists in the voltage stress and the output voltage throughout the power switch and diodes. For this reason, a power switch and diodes with reduced voltage ranges and internal resistances can be used, significantly improving the system's efficiency.

3.3. BCM assessment

During the BCM analysis, it is crucial to establish if the currents through the proposed converter's inductors L_1, and the magnetizing inductor (L_m) are continuous. Furthermore, the mathematical equation for the inductance associated with these inductors can be obtained by studying their current connections in this operation state. Hence, selecting the inductor with the correct value allows one to determine the circuit's conduction mode. If we assume that Δi_{L1} is the inductor L_1's current ripple, we can define it as follows:

$$\begin{cases} \int_0^{I_{L1MAX}} di_{L1} = \int_0^{DT_S} \frac{1}{L_1} V_{L1} dt \\ \Delta i_{L1} = \frac{V_{in} DT_S}{L_1} \end{cases} \tag{9}$$

Accordingly, the formula for the average current via the inductor L_1 is:

$$I_{L1} = \frac{\Delta i_{L1}}{2} \tag{10}$$

The following inference can be drawn from this:

$$I_{L1} = \frac{V_{in} DT_S}{2L_1} \tag{11}$$

$$L_1^{BCM} = \frac{V_{in} DT_S}{2I_{L1}} \tag{12}$$

Eq. (12) may be rewritten as follows as the input current is equivalent to the inductor L_1 current:

$$L_1^{BCM} = \frac{RD}{2f_s M_{CCM}^2} \tag{13}$$

Moreover, the L_m of the CI follows similar relations:

$$\begin{cases} \Delta i_{Lm} = \frac{V_{Lm} DT_S}{L_m} = \frac{V_{in} DT_S}{L_m(1-D)} \\ I_{Lm} = \frac{\Delta i_{Lm}}{2} \\ I_{Lm} = I_{N1} - nI_{N2} = \frac{((2D+1)n+1)V_O}{(1-D)R} \\ L_m^{BCM} = \frac{V_{in} D}{2I_{Lm} f_s (1-D)} = \frac{RD}{2((2D+1)n+1)M_{CCM} f_s} \end{cases} \tag{14}$$

Consequently, utilizing Eqs. (13) and (14), the intended conduction mode can be described with the L_1 and L_m inductance. Regarding the inductor L_2, its current is identical to that of the capacitor C_3 in all modes. Additionally, because the average current of the capacitors is zero, the average current of this inductor is likewise almost zero. This inductor is placed in HVMC to dampen spikes in the circuit. Furthermore, the normalizing inductor value can be obtained by calculating the time constant τ_L as $\tau_L = Lf_s/R$ [2]. This leads us to the following boundary states for L_1 and L_m:

$$\begin{cases} \tau_{L1B} = \frac{D(1-D)^4}{2(nD+1)^2} \\ \tau_{LmB} = \frac{D(1-D)^2}{(nD+1)((4D+2)n+2)} \end{cases} \tag{15}$$

The relationship between τ_L and D is seen in Fig. 6, following Eq. (15). As a result, the CCM operation occurs when the value of τ_L is greater than the τ_{LB}, but the DCM operation occurs when the value of τ_L is lower than the value of τ_{LB}.

3.4. DCM assessment

In this state, as mentioned earlier and considering Fig. 4, the input current is zero in the third mode. Similar to the CCM mode, the following outcomes are formed by applying the volt-second law to the inductors in the circuit:

$$\begin{cases} \int_0^{DT_S} V_{L1} dt + \int_{DT_S}^{D'T_S} V_{L1} dt = 0 \\ V_{C1} = \frac{V_{in} D'}{D'-D} \end{cases} \tag{16}$$

$$\begin{cases} \int_0^{DT_S} V_{N1} dt + \int_{DT_S}^{D'T_S} V_{N1} dt = 0 \\ V_{C2} = V_{in}(\frac{D'^2+nDD'}{(D'-D)^2}) \end{cases} \tag{17}$$

$$\begin{cases} -V_{C1}+(n+1)(V_{C1}-V_{C2})+V_O=0 \\ V_O=V_{in}(\frac{D'^2+nDD'}{(D'-D)^2}) \end{cases} \quad (18)$$

Using the relationships discussed, the following formula can be used to get the voltage gain in the DCM of the converter:

$$M_{DCM}=\frac{D'^2+nDD'}{(D'-D)^2} \quad (19)$$

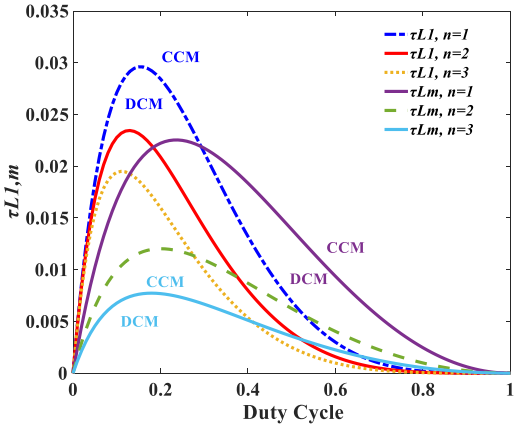

Fig. 6. Suggested converter's boundary conditions.

By comparing the voltage gains in DCM and CCM (Eqs. (6) and (19)), it can be inferred that they are precisely proportional to each other when $D'=1$. The findings validate the correctness of the calculations and allow us to infer that D' ought to perpetually remain less than one.

4. Procedure of Designing Elements

Determining the appropriate values of the capacitor and inductance, the highest possible current and voltage stress of the semiconductors, and selecting the correct model of these components are crucial to designing and deploying a converter's topology. Section 3.2 has addressed the voltage stresses imposed on the switch and diodes. In addition, the average currents of semiconductors can be calculated using the following formulas:

$$\begin{cases} I_S^{avg}=(\frac{D(nD+1)(2-D)}{(1-D)^2}-D)I_O \\ I_{D1}^{avg}=\frac{nD+1}{1-D}I_O \\ I_{D2}^{avg}=\frac{nD^2+D}{(1-D)^2}I_O \\ I_{D3}^{avg}=\frac{nD+1}{1-D}I_O \\ I_{D4}^{avg}=I_O \end{cases} \quad (20)$$

The following subsections discuss the design approaches for the inductors and capacitors, which are crucial components of the converter.

4.1. Design of the inductors

Notable considerations in CI design involve magnetizing current, turns ratio, and inductance value. According to Eq. (6), the turn ratio of CI is directly related to the voltage gain and duty cycle. As a result, this is how to determine n:

$$n=\frac{V_O(1-D)^2-V_{in}}{V_{in}D} \quad (21)$$

It is also possible to establish the magnetizing inductance by considering the circuit's operating conditions and the appropriate current ripple. Therefore, finding the value of L_m is possible using Eq. (14). During the design process, the recommended converter's inductors had their minimum values of $\Delta i_L=0.3I_L$ selected to ensure optimum performance and efficiency. Due to the fact that the design of the CI is dependent on these values, the following are the average and maximum magnetizing currents found:

$$\begin{cases} I_{Lm}=I_{N1}-nI_{N2}=\frac{((2D+1)n+1)V_O}{(1-D)R} \\ i_{Lm}^{\max}=I_{Lm}+\Delta i_{Lm}/2=\frac{((2D+1)n+1)V_O}{(1-D)R}+\frac{V_{in}DT_S}{2L_m(1-D)} \end{cases} \quad (22)$$

The value of the L_1 inductor's inductance can be found using Eq. (12). More details on the L_1 current's average and maximum values can be obtained from the following formula:

$$\begin{cases} I_{L1}=I_{in} \\ i_{L1}^{\max}=\frac{(nD+1)V_O}{R(1-D)^2}+\frac{V_{in}DT_S}{2L_1} \end{cases} \quad (23)$$

4.2. Design of the capacitors

Capacitors are regarded as elements that keep a constant voltage as there seems to be a possibility that a change in the capacitor voltage might affect the system's operation. Section 3.2 (Eq. (7)) contains the formula for determining the voltage value of capacitors. Moreover, to determine the capacitors' voltage ripple, $\Delta V_C<0.01V_C$ is also taken into account. Consequently, the values of the capacitors are determined by evaluating the current flowing across them and the permissible voltage ripple as follows:

$$\begin{cases} I_{C1}^{I}=I_{in}(1-D) \\ C_1=\frac{I_{C1}DT}{\Delta V_{C1}} \end{cases} \quad (24)$$

$$\begin{cases} I_{C2}^{II}=I_{in}(1-D)-I_O \\ C_2=\frac{I_{C2}(1-D)T}{\Delta V_{C2}} \end{cases} \quad (25)$$

$$\begin{cases} I_{C3}^{II}=\frac{I_OD}{1-D} \\ C_3=\frac{I_{C3}(1-D)T}{\Delta V_{C3}} \end{cases} \quad (26)$$

$$\begin{cases} I_{C4}^{II}=\frac{I_O}{1-D} \\ C_4=\frac{I_{C4}(1-D)T}{\Delta V_{C4}} \end{cases} \quad (27)$$

The superscripts I and II denote the initial and second operating modes in CCM computations, respectively. Based on the calculations above and applied to a 205W version of the suggested converter working in CCM, the experimental prototype's element specifications are shown in Table 1.

5. Evaluation of Power Loss and Efficiency

Earlier sections conducted the general design formulae and steady-state evaluation of the converter, presuming the provided circuit is ideal. Here, we add parasitic components and resistance into the circuit to simulate real-world operating conditions and calculate the system's efficiency and total losses.

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As a result, these resistances are often described using the following explanations:

- In CI ESRs, R_{N1} and R_{N2} correspondingly represent the primary and secondary sides.
- R_{L1} and R_{L2} denote the ESRs of the L_1 and L_2 inductors.
- As power switch S is activated, the abbreviation R_{DS} indicates the switch's resistance.
- The capacitors' ESR values are denoted by R_1-R_4.

Table 1. Suggested converter configurations and parameter specifications.

Element/Parameter	Features
S	IRFP260N
$D_1 - D_6$	MUR1560
L_1	$700\mu H, 15A$
L_2	$150\mu H, 10A$
L_m	$600\mu H, 10A$
C_{1-3}	$470\mu F/100V$
C_4	$470\mu F/400V$
n/R	1:1/65Ω
V_{in}/V_{out}	20V/115V
Frequency/Output power	40kHz/205W

- $R_{F1} - R_{F4}$ represents the forward resistances of the diodes, whereas $V_{F1} - V_{F4}$ reveals the threshold voltages.

Here are the parasitic components' values: $R_{F1} - R_{F4} = 0.05\Omega$, $V_{F1} - V_{F4} = 1V$, $R_1 - R_3 = 0.047\Omega$, $R_4 = 0.03\Omega$, $R_{DS} = 0.05\Omega$, $R_{L1} = 0.2\Omega$, $R_{L2} = 0.05\Omega$, $R_{N1} = 0.13\Omega$, $R_{N2} = 0.14\Omega$

To determine the total losses of the converter, one may use the following formula:

$$P_{loss} = P_{SW} + P_{RF} + P_{VF} + P_L + P_C \tag{28}$$

where diode losses (P_{RF} and P_{VF}), power switch loss (P_{SW}), inductor losses (P_L), and capacitor losses (P_C) all contribute to the overall system losses in the proposed topology. Moreover, it is possible to ascertain the circuit's efficiency by using the following:

$$\eta_{conv} = (\frac{P_O}{P_O + P_{loss}}) \tag{29}$$

The losses related to power switches usually consist of two types: conduction and switching losses. Due to their fast switching time, MOSFETs have switching losses during on and off operations as they adapt to changes in voltage and current. In fact, turning the power switch from off to on or back again causes switching losses. This leads us to the following formula for the circuit's loss of a single power switch [1]:

$$P_{SW} = R_{DS}(I_{\mathrm{S}}^{\mathrm{rms}})^2 + \frac{1}{2} f_s (t_{\mathrm{on}} + t_{\mathrm{off}}) I_S^{\mathrm{avg}} V_S \tag{30}$$

where t_{on} represents the rising time of the MOSFET and t_{off} represents the falling time. Eq. (20) obtains the average current value of the power switch, and the RMS value is computed as shown in the following:

$$I_S^{rms} = (\frac{\sqrt{D}(nD+1)(2-D)}{(1-D)^2} - \sqrt{D}) I_O \tag{31}$$

Furthermore, the diodes' P_{RF} and P_{VF} are defined in the following:

$$\begin{cases} P_{RF} = \sum_{i=1}^{4} R_{Fi} (I_{Di}^{rms})^2 \\ P_{VF} = \sum_{i=1}^{4} V_{Fi} I_{Di}^{avg} \end{cases} \tag{32}$$

where,

$$\begin{cases} I_{D1}^{rms} = \frac{nD+1}{\sqrt{1-D}} I_O \\ I_{D2}^{rms} = (\frac{nD+1}{(1-D)^2}) \sqrt{D} I_O \\ I_{D3}^{rms} = \frac{nD+1}{\sqrt{1-D}} I_O \\ I_{D4}^{rms} = \frac{I_O}{\sqrt{1-D}} \end{cases} \tag{33}$$

Moreover, the following are used to calculate the losses of the inductors and CI:

$$P_L = R_{L1}(I_{L1}^{rms})^2 + R_{L2}(I_{L2}^{rms})^2 + R_{N1}(I_{N1}^{rms})^2 + R_{N2}(I_{N2}^{rms})^2 \tag{34}$$

Subsequently, the following is utilized to determine the capacitors' power losses:

$$P_C = \sum_{i=1}^{4} R_i (I_{Ci}^{rms})^2 \tag{35}$$

According to the mentioned formulas, Fig. 7 shows the efficiency curve for different power ranges of the suggested topology based on the duty cycle. Although the efficiency decreases with increasing converter power, the suggested topology is still well-suited for high-power applications and has an acceptable efficiency range. Increasing D to 1 also causes a short circuit on the output side, which means no power goes to the output.

6. Comparing and Analyzing Research Findings

6.1. Comparisons with other topologies

To demonstrate and confirm the beneficial aspects of the proposed topology, a comparative analysis is provided in this section. Table 2 lists the main characteristics of the recommended converter and compares them to similar and comparable topologies. This table summarizes the following briefly: voltage gain, maximum voltage stress among semiconductors, number of power switches, capacitors, and magnetic components. Furthermore, the investigated converter is identical to all of the others in that it has a continuous-current input.

In contrast to the converters discussed in [21] and [22], which use more components overall, the one proposed here uses the same number of elements as the ones listed in [1], [23], and [24]. Even though they include fewer components, the converters in [25], [26], and [27] are completely inferior to the proposed ones in terms of voltage gain and voltage stress on the diodes.

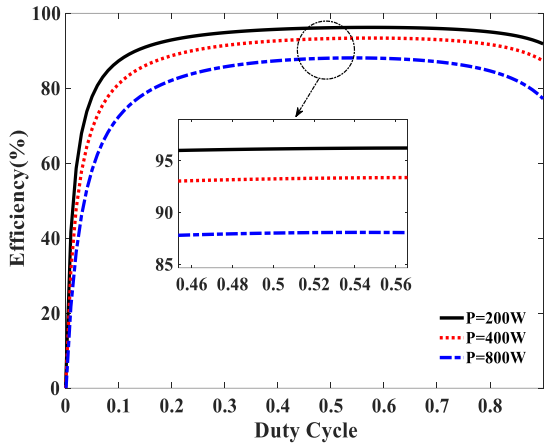

Fig. 7. Theoretical efficiency curve of the suggested topology.

One benefit of this topology is that the suggested converter outperforms other investigated converters at the same power level because it has a single-switch circuit, low voltage stress on the semiconductors, and soft switching conditions on the circuit's diodes, resulting in more efficiency.

Fig. 8 reveals the results of comparing the proposed converter's voltage gain to the other converters of Table 2 (n is considered to be

Table 2. suggested high step-up converter specifications and comparison to comparable topologies.

Converter	Components numeral information	Voltage gain	V_S/V_O	Diodes' maximum voltage stress	Power	Efficiency	Total price
Proposed	S = 1, D = 4, C = 4, L = 2 + 1 CI, T = 12	$\frac{nD+1}{(1-D)^2}$	$\frac{1}{nD+1}$	$\frac{(n-1)D+1}{nD+1}$	205W	95.1%	$33
[1]	S = 1, D = 5, C = 5, L = 0 + 1 CI, T = 12	$\frac{nD+1}{1-D}+2n$	$\frac{1}{n(2-D)+1}$	$\frac{n}{2n+1-nD}$	200W	96%	$30
[23]	S = 1, D = 4, C = 4, L = 3 + 0 CI, T = 12	$\frac{1+D(1-D)}{(1-D)^2}$	1	$\frac{1}{1+D(1-D)}$	200W	92.7%	$34
[21]	S = 1, D = 6, C = 4, L = 1 + 2 CI, T = 14	$\frac{1+nD}{(1-D)^2}$	$\frac{1}{1+nD}$	$\frac{1+n}{1+nD}$	200W	92%	$40
[25]	S = 2, D = 2, C = 2, L = 2 + 0 CI, T = 8	$\frac{1}{(1-D)^2}$	1	1	200W	84%	$24
[24]	S = 2, D = 3, C = 4, L = 3 + 0 CI, T = 12	$\frac{(3D-D^2)}{(1-D)^2}$	$\frac{1}{(3D-D^2)}$	$\frac{1}{(3D-D^2)}$	200W	90%	$35
[22]	S = 2, D = 5, C = 4, L = 1 + 1 CI, T = 13	$\frac{n(2-D)}{(1-D)^2}$	$\frac{1-D}{n(2-D)}$	$\frac{1}{2-D}$	200W	91%	$36
[26]	S = 1, D = 2, C = 2, L = 0 + 1 CI, T = 6	$\frac{2+n-D}{1-D}$	$\frac{1}{2+n-D}$	$\frac{n+1}{2+n-D}$	250W	93.6%	$18
[27]	S = 2, D = 5, C = 3, L = 0 + 1 CI, T = 11	$\frac{n(2-D)}{1-D}$	$\frac{1}{2n(2-D)}$	$\frac{1}{2-D}$	200W	93%	$30

S: Switch, D: Diode, C: Capacitor, L: Inductor, CI: Coupled Inductor, T: Total Number

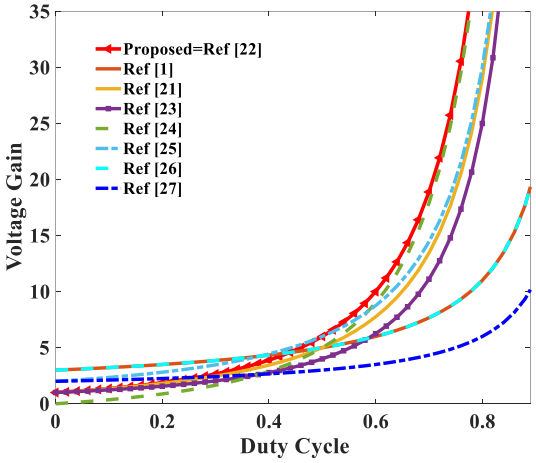

Fig. 8. Output voltage gain of the converters based on the duty cycle with n= 1.

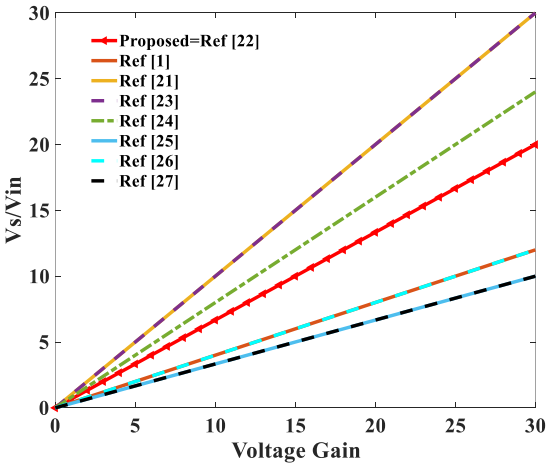

Fig. 10. Voltage stress on the switches as a function of voltage gain (n= 1, D= 0.5).

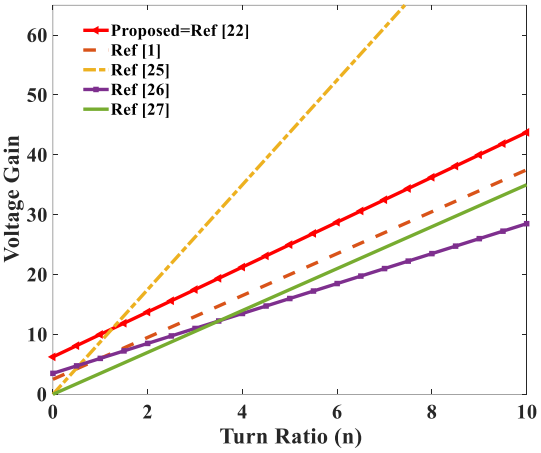

Fig. 9. Voltage gain curve comparison based on the n.

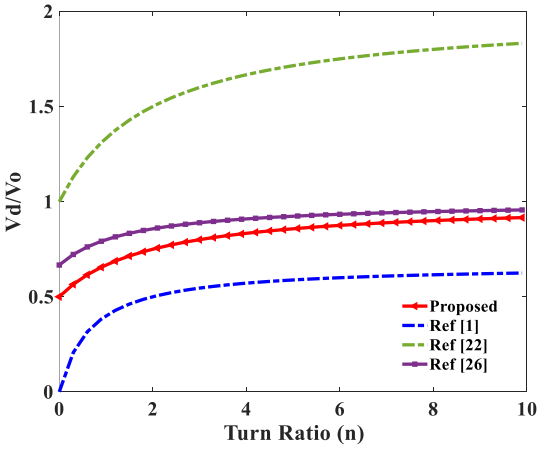

Fig. 11. Maximum normalized voltage stress on diodes for different turn ratios (D= 0.5).

1). The proposed topology outperforms other converters regarding M_{CCM} throughout the appropriate duty cycle range ($0.5 \leq$ D $\leq$ 0.7). Moreover, the suggested converter and the converter described in [21] have the same voltage gain. Nevertheless, as will be shown and examined further down, more research into this converter reveals that the voltage stress on its diodes negatively affects its

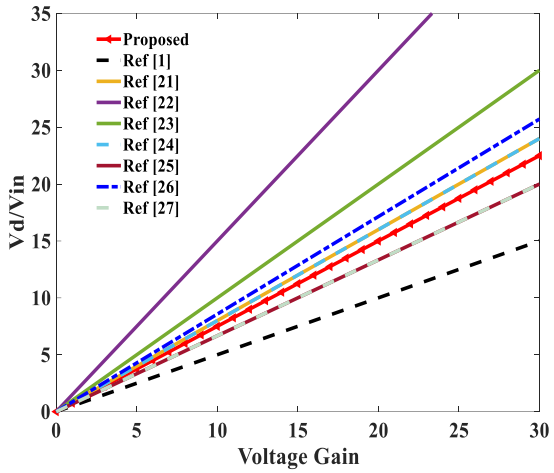

Fig. 12. Maximum voltage stress on the diodes as a function of voltage gain (n= 2, D= 0.5).

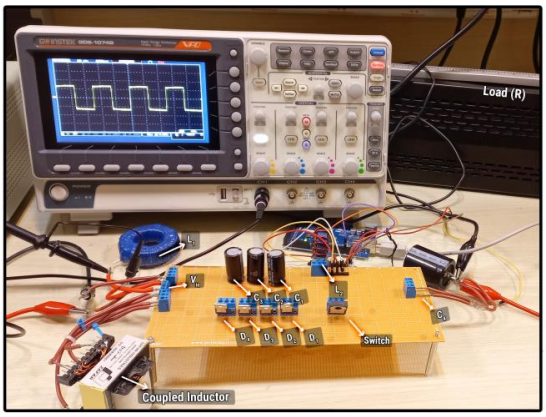

Fig. 13. The experimental setup of the suggested converter.

efficiency.

The proposed circuit and various converters' voltage gains vs. the CI's turn ratios are shown in Fig. 9 ($D = 0.6$). While the CI's turn ratio improves the converters' voltage gains in Table 2, it has a much more noticeable effect in the proposed topology and the one detailed in [22]. Therefore, the suggested converter achieves better voltage gain than competing converters when n is increased. It should be noted that the gain of the converter given in [22] grows at a faster rate than other configurations, but the system's efficiency drops dramatically, limiting its practical use.

Fig. 10 shows a comparison of the voltage stresses on the major switches of converters (V_S/V_{in}) according to the MCCM, which is necessary for a deeper understanding of the proposed circuit's merits. Compared to the converters detailed in references [23], [25], and [24], the proposed converter obviously performs better from this point of view. The converters listed in references [1], [22], [26], and [27] have a lower V_S/V_{in} ratio than the suggested configuration. However, the proposed circuit's increased voltage gain and improved efficiency have made its implementation more practical and feasible.

All other converters, except the converters in [25] and [26], have several diodes built into their design. Hence, comparing the voltage stress on each diode separately would not be feasible or accurate due to their different designs. As a result, the diodes chosen endure the greatest voltage stress, which is often located on the output side of the circuits. The normalized voltage stress on each converter's diodes based on various values of n is shown in Fig. 11. The results show that the suggested topology has a lower V_D/V_O compared to the configurations presented in [21] and [26]. Actually, the diodes' voltage stress is what clearly differentiates the suggested converter from the one in [21]. Fig. 12 also compares converter diodes' gain-determined voltage stresses (VD/Vin). Even here, the suggested converter's maximum diode voltage remains within a tolerable range when compared to competing models. Although the converters mentioned in references [1], [22], and [27] have a lower VD/Vin ratio than the recommended design, the suggested converter is more practical due to its high efficiency and voltage gain. As a result of the comparisons made in this section, the presented converter has the capacity to be useful in many high-power industrial applications.

Moreover, the cost analysis in Table 2 shows that the proposed converter is competitively priced at $34, which compared to the investigated converters, it has a reasonable price. The potential features like high efficiency, high voltage gain, and simplified integration further enhance its value proposition. This makes the proposed converter a suitable option for various applications.

6.2. Discussion on the experimental results

Following the steady-state investigation, this section details the proposed converter constructed in the lab and presents the obtained experimental data. Hence, the operation of the presented circuit was tested by evaluating a 205W prototype under real conditions, as illustrated in Fig. 13 In addition, a switching frequency of 40kHz and a DC input voltage of 20V were specified. An Arduino Mega2560 was also used to generate a pulse width modulation (PWM) signal and manage the power switch for the proposed converter. Table 1 lays out the technical specifications of the converter's elements and explains how the circuit operates. Some of the more noteworthy results from the CCM converter's experiments are shown in Fig. 14. In Fig. 14-(a), the proposed circuit shows its steady-state performance with an input voltage of 20V, a duty cycle of 50%, and an output voltage of 115V, which reaches a voltage gain of around 5.75. This is fairly close to the gain calculated in Eq. (6).

Fig. 14-(b) shows voltage waveforms related to the primary side (V_{N1}) of the CI and the inductors L_1 and L_2. The inductors L_1 and L_2 have voltage values of around 18.5V and 75.4V, respectively, while the primary side of the CI has a voltage of about 38.6V. These values are in agreement with the formulae in Eqs. (1), (2). In accordance with Eq. (8), Fig. 14-(c) also displays the voltage stress waveforms of diodes D_1 and D_2, measuring about 38 and 38.4 volts, respectively. The results demonstrate that these diodes are under minimal voltage stress, with values below $V_O/3$.

The voltage and current stress waveforms of diode D_3 can be observed in Fig. Fig. 14-(d). It can be seen that there is a soft-switching condition in D_3 (ZVS turn on). As seen in Eq. (8), this diode clearly undergoes a voltage stress of 77 volts, and the average current value agrees with Eq. (20). As shown in Fig. 14-(e), Diode D_4 is also affected by the similar circumstance. Getting the ZCS turn-off is proof that D_4 fixed the reverse recovery issue. In addition, at around 78V, the voltage stress of D_4 is less than the V_O. The current stress and voltage findings on this diode perfectly agree with the Eqs. (8) and (20).

For the only power switch, Fig. 14-(f) illustrates the current and the voltage stress waveforms. The average current is in line with Eq. (20), and the voltage on switch S is near 77.5 V, which confirms Eq. (8). Additionally, the results show that the switch has low voltage stress, which is less than V_O. The waveforms associated with the input current and the secondary side of the CI are shown in Fig. 14-(g). It is clear from the waveform of the input current, which is equal to the current through inductor L_1, that the circuit functions in CCM. Also, the input inductor's current ripple shouldn't exceed 30% at its nominal working point. Moreover, consistent with Eq. (2), the voltage on the CI secondary side (V_{N2}) is around 40V.

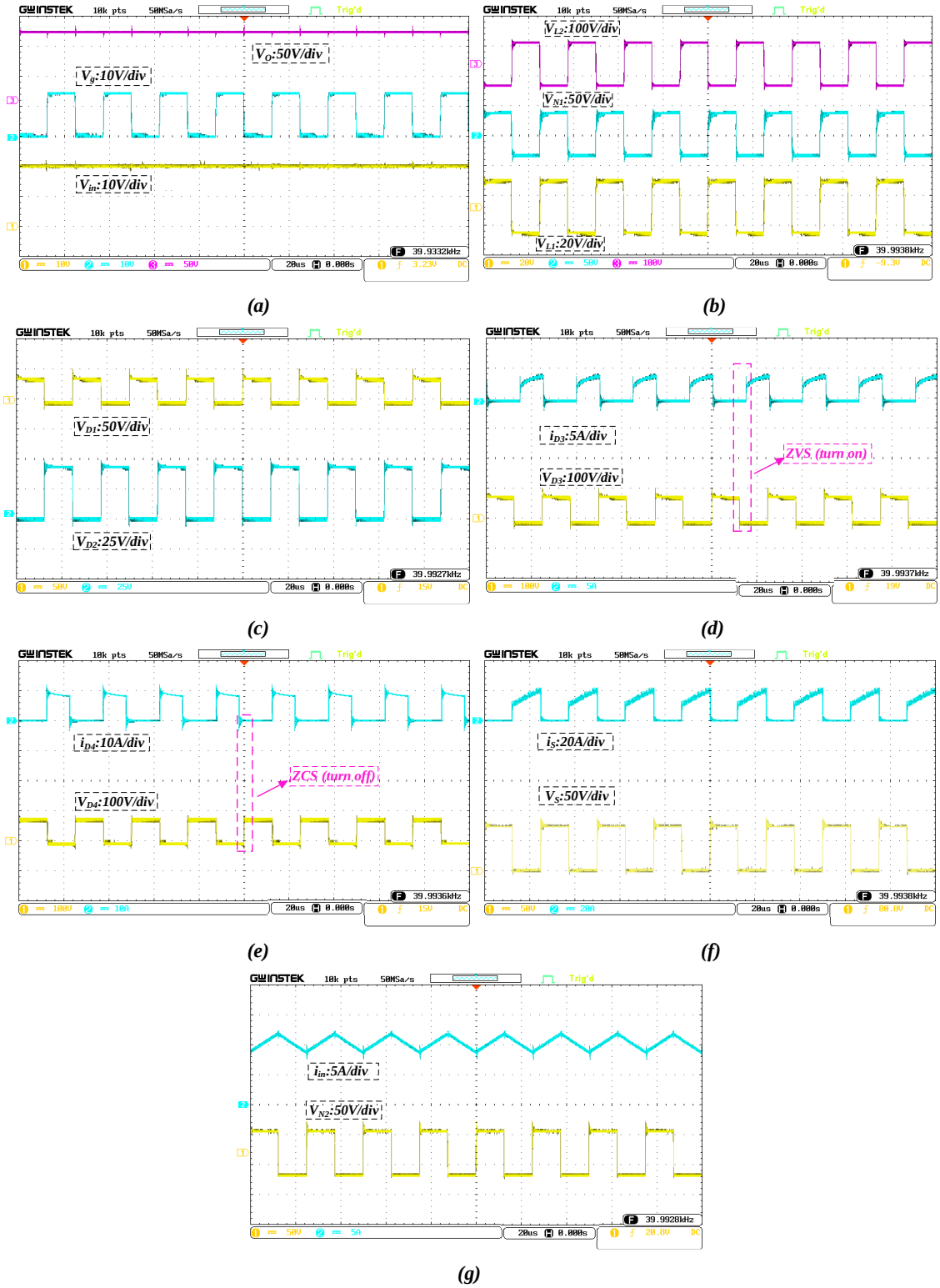

Fig. 14. Experimental waveforms of the suggested converter with V_{in}= 20V, V_O = 115V, P_O = 205W: (a) V_{in}, V_O voltage, and PWM signal from the gate waveforms (b) Inductors voltage waveforms (c) Voltage stresses of D_1, D_2 (d) Soft-switching condition of D_3 (e) Soft-switching condition of D_4 (f) Power switch voltage stress and current waveform (g) Input current and CI's secondary side voltage waveforms.

By applying the power loss analysis over a range of output powers (100 to 500W), we can establish the converter's efficiency and use that information to create the curve shown in Fig. 15. It can be concluded that the results from the experiments and the computations are in agreement (the discrepancies are less than 1% for the majority of the examined conditions). As seen in this figure, the suggested configuration can maintain an efficiency of around 95.1% while producing an output power of approximately

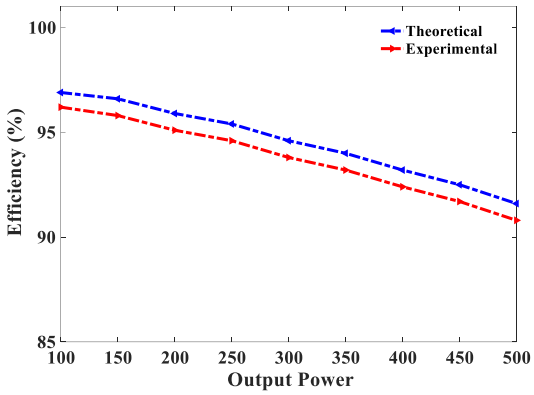

Fig. 15. Proposed converter's efficiency at different output powers.

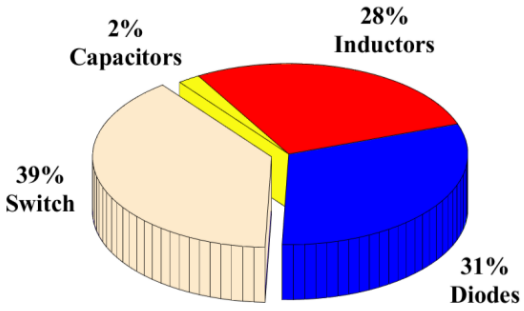

Fig. 16. Investigation of the topology's distribution losses.

205W. On top of that, regardless of the output power set, the converter always maintains an efficiency of over 90%.

Although there are several benefits to the proposed high step-up DC-DC converter, there are also some limitations and conditions that could affect its performance. These include complex closed-loop control designs, variable load conditions, and problems with thermal management. Understanding these constraints allows one to make well-informed decisions about suitable applications and critical design factors to improve performance. Moreover, efficient thermal management is essential for maintaining the converter's performance in the optimal range, especially under high power conditions. Inadequate cooling can lead to overheating of components, reducing efficiency and potentially causing failure. Furthermore, the proposed distribution of converter losses is shown in Fig. 16. This follows from the calculations done in section 5. In contrast to the obviously more troublesome semiconductors, capacitors lose the least amount of power.

7. CONCLUSION

This study introduces a novel designed high voltage gain DC-DC converter incorporating a CI and an HVMC. This topology's high voltage gain is achieved by comparatively mild voltage stress on the single switch and diodes, which results in a relatively large output voltage. The majority of the diodes also had a voltage stress lower than $V_O/2$. The recommended converter's diodes have the capacity to soft-switch, which has improved the total efficiency. Due to its common ground and constant input current, the suggested topology might suit applications using renewable energy sources. The configuration's high efficiency, simple topology, and enhanced flexibility in design are other advantages. The suggested circuit's operation principles have been thoroughly examined, and its performance has been compared to similar converters. Theoretical analysis is proven right by experimental discoveries, and a 205W prototype is built in the end.

ACKNOWLEDGMENTS

This work has been financially supported by the research deputy of University of Mohaghegh Ardabili. The grant No. was 1402.d.9.5071.

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