Research Paper

A Voltage Multiplier Based DC-DC Converter with Reduced Switch Stress and Ultra-High Voltage Gain

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Abstract— *A novel interleaved non-isolated high-gain topology is presented in this article. This converter reaches its significant gain by combining two voltage multiplier cells (VMCs), a built-in transformer (BIT) with two windings, and coupled inductors (CIs) with two windings. Leakage inductance energy recovery, reduction of input current ripple, flow sharing by interleaved technique, increased flexibility in design by improving the conversion ratio of built-in transformer and coupled inductance, power masts turned on under zero current switching (ZCS), also switched off for Diodes are features of this topology. A voltage of 20V was applied to the simulated topology. As a result, a load output voltage of 533V was achieved, and an output power of 320 watts was generated.*

Keywords—DC-DC converter, built-in transformer, coupled inductor, voltage multiplier, high step-up.

NOMENCLATURE

Abbreviations

Δi_{in}	Ripple input current
f_{SW}	Switching frequency
BIT	Built-in transformer
CI	Coupled inductor
CWM	Cockcroft-walton multiplier
DM	Dickson multiplier
EMI	Electromagnetic interference
MOSET	Metal–oxide–semiconductor field-effect transistor
SC	Switched-capacitor
SCVM	Switched capacitor voltage multiplier
VMC	Voltage multiplier cell
ZCS	Zero current switching
ZVS	Zero voltage switching

1. INTRODUCTION

Power electronics converters have attracted the attention of scientists due to their applications in renewable energy for efficiently converting and managing energy from renewable sources like solar and wind power [1], for provide smooth power transmission between the transmitter and receiver without the need for physical connections, wireless power transfer (WPT) systems rely on power electronics converters to effectively convert and control energy [2], LED drivers are power electronics converters specifically designed to regulate the electrical current supplied to LED lighting systems, ensuring optimal performance and efficiency while protecting the LEDs from fluctuations in voltage and current [3], additionally, electric vehicles rely on power electronics converters for the conversion and transfer of energy from batteries to the motor [4]. In recent years, environmentally friendly energy sources such as fuel cells and photovoltaics, which do not emit CO_2 or cause pollution, have gained attention. However, their voltage output is often much lower (around 20-50 V) than the typical voltage range of DC-link systems (400-720 V). Voltage boost converters fill this voltage gap [5].

While DC-DC boost converters have a high voltage gain, they often have a duty cycle near unity, which can cause stresses on switches and diodes. These stresses result in problems such as reverse recovery of the output diodes, high current ripple in the input inductor, and high voltage ripple in the output capacitors, leading to significant losses. Various boosting techniques have been proposed to address these issues and increase voltage gain [6, 7]. These techniques include switched-capacitor, switched-inductor (also known as a multiplier), built-in transformer (BIT), coupled inductors (CIs), hybrid boost converters structure similar to Cockcroft-Walton multiplier (CWM), Dickson multiplier (DM), voltage doubler, and switched-capacitor voltage multiplier (SCVM) [8, 9]. Although some of these methods increase voltage gain and reduce voltage stress by increasing the duty cycle, they also increase input current ripple, which can reduce the lifespan of renewable energy sources and converter components [10, 11]. Additionally, increasing the voltage gain often requires the use of a large number of energy storage components, increasing converter costs. Therefore, it is essential to apply these techniques wisely to enhance voltage gain and power density while considering economic aspects [12].

CI or BIT allows greater flexibility and increased voltage gain by adjusting the turn ratio in high-voltage step-up converters. However, this approach can lead to problems like switch voltage spikes due to leakage inductance, resulting in efficiency loss. To address this, converters incorporate active or passive clamp topologies to manage the leaked energy. Increasing the conversion ratio of CIs and BIT in high-voltage applications can boost voltage gain but at the cost of larger windings and reduced power density [13, 14].

In general, there are differences between CIs and BIT. The BIT transfers power instantly, has a gapless core, and provides electrical isolation. On the other hand, CIs transfer power in the second half-cycle, there is an air gap in its core, and it does not offer electrical isolation. However, both devices transmit power through coils [13, 15]. The combination of BIT, CI, and VMC has created a converter with very high voltage gain . In this case, it is easy to increase the voltage gain of the converter by adjusting its turn ratios with a fixed duty cycle or the number of switched-capacitor (SC) cells, and it is also possible to recover the leakage energy created by the capacitors. The problem of reverse recovery of diodes is largely mitigated with the help of leakage inductances. Some examples of these single-phase converters are presented in these articles [16, 17].

The converter proposed in [18] utilizes coupled inductance. Its voltage gain is advantageous, and the diodes operate under zero-voltage switching (ZVS) and zero-current switching (ZCS). However, the MOSFET power switch operates under hard switching conditions. By using resonant circuits, the power MOOSFETs are turned-off or -on under ZCS, ZVS or ZVCS conditions [19, 20]. In [21], which is introduced for applications involving renewable energy sources, the voltage gain increases with the coupled inductance conversion ratio. This also reduces the voltage stress on the switch. Unfortunately, increasing the conversion ratio of the coupled inductance leads to higher leakage inductance and decreased efficiency. Fortunately, leakage energy can be absorbed by using active or passive clamps and voltage stress can be decreased [22]. A symmetrical converter featuring a combination of CIs and VMCs with high voltage gain is introduced in [23]. The power switches operate under hard-switching conditions, while the diodes operate under zero-current switching (ZCS) and zero-voltage switching (ZVS) conditions. Unfortunately, the absence of a common ground increases EMI problems. Capacitive coupling or common mode filters are two ways to attenuated EMI noise. Additionally, the features mentioned in [23], the [24] converter employs ZVZCS soft switching for power MOSFETs. This results in reduced losses, increased efficiency, and greater flexibility in increasing the frequency. Fortunately, there are no disadvantages of revised literature converters in the proposed converter. The combination of a BIT, CIs, and two VMCs has created a converter with a high voltage gain. The reduction of the input current ripple and the current sharing is achieved by the interleaved technique. Power MOSFETs are turned-on under soft switching and diodes are turned-off. Among the benefits of the proposed converter are relieving the problem of reverse recovery of diodes by the presence of leakage inductances, as well as leakage energy recovery.

In summary, the proposed converter offers several advantages:

- Achieves high voltage gain.
- Reduces EMI through the use of a common ground.
- Decreases thermal losses and input current ripple thanks to the interleaved technique.
- Enables ZCS during MOSFET switch turn-on.
- Mitigates diode reverse recovery issues due to leakage inductance.
- Provides enhanced design flexibility.

In this article, Section 2 discusses the proposed converter's principles. Section 3 includes the steady-state operating modes of the proposed converters. Section 4 presents the analysis of the suggested converter. Section 5, comparison of several parallel converters. Section 6 shows PSpice/OrCAD simulation results. Finally, the conclusion is written in Section 7.

2. OPERATION PRINCIPLES OF THE SUGGESTED CONVERTER

The circuit diagram of the suggested converter for n-stages is shown in Fig. 1. This converter includes coupled inductors (CIs) with two windings, a built-in transformer (BIT) with two windings, and two voltage multiplier cells (VMCs).
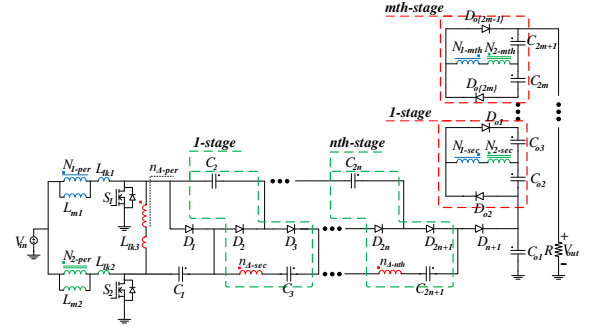

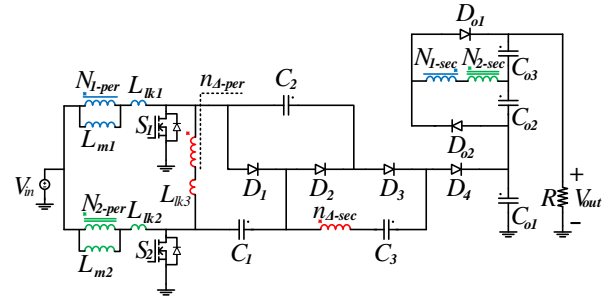Fig. 1. Structure the suggested converter for n, m-stage.

Fig. 2. Equivalent circuit of the proposed converter.

In this topology, interleaved technology is used to reduce the current ripple. The secondary winding of the CIs is connected in series, increasing the voltage gain. In this converter, The CIs are modeled as an ideal transformer, leakage inductance, and magnetizing inductance. Coupled inductors (CIs) have a turn ratio $(N_{1\text{-}sec}/N_{1\text{-}pri} = N_{2\text{-}sec}/N_{2\text{-}pri} = \alpha)$. The built-in transformer (BIT) consists of one core and two windings, which transfer more power and increase the voltage gain. The switched capacitor (SC) cell consists of two capacitors, two diodes, and the secondary winding of the BIT core. Also, the VMC, placed directly on the load, includes two diodes, two capacitors, and two secondary series windings of the CIs. In this case, one winding is added to the coupled inductors with each step increase. The built-in transformer's (BIT) turn ratio $(n_{\Delta-\sec}/n_{\Delta-pri} = \beta)$. To identify the windings more quickly, they have been personalized with specific colors and marked as "$\star$", "$\star$", and "$\star$". The converter must operate in continuous conduction mode for the desired voltage gain, which requires a duty cycle greater than 0.5.
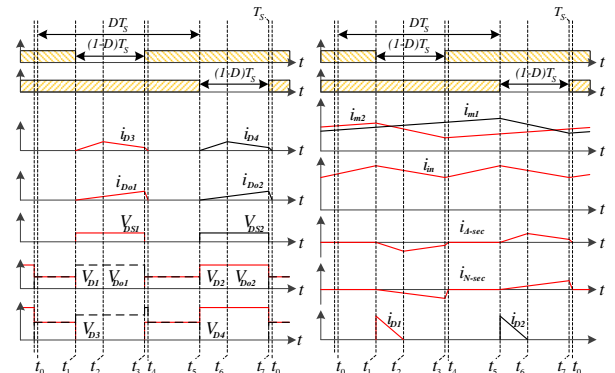

Fig. 3. The keys waveform.

3. OPERATIONS MODES OF THE PROPOSED CONVERTER

State 1[t_0-t_1]: When both power switches S_1 and S_2 are turned on, and all diodes are in a reverse-biased state, the input source begins to charge the magnetizing inductance L_{m1} and the leakage inductance L_{lk1} via switch S_1, as well as L_{m2} and L_{lk2} via switch S_2. V_{lk1} and V_{lk2}, due to their negligible significance, have been excluded from consideration:

$$v_{Lm1} = v_{Lm2} = V_{in} \tag{1}$$

$$V_{out} = V_{Co1} + V_{Co2} + V_{Co3} \tag{2}$$

State 2[t_1-t_2]: At $t = t_1$, switch S_1 is in the 'OFF' state, and diodes D_1, D_3, and D_{o1} are forward biased. The input DC source charges L_{m2} and L_{lk2} with switch S_1, and L_{m1} and L_{lk1} transfer their energy. Capacitor C_1 clamps the voltage stress of switch S_1. The current L_{lk1} charges the capacitor C_1. the secondary of the coupled inductors (CIs) stores its energy from the diode D_{o1} in the capacitor C_{o3}. Capacitor C_2 transfers energy from diode D_3 to capacitor C_3 and the BIT's secondary winding.

$$v_{Lm1} = V_{in} - V_{\Delta-pri} \tag{3}$$

$$v_{Lm2} = V_{in} \tag{4}$$

$$V_{C1} = V_{\Delta-pri} \tag{5}$$

$$V_{C3} - V_{C2} = \beta V_{\Delta-pri} \tag{6}$$

$$V_{Co3} = \beta V_{\Delta-pri} \tag{7}$$

$$i_{D1}(t) = i_{lk1}(t) + i_{\Delta-sec}(t) + i_{\Delta-pri}(t) = \\ i_{lm1}(t) - i_{N1-pri}(t) + (\beta+1)i_{\Delta-sec}(t) \tag{8}$$

State 3[t_2-t_3]: At this moment, the current flowing through D_1 gradually decreases until it reaches zero, causing the diode to turn off naturally. Consequently, this process partially mitigates the diode reverse recovery issue. During this phase, the current in the leakage inductance L_{lk1} equals the combined currents passing through capacitor C_3 and the built-in transformer's (BIT) primary winding. Additionally, the current i_{lk1} discharges capacitor C_2 while simultaneously charging capacitors C_1 and C_3. The relationships between these elements are as follows:

$$v_{Lm1} = V_{in} - V_{\Delta-pri} \tag{9}$$

$$v_{Lm2} = V_{in} \tag{10}$$

$$v_{C3} - v_{C2} = \beta V_{\Delta-pri} \tag{11}$$

$$v_{Lm1} = V_{in} - V_{C1} \tag{12}$$

$$V_{\Delta-pri} = V_{C1} \tag{13}$$

$$i_{Lk1}(t) = i_{Lm1}(t) - i_{N1-pri}(t) = \\ (\beta+1)i_{\Delta-sec}(t) \tag{14}$$

State 4[t_3-t_4]: Referring to Fig. 4-(d), both switches are in the 'ON' state, and the presence of L_{lk1} acts as a limiter that prevents abrupt changes in current. In this scenario, zero current switching (ZCS) occurs when the switch is turned on. The current through D_3 decreases, regulated by L_{lk1} to mitigate D_3's reverse recovery issue. Similar behavior is observed for diode D_{o1}.

$$\frac{di_{D3}(t)}{dt} = -\frac{V_{C1} + V_{C3} - V_{C2}}{k^2 L_{lkb}}; \\ \frac{di_{Do1}(t)}{dt} = -\frac{V_{Co3}}{K^2(L_{lk1} + L_{lk2})} \tag{15}$$

State 5[t_4-t_5]: In Fig. 4-(e), the current through diode D_3 gradually reduces to zero, resulting in the diode turning off—subsequently, the operation proceeds following the same pattern as in Mode 1.

State 6[t_5-t_6]: In Fig. 4-(f), switch S_2 is in the 'OFF' state, causing diodes D_2, D_4, and D_{o2} to become forward-biased. The input DC source charges L_{m1} and L_{lk1}. Energy from L_{m2} and L_{lk2} is transferred. The voltage difference $V_{C2} - V_{C1}$ serves to limit the voltage stress on switch S_2. The leakage inductance current i_{lk2} discharges capacitor C_1, while the secondary winding current of the built-in transformer (BIT) increases linearly. In this configuration, capacitors C_1 and C_3, along with the secondary winding of the built-in transformer, supply capacitor C_{o1}. Energy from diode D_{o2} is stored in capacitor C_{o2} via the secondary winding of the CIs, with the leakage inductance helping somewhat to alleviate the reverse recovery issue of diode D_{o2}.

$$v_{Lm1} = V_{in} \tag{16}$$

$$v_{Lm2} = v_{in} - V_{\Delta-pri} \tag{17}$$

$$V_{Co1} = V_{C1} + V_{C3} + (\beta+1)V_{\Delta-pri} \tag{18}$$

$$V_{out} = V_{Co1} + V_{Co2} + V_{Co3} \tag{19}$$

State 7[t_6-t_7]: The current through diode D_2 gradually decreases to zero, allowing the diode to naturally turn off. As a result, the reverse recovery issue associated with diode D_2 is significantly alleviated. In this situation, the leakage inductance current, i_{lk2}, equals the sum of the built-in transformer's winding currents ($i_{\Delta-sec} + i_{\Delta-pri}$).

$$v_{Lm1} = v_{in} \tag{20}$$

$$v_{Lm2} = v_{in} - V_{\Delta-pri} \tag{21}$$

$$V_{\Delta-pri} = \frac{V_{Co1} - V_{C1} + V_{C3}}{\beta + 1} \tag{22}$$

$$i_{Lk2}(t) = i_{Lm2}(t) - i_{N2-pri}(t) = \\ i_{\Delta-pri}(t) + i_{\Delta-sec}(t) = (\beta+1)i_{\Delta-sec}(t) \tag{23}$$

State 8[t_7-t_8]: In this operational mode, at time t_7, switch S_2 is in the 'ON' state, with leakage inductance L_{lk2} moderating the rate of current change. Consequently, the switch undergoes a
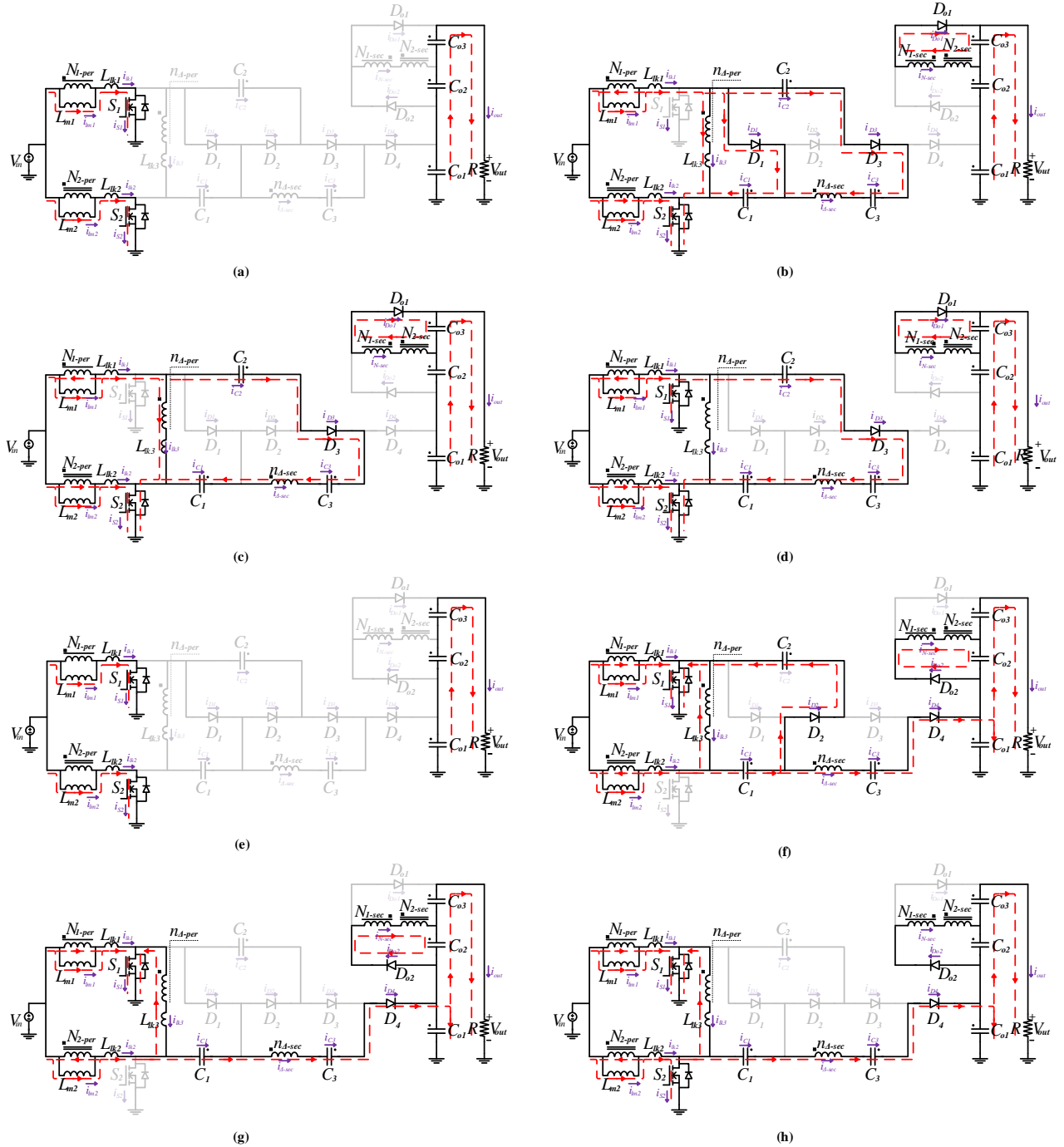
Fig. 4. Equivalent circuits for operation modes: a_Mode1, b_Mode2, c_Mode3, d_Mode4, e_Mode5 , f_Mode6, g_Mode7, h_Mode8.

gradual turn-on process, leading to zero-current switching (ZCS) at the startup moment. During this period, the currents flowing through diodes D_4 and D_{o2} experience a controlled reduction, thanks to the influence of leakage inductance L_{lk2}. As a result, the reverse recovery issue associated with these diodes is significantly alleviated.

$$\frac{di_{D4}(t)}{dt} = -\frac{V_{Co1} - V_{C1} + V_{C3}}{\beta^2 L_{lkb}};$$
$$\frac{di_{Do2}(t)}{dt} = -\frac{V_{Co2}}{\alpha^2(L_{lk1} + L_{lk2})} \qquad (24)$$

4. STEADY-STATE ANALYSIS

4.1. Voltage gain

First, determine the voltage across the capacitors by applying the balanced volt-second principle to L_{m1} and L_{m2}, resulting in the following relationships:

$$V_{lm1}^{OFF}(1-D)T + V_{lm1}^{ON}DT = 0$$
$$V_{lm2}^{OFF}(1-D)T + V_{lm2}^{ON}DT = 0 \qquad (25)$$

$$V_{C1} = \frac{V_{in}}{1-D}; V_{C2} = \frac{2V_{in}}{1-D}; V_{C3} = \frac{(\beta+2)V_{in}}{1-D} \qquad (26)$$

$$V_{Co1} = \frac{(2\beta + 4)\,V_{in}}{1 - D}; V_{Co2} = V_{Co3} = \frac{\alpha V_{in}}{1 - D} \qquad (27)$$

$$M = \frac{V_o}{V_{in}} = \frac{2\beta + 2\alpha + 4}{1 - D} \qquad (28)$$

4.2. Voltage stress

The voltage stress of semiconductor elements is obtained as follows:

$$V_{S1} = V_{S2} = \frac{V_{in}}{1 - D} = \frac{V_o}{2\beta + 2\alpha + 4} \qquad (29)$$

$$V_{C1} = \frac{V_o}{2\beta + 2\alpha + 4}; V_{C2} = \frac{V_o}{\beta + \alpha + 2}; V_{C3} = \frac{\beta + 2}{2\beta + 2\alpha + 4}V_o$$
$$V_{Co1} = \frac{2\beta + 4}{2\beta + 2\alpha + 4}V_o; V_{Co2} = V_{Co3} = \frac{\alpha V_o}{2\beta + 2\alpha + 4} \qquad (30)$$

$$V_{D1} = V_{D2} = \frac{V_o}{\beta + \alpha + 2}$$
$$V_{D3} = \frac{(\beta + 1)\,V_o}{\beta + \alpha + 2}; V_{D4} = \frac{(2k + 1)\,V_o}{2\beta + 2\alpha + 4} \qquad (31)$$
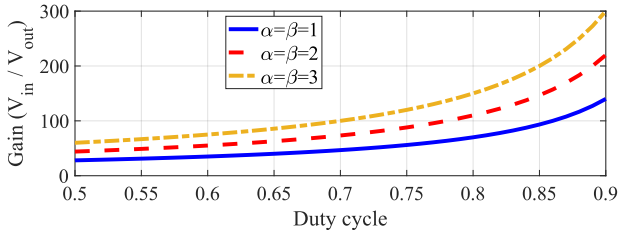$$V_{D5} = V_{D6} = \frac{2kV_o}{2\beta + 2\alpha + 4}$$

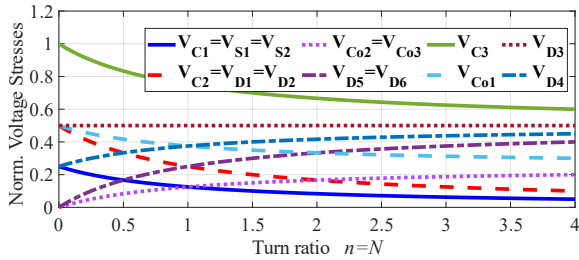Fig. 5. The suggested converter's voltage gain.

Fig. 6. The proposed converter's normalized voltage stress for components.

As it is clear from the voltage stress equations for diodes, switches, and capacitors, with the increase in the turn ratio of the built-in transformer (BIT) and the coupled inductors (CIs), the voltage stress on these elements decreases, which is one advantage of the proposed converter.
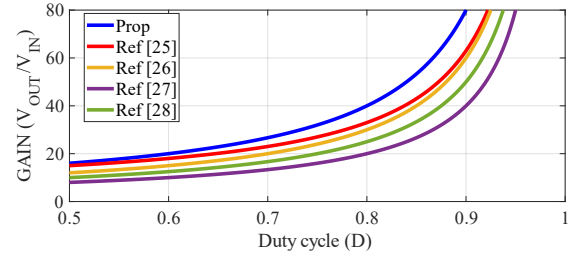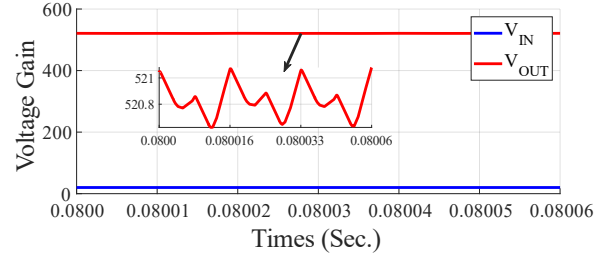

Fig. 7. Comparison of voltage gain.

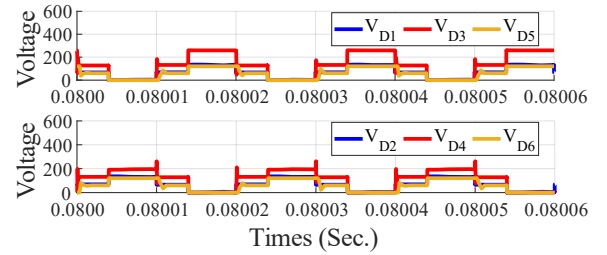Fig. 8. Display results of input/output voltage.

Fig. 9. Display results of applied voltage to diodes in reverse baias.
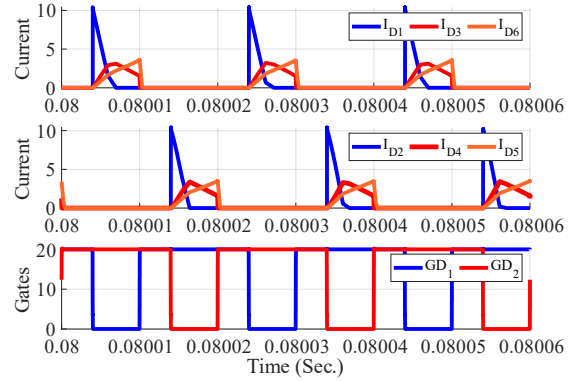

Fig. 10. Display result of current through diodes in forward baias.

5. PERFORMANCE COMPARISON

The suggested converter is examined alongside other comparable converters in this paper. All converters included the interleaved technique and high step-up. The converters have been analyzed from the perspectives of voltage gain, circuit complexity, normalized voltage stress on diodes and switches, common ground, and input current sharing, as categorized in Table 1.

Despite having more elements than converters [25–27], the proposed converter outperforms them regarding normalized voltage stress and voltage gain, particularly within the same cycle ratio and duty cycle. The converter that has been proposed comes with various features, such as common ground and balanced current

Table 1. Performance comparison.

Topologies	Proposed	Ref. [24]	Ref. [25]	Ref. [26]	Ref. [27]
Voltage gain	$\dfrac{4\left(\frac{\beta}{2}+\frac{\alpha}{2}+1\right)}{1-D}$	$\dfrac{5-2\beta D+4\beta-D}{1-D}$	$\dfrac{4\left(1+\frac{\beta}{2}\right)}{1-D}$	$\dfrac{4\left(\frac{\beta}{2}+\frac{1}{2}\right)}{1-D}$	$\dfrac{4\left(\frac{\beta}{2}+\frac{3}{4}\right)}{1-D}$
Norm. voltage stress of switches	$\dfrac{1}{2\beta+2\alpha+4}$	$\dfrac{V_o}{5-2\beta D+4\beta-D}$	$\dfrac{1}{2\beta+4}$	$\dfrac{1}{2\beta+2}$	$\dfrac{1}{2\beta+3}$
Max. norm voltage stress of diode	$\dfrac{\alpha+1}{\alpha+\beta+2}$	$\dfrac{(\beta+1)V_o}{5-2\beta D+4\beta-D}$	$\dfrac{\alpha+1}{\alpha+2}$	$\dfrac{\alpha}{\alpha+1}$	$\dfrac{2\alpha+1}{2\alpha+3}$
N. of diodes	6	6	4	4	4
N. of capacitors	6	9	4	4	4
N. of windings	6	4	4	4	4
N. of switches	2	2	2	2	2
Common ground?	Yes	No	Yes	No	Yes
Balanced current?	Yes	Yes	Yes	Yes	No

Table 2. Specifications and component values of implemented circuit.

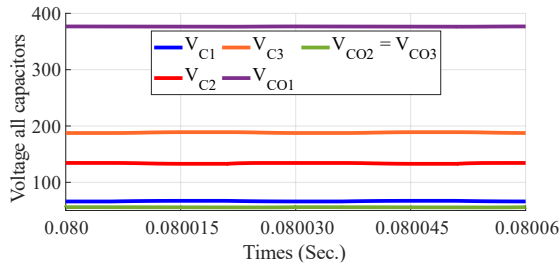| Converter's components	Parameters
Output power (P_{out})	320W
Input/output voltage ($V_{in}-V_{out}$)	20V-520V
Duty cycle (D)	0.7
Magnetizing inductances of CIs	100μH
Magnetizing inductances of BIT	400μH
C_1	22μF
C_2,C_3	8.2μF
C_{o1},C_{o2},C_{o3}	56μF
L_{lk1},L_{lk2}	3μH
L_{lk3}	2.5μH

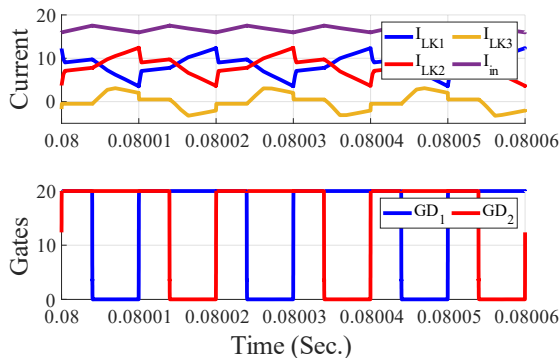Fig. 11. Display result of capacitors across voltage.

Fig. 12. Display result of input source current and leakage inductance.
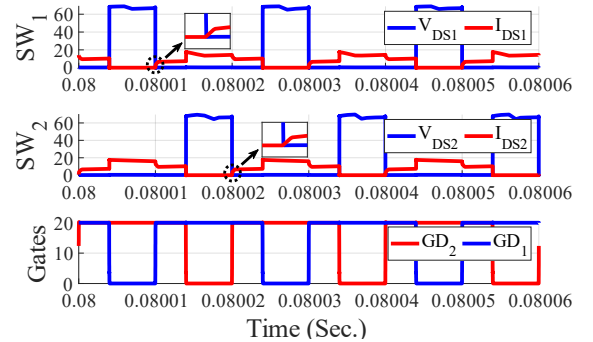

Fig. 13. Display result zero-current switching (ZCS) condition for power switches.

output voltage, enabling the use of a switch with a lower voltage rating and lower conduction losses. Additionally, the maximum voltage stress on the diode in the proposed converter is lower than that in all the compared converters, further enhancing its appeal. The proposed converter has a common ground, thereby reducing EMI, a feature not present in [24] converters.

6. SIMULATION RESULTS

We have simulated it with the help of the PSpice/OrCAD. The key parameters are outlined in Table 2. The simulation results with V_{in} = 20V are shown in Figs. 8-13. The duty cycle equals $D = 0.7$, and the turn ratio of the built-in transformer (BIT) and the coupled inductors (CIs) are considered $\alpha = \beta = 1$. The calculated voltage gain, assuming ideality, is similar to 26.6. The calculated voltage and current are 533 volts and 0.66 amperes, respectively.

In the simulation in Fig. 8, the output voltage measures 521 volts, with a deviation of 12 volts between the expected and actual values. This discrepancy may be attributed to the simulated components' leakage inductances and internal resistances.

Fig. 9 illustrates that the voltage across diodes D_1 and D_2 is approximately 130 volts, diodes D_3 and D_4 register around 256V and 192V, while diodes D_{o1} and D_{o2} show roughly 121V. This also verifies the correctness of Eq. (31). Fig. 10, displays the behavior of the diode current, demonstrating that the issue of diode reverse recovery has been effectively resolved thanks to the presence of leakage inductances.

Fig. 11, also shows the voltage of the capacitors. The voltages of the capacitors storing energy (C_1, C_2, C_3) is 66V, 121V, and 192V, respectively. The voltage of the capacitors transferring power

sharing, whereas converters [26, 27] lack these capabilities. The voltage stress is significantly lower than that in other reviewed articles. Due to ZCS at the moment of turn-on, switching losses are reduced, allowing greater flexibility in increasing the frequency. Additionally, the voltage stress is substantially lower than the

to the load (C_{o1}, C_{o2}, C_{o3}) are 382V, 60V and 60V, respectively. These values have been determined, which shows the correctness of the Eq. (30) of the voltage of the capacitors.

Fig. 12, shows the source's input and leakage inductance currents. As illustrated, the input current is evenly distributed. By using a two-phase interleaved technique, the input current has a small ripple, and the frequency Δi_{in} is twice f_s.

Referring to Fig. 13, it can be asserted that the power switches S_1 and S_2 are engaged under Zero Current Switching (ZCS) conditions. This operation significantly reduces switching losses, enhances overall efficiency, and provides greater flexibility for increasing the switching frequency.

7. CONCLUSION

The article presents a unique DC-DC converter for distributed energy systems, utilizing high-step-up and interleaved technique. The converter integrates several critical components: a built-in transformer (BIT), coupled inductors (CIs), and two voltage multiplier (VM) cell. These elements synergistically enhance voltage gain while reducing voltage stress on components. The innovative combination of these techniques, coupled with design flexibility, results in superior voltage gain. Moreover, the proposed converter operates in continuous conduction mode and utilizes interleaved ripple techniques to mitigate input current fluctuations, thereby reducing component stress. Three notable advantages of these techniques are reducing voltage stress on switches, achieving lower voltage-rated switches to minimize conduction losses, and alleviating the reverse recovery problem in diodes, achieved through leakage inductances. The article provides detailed insights into the proposed converter's operational modes, steady-state analysis, and practical comparisons. In a simulated scenario, a 320W converter with a voltage gain of 26.6 and an output voltage of 520V is presented, with simulation results confirming the theoretical relationships and the converter's performance.

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