Journal of Operation and Automation in Power Engineering

Vol. XX, No. XX, Dec. 2022, Pages: XXXX (Proofed)

http://joape.uma.ac.ir

Research Paper

Development and Optimization of High-Power and Medium-Voltage Battery Energy Storage System Based on CHB Converter

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Abstract— *Battery energy storage systems have become an integral part of electrical systems in various applications, including stabilizing and increasing the reliability and efficiency of utility grids, and they play an essential role in directly injecting the power generated from renewable sources into the grid. Therefore, investigating and conducting extensive research on various aspects of BESS, such as development, optimization, production, and installation, is essential. One of the challenges of using low-voltage BESS for medium-voltage and high-power applications is that, since two and three-level converters are not able to generate high voltage and also inject high power into the utility grid, it is necessary to utilize step-up transformers, which apart from being bulky, large and expensive, also cause damage to the system. Therefore, multi-level topologies are needed. Hence; this paper describes the development process of a 20-kV and 8-MW BESS based on a cascaded H-bridge converter with a focus on optimization of the most crucial system parameters, including switching loss in semiconductors, LCL filter, and DC-link capacitor by using Pareto Front method to minimize the overall loss, which leads to better performance and high efficiency. To verify the proper performance of the control strategy and evaluation of output results, the optimized system has been simulated in MATLAB/SIMULINK, and the system waveforms have been presented and discussed.*

Keywords—Cascaded H-Bridge, energy storage system, multi-objective optimization, state-of-charge balancing.

1. INTRODUCTION

Due to environmental issues and the continued depletion of fossil fuel reserves, there is a great interest in renewable energy sources such as wind turbines and solar power. Connecting these large and intermittent power sources to the power grid can adversely affect voltage/frequency regulation and cause serious power quality issues [1], [2]. Conventional energy sources cannot meet the increasing demand in real-time, and renewable energy sources are available intermittently. Due to these reasons, modern technologies, such as storage systems can improve power quality by powering the grid, storing the energy produced, and making it available when needed [3].

Therefore, a storage device is essential to compensate for fluctuations in active power. When wind turbines generate above-average power for long periods, energy storage systems store excess energy from the power grid. On the other hand, if the generator's output is low, it will supply insufficient power to the grid. This is called "power leveling" and dramatically improves the power reliability, quality, and stability of the grid [4].

Energy storage systems based on different technologies were considered in [5], and [6]. Besides power balancing, energy storage systems have been viewed as "load balancing" the peak power demands of elevator drives and electric vehicles. So far, several kinds of energy storage systems have been utilized in power systems such as batteries, super-capacitors, flywheels, pumped hydro, compressed hydrogen storage, static synchronous compensators, and compressed air energy storage [7], [8]. One of the most common applications of battery energy storage systems (BESS) is connecting them to utility grids for various purposes. The BESS is connected to a voltage source converter (VSC) to share active and reactive power in grid-connected mode [9].

Nowadays, the need to use medium voltage and high power energy storage systems is evident due to their excellent performance. Among all different topologies, multi-level converters are the best option for high levels of voltage and power delivered to the utility grid [10]. Multi-level topologies have both advantages and different challenges. Producing staircase output voltage, which requires many isolated DC voltages, and implementing a precise and effective control method can be considered as challenges [11], [12]. On the other hand, low THD, low voltage stress of switches, and less conduction losses are among the advantages of multi-level converters [13–15]. Among various types of multilevel converters, the CHB converter brings up more privileges such as modularity and economy, making it one of the best options for energy storage systems. Moreover, the cascade converter topology allows the BESS to be connected directly to the medium voltage grid without the use of a step-up transformer. Each H-Bridge converter coordinates the power flow of each battery (or battery bank) concerning the DC link. For this reason, CHB is primarily used in high-performance applications.

Utilizing an optimization process is one of the best and most effective ways of developing such storage systems. By applying multi-objective optimization, the most optimal parameters of the designed battery energy storage system can be obtained, which leads to high efficiency and the lowest overall loss. The parameters

Received: 29 Apr. 2024
Revised: 16 Jul. 2024
Accepted: 20 Jul. 2024
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DOI: 10.22098/joape.2024.13040.1989

chosen for optimization in this paper include; LCL filter capacitor value to improve power quality, DC-link capacitor value, and the number of H-Bridge cells per phase for specifying the output voltage level.

In [16] and [17], authors described a high-power BESS based on CHB in which the number of H-Bridge blocks per phase was determined by using a simple equation, however, the innovative idea of this paper is to determine the number of converter output levels in a way that the overall loss is minimized. In addition, other vital parameters of the system, such as the DC-link capacitor and the value of the line filter capacitor have simultaneously been optimized based on the design procedure. However, the value of the line filter capacitor in [2] and [18] is obtained through primitive ways, which is not optimal.

This paper focuses on the development and optimization of a 20 kV BESS based on a three-phase cascaded H-Bridge multilevel PWM converter (CHBM-PWM) in star configuration by using a multi-objective optimization (MOO) algorithm. The novelty of this paper is that we have used a powerful and comprehensive multi-objective optimization algorithm, which has not been used or discussed in any other related papers, [2] and [19] for instance, to make the overall performance of the system much better, by reducing the volume and size of the LCL filter capacitor as well as DC-link capacitor. Another significant novelty of this paper is the selection of the semiconductor switches based on an optimization algorithm. In contrast, [18] carried out an experimental test to select power semiconductors which is not optimal.

This paper is structured as follows. Obtaining Performance Indices for Optimization of a 3-Phase grid-connected CHB Converter is discussed in Section 2. Optimization results are presented and discussed in Section 3. The system control strategy is described in Section 4. This is followed by simulation results, discussion and comparison in Section 5. Finally, Section 6 concludes.

2. Obtaining Performance Indices for Optimization of 3-Phase Grid Connected CHB Converter

This section describes the design concept of the system and proposes a multi-objective optimization (MOO) method for the desired CHB converter by obtaining and evaluating performance indices associated with the design parameters of the system.

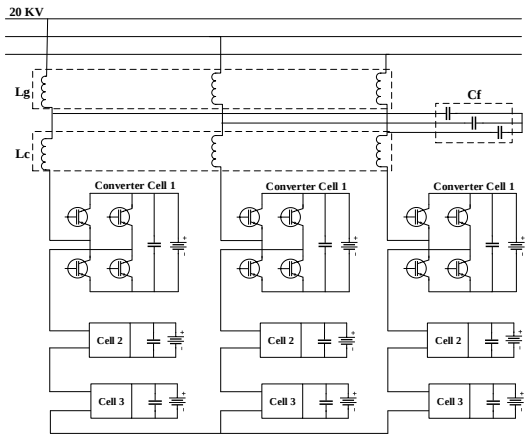

Fig. 1. The circuit configuration of the proposed 20kV transformerless BESS based on a multi-level cascaded PWM converter with an LCL filter.

2.1. Design concept of the 20 kV BESS

Fig. 1 represents a 20 kV BESS with an LCL filter. The system is based on cascading single-phase, H-Bridge PWM converter cells as described in [19]. 1 kHz is the selected PWM carrier frequency, but using a so-called "phase-shifted unipolar sinusoidal PWM" increases the equivalent carrier frequency.

For CHB converters, it is significant to note that the output voltage must have several levels to achieve the lowest losses and the highest efficiency. Therefore, to obtain the most optimal parameters of the system, especially the number of H-Bridge cells per phase, which consequently, specifies the number of output voltage levels, a multi-objective optimization process has been carried out (Section 3).

2.2. Optimization methodology

The MOO is a mathematical tool known from economics, which gives possibility to find family of solutions fulfilling the established requirements (objectives) in the best way. The MOO methods being very fast growing and developing areas of science, recently have been implemented in many engineering fields, where for solving complicated design problems with contrary design objectives are used. An area where MOO can be successfully implemented is power electronics. Thanks to increasing computational speed and further development of programming tools, there are many ways to solve multidimensional problems, and this is a very rapidly growing area of new computational methods and algorithms [20]. There is no single best solution for optimizing your system, but many different solutions and various trade-offs. The objective of the applied optimization technique is to generate a global optimum, also called the Pareto front, for a chosen criterion, such that any improvement in any objective worsens the other (in this case set of BESS parameters), shown in Fig. 2.

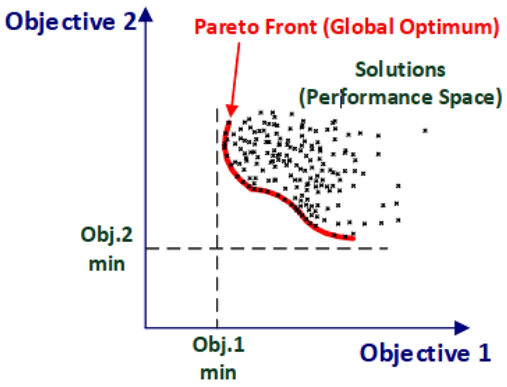

Fig. 2. Results of discrete optimization – Pareto front (global optimum).

The first classification of optimization techniques is based on some objective, which allows the techniques to be divided into single-objective and multi-objective approaches.

1) Single-goal optimization, also called scalar optimization, is a relatively simple approach whose goal is to minimize or maximize the cost function f(x) associated with one goal (criteria). Some additional constraints can be added in the form of ci constraints. The optimization problem can be formulated as Eq. (1).

$$\begin{aligned} &\min f(x) \\ &subject\ to\ g_i(x) = c_i\ \ for\ i = 1.\ ...\ .n \end{aligned} \tag{1}$$

2) Multi-objective optimization (also known as multi-objective programming, vector optimization, multi-criteria optimization, multi-attribute optimization, or Pareto optimization) is a problem involving optimization of multiple objectives, each of which is chosen and expressed by the performance. It is an index, written in terms of another cost function. This

means that we have to optimize multiple cost functions. The problem can be formulated as Eq. (2).

$$\begin{aligned} &\min(f_1(x).f_2(x).....f_n(x)) \\ &\text{subject } to\ x \in X \end{aligned} \tag{2}$$

Many cost functions create a multidimensional performance space, as shown in Fig. 3. The idea of MOO is to find the solution that best meets all set goals. This means that changing the optimal optimization parameters will not bring any benefit to the selected goal (it will not make other goals worse).

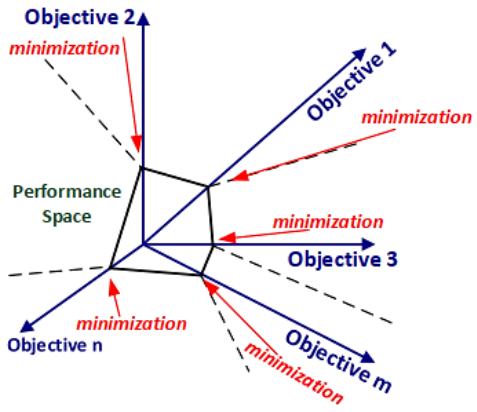

Fig. 3. A simplified representation of the multidimensional performance space created by multi-objective optimization.

2.3. Initial parameters

Primary factors specified by the designer used for the procedure.

- RMS values of grid voltage (U_{GRID}) and grid angular frequency (ω_0) – respectively for the designed system.
- Nominal power (P_N) – Based on this value and the RMS current (I_{RMS}) of the grid under nominal load, the value of the considered system's nominal power, expressed in Watts, is calculated.
- Boundary Conditions - Designer-specified range for variations in intermediate circuit voltage level (U_{DC}) and switching frequency (F_{SW}).

2.4. Line filter

The first step is to calculate the quality factor of the line filter according to the specified U_{DC} and F_{SW}. The line filter uses LCL topology. Fig. 4 shows the single-phase equivalent circuit of a VSC with an LCL filter.

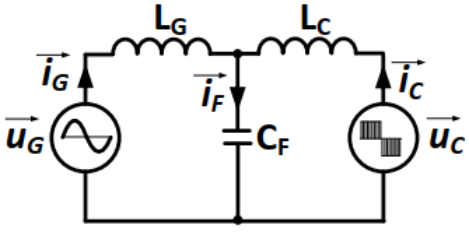

Fig. 4. Single-phase equivalent circuit of the VSC with LCL filter.

In [21] and [22] filter's most significant parameters have been calculated. The following key performance indicators are used to evaluate the constructed line filter.

- V_{LCL} – volume-related indices of filter components, estimated based on peak energies using the scaling factor described in [23]. For the analyzed LCL filter, is expressed as Eq. (3).

$$V_{LCL} = \tfrac{1}{2}.SF_C.C_F.U^2_{Grid} + \tfrac{1}{2}.SF_L.(L_C + L_G).I^2_{G\_MAX} \tag{3}$$

Where SF_C and SF_L are the capacitor and inductor scaling factors, respectively, I_{G_MAX} is the maximum LC current depending on the ripple current RippC, expressed as Eq. (4).

$$I_{G\_MAX} = I_{RMS} + (RippC.I_{RMS}) \tag{4}$$

The capacitance value of the filter is considered the first parameter that needs optimization. The scaling factor is related to the material and component technology chosen. It is 1.11 m3/kJ for the inductor and 0.54 m3/kJ for the capacitor in the analyzed case [23].

2.5. DC-link capacitor

The next step in the optimization process is to calculate the key performance indicators assigned to the DC-link capacitors of the converter. DC-link capacitors stabilize the voltage in DC circuits by supplying high currents, especially during transients. Capacitors in DC-link applications should have a sufficiently long service life, usually 20,000 hours (approximately three years) or more, preferably 100,000 hours (around 12 years) or more. The operation of DC-link capacitors usually takes place at high temperatures due to the proximity of the power semiconductor switches. The following key performance indicators are used to evaluate the type and value of the DC-link capacitor.

1) V_{C_DC} - An index associated with the volume of a DC-link capacitor based on peak energy, using a scaling factor linked to the type of materials and technology (SF_{DC}).

$$V_{C_{DC}} = \frac{1}{2}.SF_{DC}.C_{DC}.U^2_{DC} \tag{5}$$

2) PC_DC - Metric assigned to DC-link Capacitor Loss. Assuming (for simplicity) that the core temperature is equal to the case temperature, the power loss in the capacitor is given by Eq. (6).

$$P_{(C\_DC)} = I^2_{Ripp\_RMS}.ESR_{C\_DC} \tag{6}$$

I_{Ripp_RMS} is the ripple current of the capacitor, and ESR_{C_DC} is the equivalent series resistance of the capacitor as given in the manufacturer's datasheet; or formulated as Eq. (7).

$$ESR_{CDC} = \frac{\tan\delta}{2.\pi.f_{SW}.C_{DC}} \tag{7}$$

Where $\tan\delta$ – dissipation factor, F_{SW} – switching frequency, C_{DC} – DC-link capacitance.

2.6. Semiconductors

Semiconductor selection is a complex task involving many interrelated variables. There are many power semiconductors on the market with different characteristics and prices available to developers.
To evaluate and select accessible power semiconductors, it is necessary to calculate switching device losses. This criteria, provides information on required heat sink size, expected efficiency, and converter volume. The proposed design methodology; uses the following metrics:

- Loss factor (S_{LOSSES}) - factor related to losses in the switching section of the converter. Semiconductor losses; are calculated as the sum of switching (P_{SW}) and conduction losses (P_C) multiplied by the number of transistors (n_T) and diodes (n_D) used. It; is based on the standard formulas given in [24].

$$S_{Losses} = n_T.(P_{sw_T} + P_{C_T}) + n_D.(P_{sw_D} + P_{C_D}) \quad (8)$$

As a single switching device, IGBT, IGBT with reverse diode, MOSFET, or MOSFET with reverse diode are considered Eqs. (9) and (10), respectively.

$$P_{sw_T} = \frac{1}{\pi}.f_{SW}.(E_{SW}).\frac{I_M}{I_{RMS}}.\frac{U_{DC}}{U_N} \quad (9)$$

$$P_{sw_D} = \frac{1}{\pi}.f_{SW}.(E_{REC}).\frac{I_M}{I_{RMS}}.\frac{U_{DC}}{U_N} \quad (10)$$

Where, P_{SWT} is the switching loss of the transistor, P_{SWD} is the switching losses of the reverse diode, E_{SW} is the switching energy of the transistor (taken from the datasheet)', E_{REC} is the switching energy of the reverse diode (taken from the datasheet), at the test voltage U_N and the current I_N (datasheet parameters), U_{DC} is the converter DC-link voltage, I_M; peak current of the converter, F_{SW}; switching frequency. By; integrating these two relationships, the standard equation for the losses of a switch consisting of a transistor and a diode will be equal to the Eq. (11).

$$\begin{aligned} &P_{SW} = \tfrac{1}{\pi}.f_{SW}.(E_{SW} + E_{REC}).\tfrac{I_M}{I_{RMS}}.\tfrac{U_{DC}}{U_N} \\ &\text{where :} \\ &E_{SW} = E_{ON} + E_{OFF} \end{aligned} \quad (11)$$

- Conduction losses are calculated as transistor losses, optionally combined with diodes according to Eqs. (12) and (13).

$$P_{C_T} = U_{T0}.I_{T\_avg} + I^2_{T\_RMS}.\frac{R_{ON}}{n_{T1}} \quad (12)$$

$$P_{C_D} = U_{D0}.I_{D\_avg} + I^2_{D\_RMS}.\frac{R_D}{n_{D1}} \quad (13)$$

Where, P_{CT} is the conduction loss of the transistor, U_{T0} is the threshold voltage of the transistor, I_{T_avg} is the average current of the transistor, I_{T_RMS} is the rated current of the transistor, R_{on} is the on-resistance of the transistor (taken from the datasheet), n_{T1} is the transistor's number. P_{CD} is diode conduction loss, U_{D0} is the diode threshold voltage, I_{D_avg} is the diode average current, I_{D_RMS} is the diode rated current, r_D is diode forward resistance (taken from datasheet), n_{D1} is the number of diodes, which by simplifying, and summarizing the above relations for the total conduction loss of the semiconductor, it will be according to the Eq. (14).

$$P_{CON} = 2 * I^2_{RMS} * r_{ON} \quad (14)$$

For a proper and optimal design and optimization of 20-kV BESS, four different power switches (IGBTs) have been analyzed according to the described methodology. The specification of these four switches is observed in Table 1.

The obtained results for U_{DC} = 5.55 kV in the frequency range of 0-2 KHz are presented in Fig. 5.

According to the lowest overall loss, IGBT number one (5SNA 0600G650100) has been selected for optimization.

Table 1. Technical specifications of power switches (taken from datasheet).

Specification	IGBT 1	IGBT 2	IGBT 3	IGBT 4
Module's Name	5SNA 0600G650100	FD250R65KE3-K	CM1000HG-130XA	FZ400R65KE3
Voltage (V_{CE})	6500 V	6500 V	6500 V	6500 V
Current (I_C)	600 A	250 A	1000 A	400 A
Forward Voltage	3.2 V	3 V	2.4 V	3 V
E_{on}	3800 mJ	1400 mJ	7850 mJ	2250 mJ
E_{off}	1950 mJ	1200 mJ	6700 mJ	2000 mJ
E_{rec}	1100 mJ	470 mJ	4450 mJ	740 mJ
R_{on}	0.0053 Ω	0.012 Ω	0.0024 Ω	0.0075 Ω

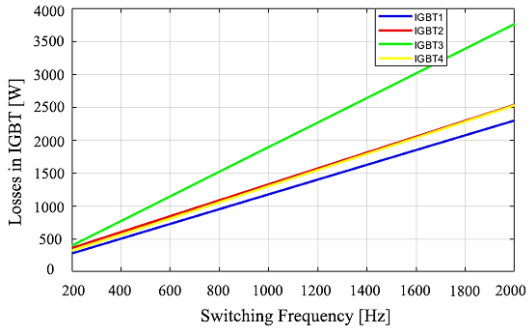

Fig. 5. P_{SEM} performance index for analyzed power IGBTs in switching frequency range 0-2 kHz.

3. Optimization Results

In this section, the results of the multi-objective optimization algorithm based on the Pareto front method presented, which is shown in Fig. 6. The objective functions and parameters have previously been described. The values of optimized parameters are shown in Table 2.

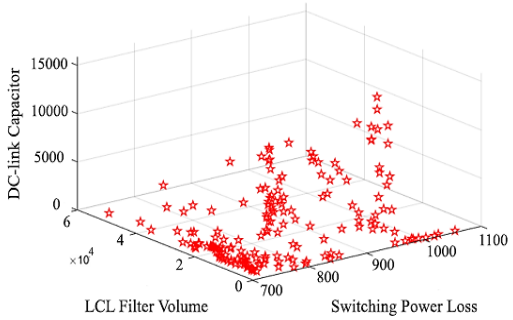

Fig. 6. The result of multi-objective Pareto front optimization for three considered objective functions.

This group of answers obtained from the optimization can be used in the optimal design and development of a medium voltage and high power battery energy storage system based on a CHB

Table 2. The final values of parameters optimized by a multi-objective genetic algorithm.

Number of H-Bridge cells per phase	LCL Filter capacitance (F)	DC-link capacitance (F)
6.8879	1.6935e-06	1.5301e-04
3.3179	4.5925e-04	1.0000e-06
3.7520	1.7512e-04	1.0000e-06
5.7421	1.2435e-06	1.6754e-04
6.8618	4.2275e-04	1.0025e-06
6.3981	5.3908e-05	1.0002e-06
4.9711	1.1814e-06	4.6924e-05
4.7815	1.5157e-04	1.0000e-06
4.6921	4.6282e-05	1.0000e-06
6.1498	5.8507e-06	3.2146e-05
5.6546	9.3007e-05	1.0000e-06
3.8426	1.4288e-05	2.2670e-06
5.4188	5.9662e-04	1.0000e-06
6.9013	2.9870e-04	1.2419e-06
5.3965	1.7895e-04	1.0000e-06
6.8121	1.4454e-05	3.9758e-04

multi-level converter.

The vital point taken from Fig. 6 is that those dots and solutions that are placed together and concentrated in the lower parts of the three-dimensional diagram are more optimal solutions compared to the points scattered in the upper parts of the graph. As explained in the previous sections, the way the multi-objective optimization algorithm works is based on the optimization and improvement of each variable without leaving the other variables out of their optimal range. In other words, each objective function is considered as a constraint for different objective functions, and thus, all parameters are optimized together. But, as seen in Table 2, the few solutions scattered in the corners of the graph simply are one of the optimized objective functions, and the other two are not in their optimal range. Therefore; they are not used as answers for the system. Of all available optimal answers, N=3 is chosen as the number of H-Bridge cells per phase because of the price or the system's overall cost. According to Eq. (15) which is the cost function of the system, by adding the number of cells per phase the overall cost of the system will significantly increase.

$$\gamma = \sum_{i=1} nC_i + \beta \tag{15}$$

Where: n is the number of H-Bridge cells per phase, C_i is the cost of each switch, and β is other system costs excluding switches.

Consequently, considering all criteria and conditions, N=3 is the best and most optimal solution for this system, and the Control strategy has been implemented based on this number.

4. System Control Strategy

SOC compensation control and active power control are two main parts of the entire control system. Also, as shown in Fig. 7, SOC balance control consists of battery unit SOC balance control and interphase SOC balance control, and this entire figure will be described in detail in subsections A and B.

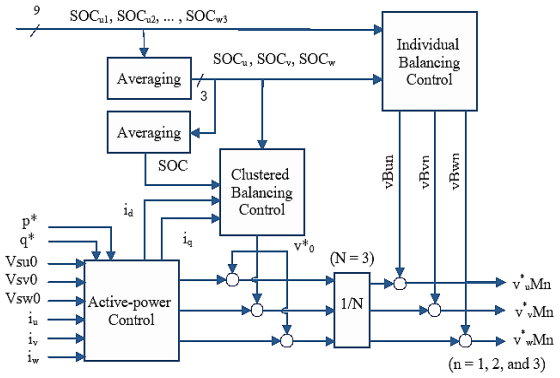

Fig. 7. Control block diagram for the 20 KV system with a cascade number of N = 3.

4.1. Active power control

Fig. 8 illustrates the block diagram of the active power control, developed on the decoupled current control scheme concept [25]. Let us define the supply voltage from the three-phase line to neutral as Eq. (16).

$$\begin{bmatrix} V_{SuO} \\ V_{SvO} \\ V_{SwO} \end{bmatrix} = \sqrt{\frac{2}{3}} V_S \begin{bmatrix} \sin\omega t \\ \sin(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{16}$$

The d-axis current set points are obtained from the instantaneous active power set point p*. Similarly, the current set points of the

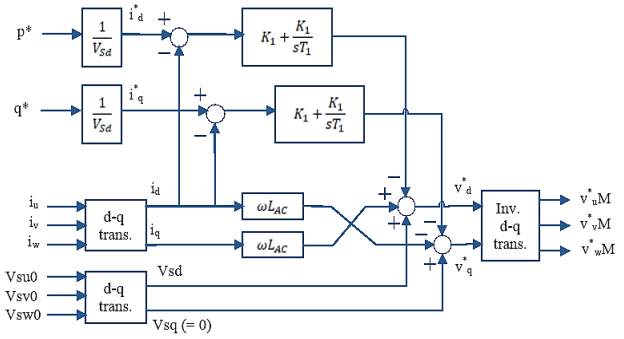

Fig. 8. Active-power control based on the decoupled current control.

q-axis are determined from the instantaneous reactive power set point q*.

$$i_d^* = \frac{p^*}{V_{sd}} \tag{17}$$

$$i_q^* = \frac{q^*}{V_{sq}} = 0 \tag{18}$$

Where v_{Sd} and v_{Sq} are the d-axis and q-axis components of v_S.

The d-axis and q-axis AC voltage commands are calculated as follows:

$$\begin{bmatrix} V_d^* \\ V_q^* \end{bmatrix} = \begin{bmatrix} V_{sd} \\ 0 \end{bmatrix} - \begin{bmatrix} 0 & -\omega L_{AC} \\ \omega L_{AC} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} - K_1 \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} - \frac{k_1}{T_1} \int \begin{bmatrix} i_d^* - i_d \\ i_q^* - i_q \end{bmatrix} dt \tag{19}$$

Where i_d and i_q are the d-axis and q-axis components of i. The first and second terms on the right side of Eq. (19) eliminate the effects of the supply voltage and the steady-state voltage appearing across the AC inductor L_{AC}. The third, and fourth terms form a proportional-integral (PI) controller with a proportional gain K_1 and an integral time constant T_1. The three-phase reference signals v_{uM*}, v_{vM*}, and v_{wM*} are obtained by applying the inverse d-q transform Eq. (19).

Referring to [26], the critical damping response is obtained with the following gain Eq. (20):

$$K_1 = \frac{4L_{AC}}{T_1} = 0.5\frac{V}{A} \; at \; T_1 = 10ms \tag{20}$$

4.2. Phase-group SOC-balancing control

Fig. 9 shows the block diagram of cluster SOC balancing control based on zero-sequence voltage injection. The idea is to add a zero sequence zero frequency voltage V_0 to the three-phase ac voltages V_{uM}, V_{vM}, and V_{wM} of the cascaded converter.

This allows each cluster (phase) to draw or release an unequal active power without pulling a negative sequence current. Since; the zero-sequence voltage injection causes no change in the line-to-line voltages, the cluster balancing control does not affect the three-phase line currents and the total power. Assuming the cascade converter voltage does not contain negative voltage, it would be expressed as Eq. (21).

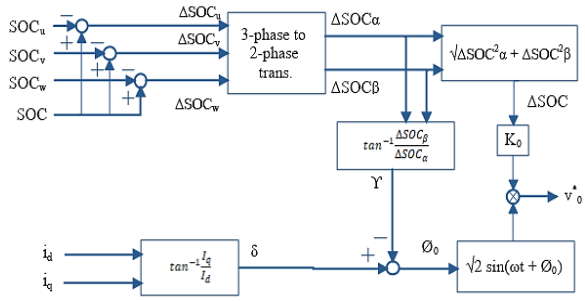

Fig. 9. The diagram of phase-group SOC-balancing control between three phases.

$$\begin{bmatrix} V_{uM}^{\cdot} \\ V_{vM}^{\cdot} \\ V_{wM}^{\cdot} \end{bmatrix} = \begin{bmatrix} V_{fuM}^{\cdot} \\ V_{fvM}^{\cdot} \\ V_{fwM}^{\cdot} \end{bmatrix} + \begin{bmatrix} V_0^{\cdot} \\ V_0^{\cdot} \\ V_0^{\cdot} \end{bmatrix} = V_{fM} e^{j\phi f} \begin{bmatrix} 1 \\ e^{-j\frac{2\pi}{3}} \\ e^{j\frac{2\pi}{3}} \end{bmatrix} + V_0 e^{j\phi 0} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{21}$$

The first term on the right side of the equation indicates the positive sequence voltage with the value $V_{fM\ rms}$ and the phase angle ϕ_f concerning the phase voltage u. The second expression represents the zero sequence voltage of the fundamental frequency with the value of $V_0\ rms$ and the phase angle ϕ_0. Both V_0 and ϕ_0 can be adjusted with cluster balancing control.

In this part of the design process of the converter control system, we will calculate the zero sequence voltage equation, which plays a vital role in balancing the charging state of the batteries. Let Δ_{SOCu} be the difference between the average value of SOC of nine battery units in three phases and the average value of SOC of three battery units in the U phase.

$$\Delta SOC_u = SOC - SOC_u \tag{22}$$

$$SOC = \frac{1}{3}\left(SOC_u + SOC_v + SOC_w\right) \tag{23}$$

$$SOC_u = \frac{1}{3}\left(SOC_{u1} + SOC_{u2} + SOC_{u3}\right) \tag{24}$$

The difference between Δ_{SOCv} and Δ_{SOCw} can also be expressed in the same way as Eq. (25).

$$\begin{bmatrix} \Delta SOC_u \\ \Delta SOC_v \\ \Delta SOC_w \end{bmatrix} = \begin{bmatrix} SOC - SOC_u \\ SOC - SOC_v \\ SOC - SOC_w \end{bmatrix} \tag{25}$$

These differences are associated with the amount of active power that should be either absorbed or injected by each of the three phases of the utility grid to maintain SOC balance among the clusters. By converting three-phase to two-phase, the Eq. (26) is achieved.

$$\begin{bmatrix} \Delta SOC_\alpha \\ \Delta SOC_\beta \\ \Delta SOC_0 \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{3}{2}} SOC_u \\ \frac{1}{\sqrt{2}}\left(\Delta SOC_v - \Delta SOC_w\right) \\ 0 \end{bmatrix} \tag{26}$$

ΔSOC and γ calculated according to relations Eqs. (27) and (28), respectively.

$$\begin{aligned} \Delta SOC &= \sqrt{\Delta SOC_\alpha^2 + \Delta SOC_\beta^2} \\ \Delta SOC &= \sqrt{\Delta SOC_u^2 + \Delta SOC_v^2 + \Delta SOC_w^2} \end{aligned} \tag{27}$$

$$\gamma = \begin{cases} \tan^{-1}\frac{\Delta SOC_\beta}{\Delta SOC_\alpha} & if\ \Delta SOC_\alpha \neq 0 \\ \frac{\pi}{2}\ if\ \Delta SOC_\alpha = 0\ and\ \Delta SOC_\beta > 0 \\ -\frac{\pi}{2}\ if\ \Delta SOC_\alpha = 0\ and\ \Delta SOC_\beta < 0 \end{cases} \tag{28}$$

Here, ΔSOC is a parameter that indicates the degree of SOC imbalance among the three phases. In comparison, γ is a parameter related to the SOC imbalance distribution among the three phases in terms of phase angle on the α - β axes.

The reference zero-sequence voltage is determined according to Eq. (29).

$$V_0^* = \sqrt{2}.K_0.\Delta SOC.\sin(wt + \varphi_0) \tag{29}$$

K_0 is a proportional gain, and ϕ_0 is calculated by Eq. (30).

$$\varphi_0 = \delta - \gamma \tag{30}$$

4.3. Battery unit SOC-balancing control

Fig. 10 shows a SOC-balancing control diagram of a battery pack of converter cells in each phase. The SOC difference between battery units in each phase is given by Eq. (31). Thus, SOC-balancing control of the battery packs can be achieved by adding the AC output voltages to the corresponding base voltages of each battery pack, as shown in Fig. 10 [26], [27].

$$\begin{aligned} &\Delta SOC_{xn} = SOC_x - SOC_{xn} * x = u * v * w \\ &and\ n = 1.2.3 \end{aligned} \tag{31}$$

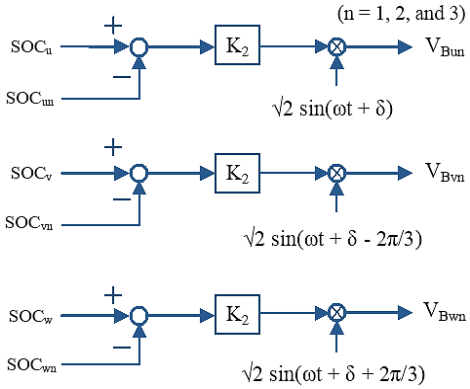

Fig. 10. Battery unit SOC-balancing control diagram of converter cells.

where SOC_x is the average value of each phase, SOC_{xn} is the value of the nth-converter cell in each phase, and K_2 is the proportional gain as in [27].

5. Simulation Results, Discussion and Comparison

This paper uses MATLAB software to verify the optimized system and analyze the output results of the medium voltage and high-power battery energy storage system simulation. The power level has been set equal to 8 MW. The specifications and general parameters of this system are summarized in Table 3.

According to the multi-objective optimization results, N = 3 has been chosen as the cascade number of H-bridge cells per phase. For cascade number N=3, the cascaded line to neutral and line-to-line AC voltage will be a 7-level waveform and a 13-level waveform, respectively.

Table 3. The parameters of the designed BESS with the voltage of 20 kV and power of 8 MW.

Parameter	Symbol	Value
Nominal line-to-line rms voltage	V_s	20 kv
Power rating	P	8 MW
Cascade number	N	3
Filter capacitor	C_{LCL}	20 uF
AC inductor	L_{AC}	80.1 mH
DC-link capacitor	C_{dc}	60 uF
Lithium-ion battery unit	$V_{(Batt,Pack)}$	6500 V
PWM carrier frequency	f_{sw}	1 kHz
Equivalent carrier frequency	$f_{(car,eqiu)}$	6 kHz

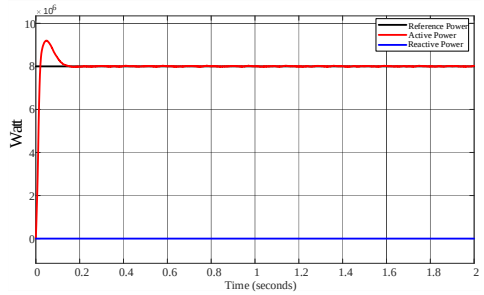

Fig. 11. Output active and reactive power of battery energy storage system P=8 MW.

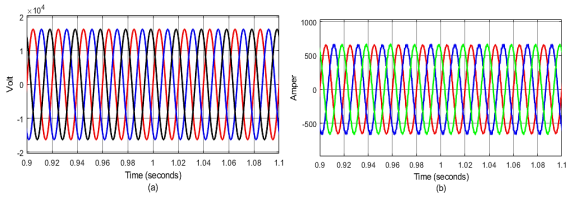

Fig. 12. Output waveforms of the system in charging mode. a) Three-phase voltage, b) Three-phase current.

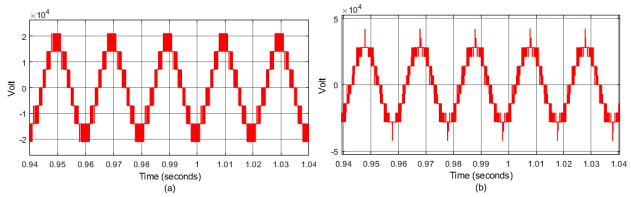

Fig. 13. Multi-level voltage waveforms produced by the converter. a) Phase-to-neutral voltage, b) Line-to-line voltage.

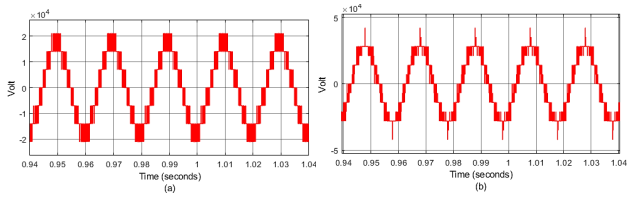

Fig. 14. Average SOC value of all batteries in three phases during charging mode. a) Phase A SOC, b) Phase B SOC, c) Phase C SOC, d) Zero-sequence voltage.

5.1. Charging waveforms

Fig. 11 shows the output active and reactive power of the battery energy storage system. The active power is set to 8 MV, and the reactive power is set to zero to reach the unity power factor.

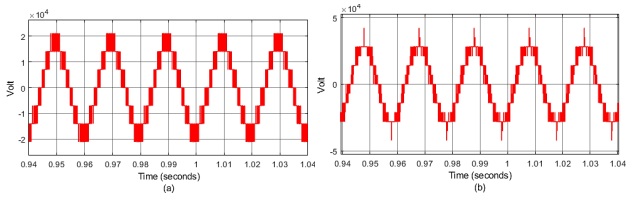

Fig. 15. Comparison of output active power of the battery energy storage system and reference power in transient mode.

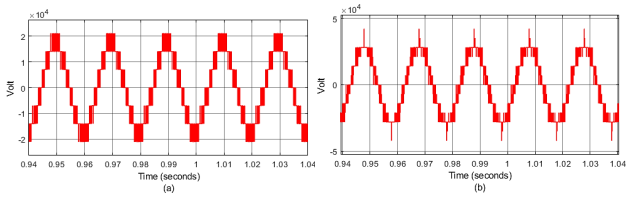

Fig. 16. The simulation of the d-q voltage and current waveforms during the transient mode. a) d-axis and q-axis voltages, b) d-axis and q-axis currents.

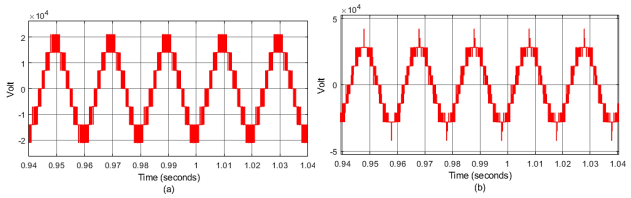

Fig. 17. Average SOC value of all batteries in three phases in transient state.

Moreover, the speed of the output power control is illustrated.

The three-phase voltage and current of BESS are shown in Fig. 12-(a) and Fig. 12-(b) respectively. In this mode which is charging mode, the control system injects the required current into the utility grid to compensate for the power factor.

According to the optimization results, the optimal number of H-bridge cells per phase was chosen as 3. Therefore; the expected number of the converter's output voltage is 7, shown in Fig. 13-(a). Consequently, the line-to-line voltage is 13 levels as shown in Fig. 13-(b).

By injecting the zero sequence voltage shown in Fig. 14-(d), control and balancing the charging status of batteries in all three phases, A, B, and C, is carried out, which can be seen in Fig. 14. This indicates that the control strategy designed for this system is properly performing.

5.2. Transient state waveforms

In this part, the simulation waveforms of the transient state mod are presented. In this mode, the reference active power is set to zero until 0.5 seconds, but after that, the BESS is connected to the utility grid, and the reference power changes to 8 MW.

Fig. 15 shows the changes in the output power of the battery energy storage system according to the given reference power. At, t = 0.5 S, the power has increased from zero to 8 MW, indicating that the control system is working correctly.

Figs. 16-(a) and 16-(b) illustrate the voltage and currents of the d and q axes, respectively, which are calculated using the d-q conversion of three-phase voltage and current values of the system.

The average SOC balancing control of all battery packs is shown in Fig. 17-(a). Fig. 17-(b) shows SOC differences between the three phases when the battery is in charging operation mode.

Table 4. Comparison of selected parameters of this research with recently published papers.

Criteria \ References	Ref. [18] (A constrained inter submodule, 2022)	Ref. [19] (A constrained inter submodule, 2022)	Ref. [2] (Control of multilevel CHB converter, 2021)	Proposed method	Improvement rate (%)
DC-link capacitor	5 mF			60 uF	98.8%
LCL filter inductor		7.5 mH		1 mH	86.6%
LCL filter capacitor			47 uF	20 uF	57.4%

5.3. Comparison

This section of the paper presents a numerical comparison between the results of this research and the works done by other researchers. Battery energy storage is a broad system with many significant factors contributing to its performance. To make this comparison, several vital elements of the optimized system, such as the value of the DC-link capacitor, LCL filter capacitor, and inductor have been selected. In Table 4 the same parameters of other recently published papers were compared.

This comparison indicates that the innovative idea of this research, which is implementing a powerful and comprehensive multi-objective optimization algorithm was successfully validated. As Table 4 shows the proposed design procedure gains a reduction of the size and volume of considered capacitors, decreases the system's total cost and improvement of system efficiency (overall loss reduction).

6. CONCLUSION

This paper has presented the optimum development of a 20-KV and 8-MV battery energy storage system based on a cascaded H-bridge converter connecting to a medium-voltage and high-power utility grid. The focus is on optimizing the most crucial system parameters, including the LCL filter, DC-link capacitance, and semiconductors, to achieve the lowest power switch loss and high-efficiency performance under different modes. It should be noted that the proposed method has been able to successfully reduce the size and volume of the LCL filter and DC-link capacitor by 57.4 and 98.8% respectively, which is a significant achievement. In addition, an innovative method based on an optimization algorithm was proposed to determine the best and most appropriate power switch (IGBT) for this system. The simulation of this system has been carried out in MATLAB/SIMULINK to verify the performance of control components. According to the optimization results, the number of H-bridge cells per phase has been chosen as 3, which is the most optimal number of converter submodules. Eventually, the waveforms of the system's primary parameters, such as active and reactive power in both charging and discharging modes, indicate that the BESS has an outstanding performance.

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