Journal of Operation and Automation in Power Engineering

Vol. XX, No. XX, Dec. 2022, Pages: XXXX (Proofed)

http://joape.uma.ac.ir

Research Paper

Innovative Z-Source High Gain Step-up DC-DC Converter Integrated with Built-in Transformer

Taha Irani[1] , *Saeed Hasanzadeh*[1] * , and *Seyed Mohsen Salehi*[2]

[1]*Department of Electrical and Computer Engineering, Qom University of Technology, Qom, Iran.*
[2]*Department of Electrical and Computer Engineering, Tarbiat Modares University, Tehran, Iran.*

Abstract— *The increasing deployment of photovoltaic (PV) panels has raised the need for efficient voltage-boosting solutions to overcome low output voltages. Conventional DC-DC boost converters face high conduction losses and voltage stress on components. This paper proposes a new topology for a Z-source converter that integrates the switched inductor technique by using Built-in-Transformer. Various voltage-boosting methods have been explored. However, existing solutions suffer from limitations in voltage gain, voltage stresses, duty cycle range, and the number of components. The proposed topology combines the advantages of the Z-Source converter, switched capacitor technique, and switched inductor technique, to address these limitations. The paper presents the circuit configuration, operating modes, steady-state analysis, design considerations, efficiency analysis, small signal analysis, and simulation of the proposed converter. The new topology significantly improves active component count, device voltage stress, and voltage gain control, making it a promising solution for efficient voltage boosting in PV applications. Finally, to validate the performance of the proposed converter, a 150W prototype is presented.*

Keywords—DC-DC converters, photovoltaic panels, small signal analysis, switched capacitor technique, switched inductor technique, Voltage multiplier cell, Z-source converter.

1. INTRODUCTION

In recent years, there has been a notable rise in the use of photovoltaic (PV) panels. One of the main challenges faced in PV generation is the low voltage output of these panels. Traditionally, connecting PV panels in series has been the go-to solution for increasing voltage levels. However, this approach has significant drawbacks such as susceptibility to shading losses, mismatch losses from panel variances, lack of flexibility, single point failure risk, challenging wiring, limited panel-level monitoring, and inability to maximize performance for each individual panel. In such scenarios, opting for a parallel-connected arrangement of PV panels is more effective than a series-connected setup [1]. Nevertheless, PV panels still suffer from relatively low output voltage. As a result, it becomes necessary to employ high-gain DC-DC converters that can increase the voltage of these panels to the grid level. Primary DC-DC boost converters can achieve this goal but must operate in high duty cycle values. Although high duty cycle operation of boost converters is necessary for reaching high voltage step-up ratios, it causes problems like lower efficiency, thermal issues, ripple, control difficulties, and electromagnetic interference. Mitigating these effects adds complexity through requirements for more extensive heat sinking, input filtering, compensation network design, switch selection for minimal transition times, potential derating, and output ripple management. The main parameters of a converter in PV applications are a low current ripple in input, low power losses, high gain, and a minimum number of components and costs.

Voltage multiplying methods in boost DC-DC converters are categorized into three main structures: ladder networks, switched capacitor configurations, and switched inductor configurations. While ladder networks provide basic voltage multiplication, their lack of efficiency, dynamic response, and controllability motivate to developing more advanced converter topologies and control strategies [2]. Previous studies [3] applied the switched capacitor method to converters; however, these converters suffered from drawbacks such as high spike of electric current in capacitors and more resistance losses. On the other hand, the converter proposed in [4] adopted the switched inductor method to achieve high gain. In [5, 6], the gain exhibited a quadratic relationship with the duty cycle, resulting in a significant gain. The coupled inductor was combined with the quadratic method in [7, 8]. By incorporation of coupled inductors or transformers, these converters offer two degrees of freedom to tune gain: the duty cycle and the turn ratio. As a result, it allowed more flexibility in designing these types of converters.

The Z-source (ZS) converter, first proposed in 2002 [9], provides a unique impedance network. This converter provides a versatile single-stage buck-boost topology with added benefits of reliability, efficiency, and simplicity compared to traditional converter designs [10]. Also, a variation of this method, called the quasi-ZS, retain the core functionality and advantages while easing implementation [11]. Integrated switched inductor cells with the conventional ZS network, introducing a new switched inductor ZS impedance network [12]. A new ZS converter was proposed in [13], where the position of the output capacitor and diode is different. This

Received: 03 Sep. 2023
Revised: 05 Mar. 2024
Accepted: 18 Jun. 2024
*Corresponding author:
E-mail: hasanzadeh@qut.ac.ir (S. Hasanzadeh)
DOI: 10.22098/joape.2024.13629.2043

converter has higher voltage gains and common ground for the input and output.

In [14], a novel category of ZS and quasi-ZS converters was proposed. These converters were designed to have a four-quadrant operation and bipolar output, reducing component requirements. However, it was noted that the voltage gain needed to be increased for optimal performance. Inspiring this research, another study combined the switched capacitor and the quasi-ZS converter to develop an enhanced version with higher gain and improved capacitor voltage stress [15]. Although the voltage gain of this converter still fell short of expectations, it did offer the advantage of having a common ground. Another quasi-ZS converter combined with the switched capacitor method was suggested in [16], presenting high gain, but with drawbacks like high voltage stresses on the switched capacitors. In [17], the voltage lift method was applied to the quasi-ZS converter to raise the voltage gain. But in this converter, the voltage stress of semiconductor components is high. In [18], a hybrid switched capacitor-switched inductor approach is employed to propose a high gain converter, but with too many devices. [19] suggested a high gain converter by combining two switched capacitor cells to the quasi-ZS method. However, this approach resulted in many passive components, high voltage stress, and a duty cycle range of less than 0.25. in [20], a ZS converter integrated with a coupled inductor topology resulted in a significant gain with a lower duty cycle, but a duty cycle range is limited to 50%. Also, it includes too many active and passive components and complicated circuits.

Integrating the switched capacitor technique into the conventional ZS network has led to the development of a novel switched capacitor-based ZS network, as proposed in [21]. In this network, there are notable differences in how the output diode and output capacitor are connected when compared to traditional ZS converters. These modifications result in a significant increase in voltage gain and a reduction in voltage stresses on semiconductor devices. Moreover, all capacitors within the ZS network and switched capacitor cells experience equal and low voltage stresses. Another advantage is that these converters do not face any limitations on the duty cycle. Ref. [22] introduced three new Z-source converters with integrated switched capacitor cells, which provide a straightforward topology with high voltage gain and smooth input current ripple. However, while the gain is adequately high, these converters suffer from high voltage stress on the semiconductor devices. Motivated by the works in [22], this paper presents a novel Z-source converter topology that integrates the switched inductor technique using two windings' transformers. The key innovation in this work is the replacement of the two coupled inductors used in [22] with integrated transformer windings, allowing for a built-in transformer configuration. Compared to [22] and other mentioned converters, this modification, along with changes in the arrangement of diodes and capacitors, offers several notable advantages.

Firstly, it reduces the number of active components required. Secondly, it mitigates the voltage stresses experienced by the semiconductor devices. Thirdly, it provides a reasonable improvement in the voltage gain of the converter. Moreover, the built-in transformer topology offers two degrees of freedom for tuning the voltage gain: adjusting the turn ratio of the transformer windings and varying the duty cycle of operation. This flexibility in gain control is a significant benefit of the proposed approach. The main contributions of the paper are as follows:

- Combining the advantages of the Z-source converter, switched capacitor technique, and switched inductor technique to address limitations in voltage gain, voltage stresses, duty cycle range, and component count faced by existing solutions.
- Efficiency analysis highlighting the low conduction losses and identifying the switch loss as the dominant factor.
- Small-signal modeling and analysis proving the stability robustness of the converter, with a high 45-degree phase margin and stable pole-zero locations.
- Extensive simulations validating the theoretical analysis and design considerations over a wide operating range and experimental verification with a 150W prototype demonstrating the high gain, high efficiency, and flexibility advantages of the proposed topology.

The paper is structured as follows: Section 2 outlines the proposed converter's circuit configuration and operating modes, including the steady-state analysis. Section 3 discusses the primary design considerations. Efficiency analysis is provided in Section 4, followed by small signal analysis and results in Section 5. Section 6 presents the simulation results and an experimental prototype of the proposed converter investigated in Section 7. Finally, Section 8 concludes the paper.

2. TOPOLOGY AND OPERATION PRINCIPLE OF THE PROPOSED CONVERTER

2.1. Topology of the proposed converter

The proposed DC-DC converter is built of an input inductor (L_{in}), an input capacitor (C_{in}), an input diode (D_{in}), a combined network and an output capacitor (C_3). The network comprises of two symmetrical transformers and diodes (D_1, D_2) and two capacitors (C_1, C_2). Fig. 1 shows the circuit diagram of the proposed converter. Also, the key waveform of the proposed converter is shown in Fig. 2.

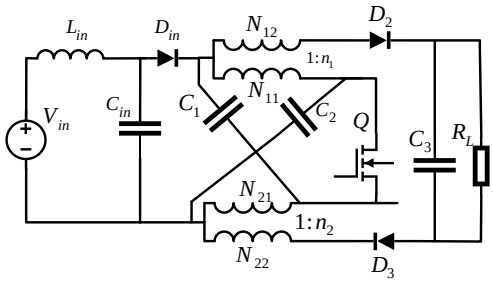

Fig. 1. Diagram of the proposed converter.

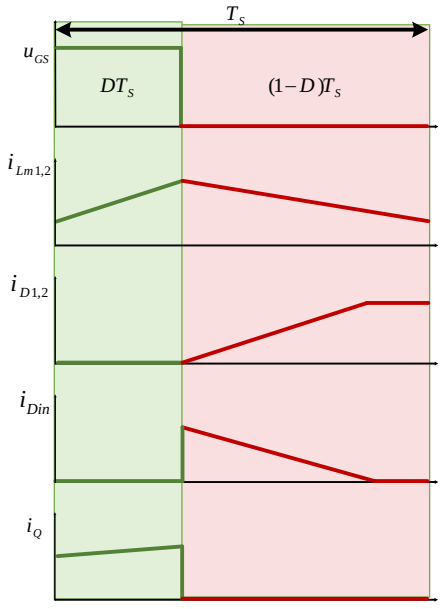

Fig. 2. Key waveforms of the proposed converter.

2.2. Operating principles of converter

The following assumptions have been taken into account for the analysis of the proposed converter: the converter is operating under steady-state conditions, the capacitors are sufficiently large to maintain constant voltages, all components in the study are assumed to be ideal, with no non-ideal parasitic parameters, and there is no consideration given to switching transients. The input filter (with L_{in} and C_{in}) is designed so the voltage of C_{in} equals the input voltage V_{in}, and the average current through L_{in} is the input current I_{in}. When switch Q is on, the converter is in the On-state, and when Q is off, it is in the off-state.

In the switching On-state ($0 < t < DT$), the Q switch is in conducting mode, and all diodes are off. Fig. 3-(a) shows this state's equivalent circuit.

$$V_{Lin} = V_{in} - V_{Cin} \tag{1}$$

$$V_{N11} = V_{C1} \tag{2}$$

$$V_{N21} = V_{C2} \tag{3}$$

$$V_o = V_{C3} \tag{4}$$

Conversely, in off-state ($0 < t < DT$), the Q switch is off mode, and diodes are conducting. Fig. 3-(b) shows an equivalent circuit. The equations can be written as follows:

$$V_{Lin} = V_{in} - V_{Cin} \tag{5}$$

$$V_{N11} = V_{in} - V_{C2} \tag{6}$$

$$V_{N21} = V_{in} - V_{C1} \tag{7}$$

$$V_{N12} = n_1 V_{N11} \tag{8}$$

$$V_{N22} = n_2 V_{N21} \tag{9}$$

2.3. Voltage gain and stress on components

Considering Eqs. (1)- (7). By applying voltage second balance for L_{in} and L_{m1} and L_{m2} in CCM, we can calculate voltage stress across capacitors:

$$d\left(V_{in} - V_{Cin}\right) + (1-d)\left(V_{in} - V_{Cin}\right) = 0 \tag{10}$$

$$\overset{yields}{\rightarrow} V_{in} = V_{Cin} V_{in} = V_{Cin}$$

$$\begin{cases} dV_{C1} + (1-d)\left(V_{Cin} - V_{C2}\right) = 0 \\ dV_{C2} + (1-d)\left(V_{Cin} - V_{C1}\right) = 0 \end{cases} \overset{yields}{\rightarrow} \begin{cases} V_{C1} = V_{in}\frac{d-1}{2d-1} \\ V_{C2} = V_{in}\frac{d-1}{2d-1} \end{cases} \tag{11}$$

And by Eqs. (8) and (9), we can consider that:

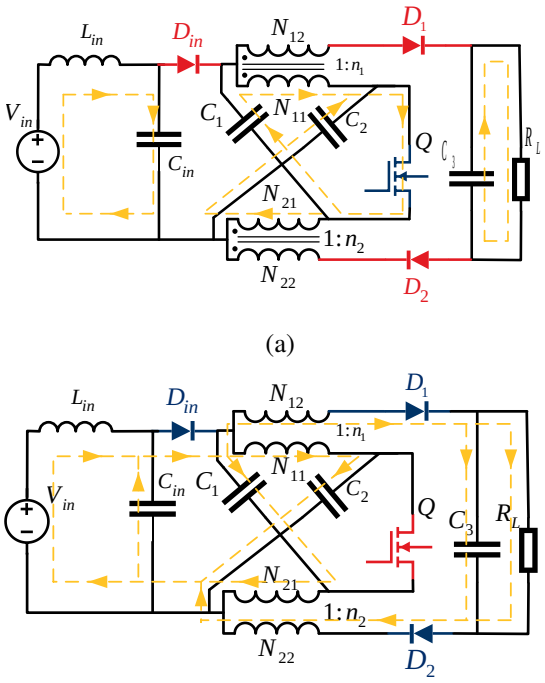

Fig. 3. Equivalent circuit of the proposed converter in (a) On-state and (b) Off-state.

$$V_{N12} + V_{N22} = (n_1 + n_2)\, V_{N11} = V_{in} - V_o \tag{12}$$

So,

$$V_o = V_{in} * \left(1 - (n_1 + n_2)\left(\frac{d}{2d-1}\right)\right) = V_{C3} \tag{13}$$

Voltage gain in Continuous Conduction Mode (CCM) can be calculated as follows:

$$M_{CCM} = 1 - (n_1 + n_2)\left(\frac{d}{2d-1}\right) \tag{14}$$

where $0 < d < 0.5$.

Fig. 4 shows voltage gain for different Duty-Cycle and turn ratio values. Notice that this figure represents the gain value on a logarithmic scale. In Fig. 5, we can see the gain versus duty cycle for three different values of turn ratio. Reverse voltage stress on diodes and voltage stress on semiconductor switches can be deduced as follows:

$$V_{Din} = V_{C1} + V_{C2} - V_{Cin} = V_{in}\frac{1}{2d-1} \tag{15}$$

$$V_{D1} = V_{D2} = \frac{V_{C3} + V_{N22} - V_{C2} - V_{C1} + V_{N12}}{2} = \frac{0.5}{1-2d} + \frac{(n1+n2)d}{1-2d} \tag{16}$$

$$V_Q = V_{C1} + V_{C2} - V_{Cin} = V_{in}\frac{1}{1-2d} \tag{17}$$

Fig. 6 and Fig. 7 show voltage stress on D_2 and D_3 diodes and Q switch, respectively. Unlike diodes, active switch voltage is independent of the transformers' turn ratio. A comparison of the main components' voltage stress for this circuit and [22] is included in Table 1.

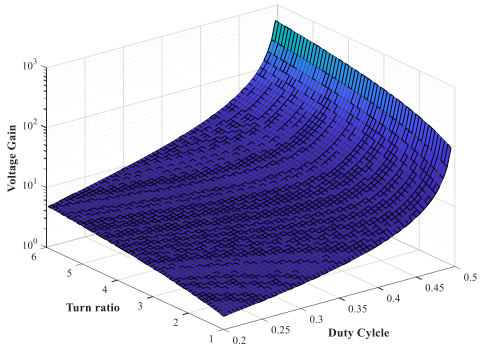

Fig. 4. Logarithmic voltage gain of converter for $1 < (n_1 + n_2) < 6$ and $0.2 < \mathrm{d} < 0.5$.

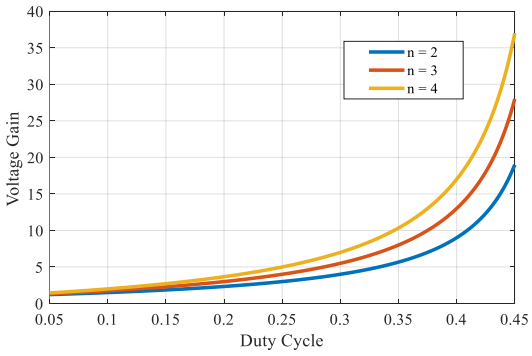

Fig. 5. Voltage gain for different values of duty cycle.

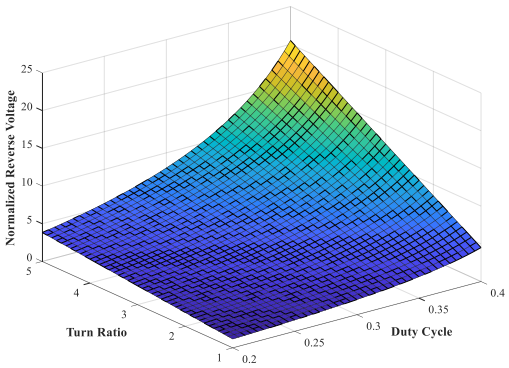

Fig. 6. Voltage stress on output diodes for $1 < (n_1 + n_2) < 5$ and $0.2 < d < 0.4$.

2.4. Current stress of the components

To assess the current stress on the components in this circuit, we assume that the current travels from the positive terminal to the negative terminal of each component, except for the input current. By utilizing Kirchhoff's Current Law (KCL) on the equivalent circuits of our proposed converter, we can derive a set of current relationships as follows:

$$I_{Cin}^{on} = I_{in} \tag{18}$$

$$I_{C1}^{On} = -I_{Lm1} \tag{19}$$

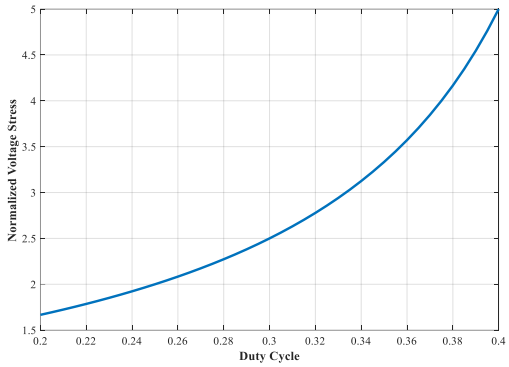

Fig. 7. Voltage stress on switch for $1 < (n_1 + n_2) < 5$ and $0.2 < d < 0.4$.

Table 1. Compare voltages stress and gain in the proposed converter and [22] ($n_1 = n_2 = n$).

Component	Parameter	Proposed	[22]
Inductor	V_{Lm1}^{On}	$-\frac{1-d}{1-2d}V_{in}$	$-\frac{1-d}{1-2d}V_{in}$
	V_{Lm1}^{Off}	$\frac{d}{1-2d}V_{in}$	$\frac{d}{1-2d}V_{in}$
	V_{Lm2}^{On}	$\frac{d-1}{1-2d}V_{in}$	$\frac{d-1}{1-2d}V_{in}$
	V_{Lm2}^{Off}	$\frac{d}{1-2d}V_{in}$	$\frac{d}{1-2d}V_{in}$
Capacitor	V_{C1}	$\frac{d-1}{1-2d}V_{in}$	$\frac{d-1}{1-2d}V_{in}$
	V_{C2}	$\frac{d-1}{1-2d}V_{in}$	$\frac{d-1}{1-2d}V_{in}$
	V_{C3}	$(1+\left(\frac{2nd}{1-2d}\right))V_{in}$	$\frac{3-2d}{1-2d}V_{in}$
Diode	V_{Din}	$\frac{1}{1-2d}V_{in}$	$\frac{1}{1-2d}V_{in}$
	V_{D1}	$\frac{2nd+0.5}{1-2d}$	$\frac{1}{1-2d}V_{in}$
	V_{D2}	$\frac{2nd+0.5}{1-2d}$	$\frac{1}{1-2d}V_{in}$
Switch	V_Q	$\frac{1}{1-2d}V_{in}$	$\frac{1}{1-2d}V_{in}$
Voltage Gain		$(1+\left(\frac{2nd}{1-2d}\right))$	$\frac{3-2d}{1-2d}$

$$I_{C2}^{On} = -I_{Lm2} \tag{20}$$

$$I_{C3}^{On} = -I_o \tag{21}$$

$$I_{Cin}^{off} = I_{in} - I_{N12} - I_{N22} - I_{C1}^{off} \tag{22}$$

$$I_{C1}^{Off} = I_{Lm2} - n_2 I_{N22} \tag{23}$$

$$I_{C2}^{Off} = I_{Lm1} - n_1 I_{N22} \tag{24}$$

$$I_{C3}^{Off} = I_{N22} - I_o \tag{25}$$

By applying the ampere-second balance rule, which states that a capacitor's average current must be zero in steady state, a set of equations governing the voltages and currents of capacitors C_1, C_2, and C_3 is obtained by analyzing their currents over one full switching cycle in CCM:

$$\langle I_{C3} \rangle_T = 0 \overset{yields}{\rightarrow} I_{N12} = I_{N22} = \frac{I_o}{1-d} \tag{26}$$

$$\begin{cases} \langle I_{C1}\rangle_T = 0 \rightarrow I_{Lm1} = \frac{1-d}{d} I_{Lm2} - \frac{n_2}{d} I_o \\ \langle I_{C2}\rangle_T = 0 \rightarrow I_{Lm2} = \frac{1-d}{d} I_{Lm1} - \frac{n_1}{d} I_o \end{cases} \rightarrow \\ I_{Lm1} = \frac{(1-d)n_1+dn_2}{1-2d} I_o \\ I_{Lm2} = \frac{(1-d)n_2+dn_1}{1-2d} I_o \quad (27)$$

From Eqs. (18)- (27), the following relationships are obtained:

$$I_{C1}^{On} = -\frac{(1-d)\,n_1 + dn_2}{1-2d} I_o \quad (28)$$

$$I_{C2}^{On} = -\frac{(1-d)\,n_2 + dn_1}{1-2d} I_o \quad (29)$$

$$I_{C3}^{On} = -I_o \quad (30)$$

$$I_{C1}^{Off} = \left(\frac{(1-d)\,n_2 + dn_1}{1-2d} - \frac{n_2}{1-d}\right) I_o \quad (31)$$

$$I_{C2}^{Off} = \left(\frac{(1-d)\,n_1 + dn_2}{1-2d} - \frac{n_1}{1-d}\right) I_o \quad (32)$$

$$I_{C3}^{Off} = \frac{dI_o}{1-d} \quad (33)$$

By utilizing the circuit diagram in both states and Eqs. (28)–(33), it is possible to calculate the current stress for Diodes and Q switch. These current stresses refer to the equivalent average currents during conduction state rather than the entire switching period.

$$I_{Din} = \frac{MI_o}{1-d} \quad (34)$$

$$I_{D1} = I_{D2} = \frac{I_o}{1-d} \quad (35)$$

$$I_Q = -I_{C1}^{on} - I_{C2}^{on} = \frac{n_1+n_2}{1-2d} I_o \quad (36)$$

Table 2 compares the current stress of components of this circuit and [22]. Also, in Table 3, the proposed converter is compared in terms of voltage gain, circuit complexity and voltage stress on semiconductors with some similar converters. The RMS value of the above parameters can be calculated as follows:

$$I_{Din,RMS} = \sqrt{1-d} * (\frac{MI_o}{1-d}) I_o \quad (37)$$

$$I_{D1,RMS} = I_{D2,RMS} = \sqrt{1-d} * \frac{1}{1-d} I_o \quad (38)$$

$$I_{Q,RMS} = \sqrt{d} * \frac{n_1+n_2}{1-2d} I_o \quad (39)$$

Fig. 8 shows a comparison of the voltage gain of the proposed converter to other converters from Table 3 for a set value of $n = 4$. Fig. 9 and Fig. 10 display the normalized voltage stress values for the diodes and switches, respectively, in the converters. The comparison in Fig. 8 demonstrates that the proposed converter has a considerably higher voltage gain than most of the referenced converters. This is especially notable given that the voltage stress on the diodes in the proposed converter is at a reasonable level compared to the other circuits, as seen in Fig. 9. In essence, the proposed converter achieves an impressively high voltage gain without sacrificing reasonable diode voltage stress.

Table 2. Compare current stress in the proposed converter and [22] ($n_1 = n_2 = n$).

Component	Parameter	Proposed	[22]
Capacitor	I_{C1}^{On}	$\frac{nI_o}{2d-1}$	$\frac{I_o}{d(2d-1)}$
	I_{C1}^{Off}	$-\frac{ndI_o}{(1-d)(2d-1)}$	$-\frac{I_o}{(1-d)(2d-1)}$
	I_{C2}^{On}	$\frac{nI_o}{2d-1}$	$\frac{I_o}{d(2d-1)}$
	I_{C2}^{Off}	$-\left(\frac{n}{2d-1}+\frac{n}{1-d}\right) I_o$	$-\frac{I_o}{(1-d)(2d-1)}$
	I_{C3}^{On}	$-I_o$	$-I_o$
	I_{C3}^{Off}	$\frac{dI_o}{1-d}$	$\frac{dI_o}{1-d}$
Inductor	I_{Lm1}	$-\frac{n}{2d-1} I_o$	$-\frac{2}{2d-1} I_o$
	I_{Lm2}	$-\frac{n}{2d-1} I_o$	$-\frac{2}{2d-1} I_o$
Diode	I_{Din}	$\frac{MI_o}{1-d}$	$\frac{-3+2d}{(1-d)(2d-1)} I_o$
	I_{D1}	$\frac{I_o}{1-d}$	$\frac{I_o}{1-d}$
	I_{D2}	$\frac{I_o}{1-d}$	$\frac{I_o}{1-d}$
Switch	I_Q	$-\frac{2n}{2d-1} I_o$	$-\frac{2}{d(2d-1)} I_o$

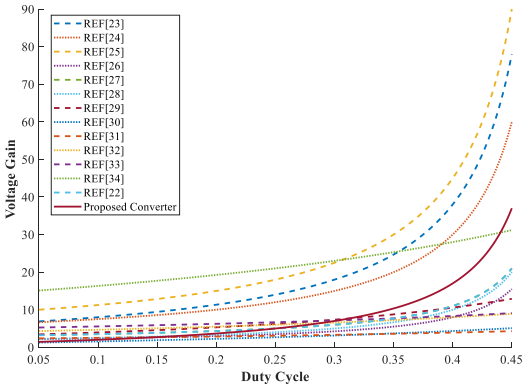

Fig. 8. Comparison of voltage gain of introduced topologies and proposed converter.

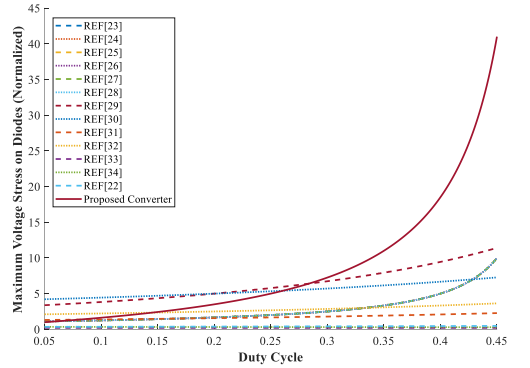

Fig. 9. Comparison of normalized maximum voltage stress on diodes in introduced topologies and proposed converter.

2.5. Switch utilization

Switch utilization is an essential metric for comparing the performance of different types of DC-DC converters. It measures how efficiently the switches in a converter handle the power transfer from the input to the output. A higher switch utilization means the switch can deliver more power to the output with less stress and loss. Fig. 11 shows the switch utilization parameter for different turn ratios and Duty-Cycles. Switch utilization can be defined as the ratio of output power to switch power:

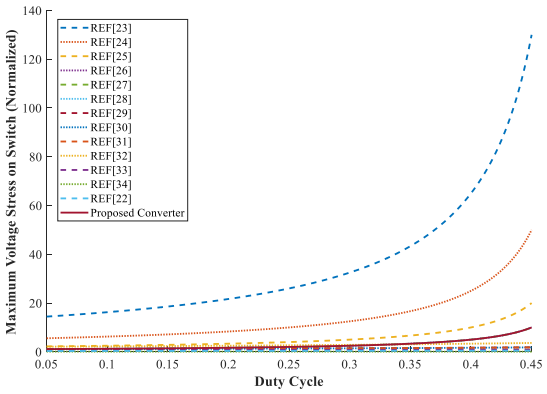

Fig. 10. Comparison of normalized maximum voltage stress on switches in introduced topologies and proposed converter.

$$SU = \frac{P_{out}}{P_{sw}} = \frac{M\,(1-d)\,(1-2d)}{\sqrt{d}\,(M-1)} \tag{40}$$

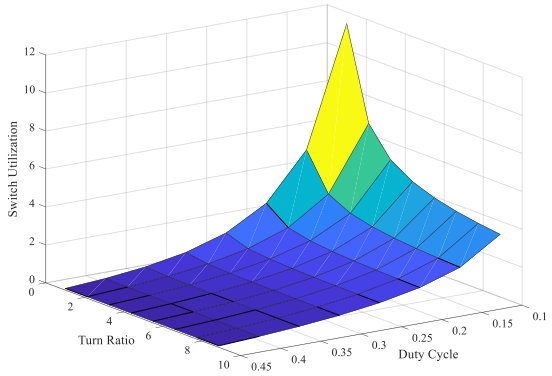

Fig. 11. Switch utilization for $0.1 < d < 0.45$ and $1 < n < 10$.

3. DESIGN CONSIDERATIONS FOR CONVERTER

3.1. Selecting semiconductor devices

To ensure safe operation, the voltage and current ratings of semiconductor devices must exceed the calculated voltage stresses Eqs. (15)- (17) and current stresses Eqs. (34)- (36) within the safety operation area (SOA).

3.2. Magnetizing inductors design

For designing magnetizing inductors, we should consider the desired value of the current ripple in Table 4, one can acquire an appropriate value for the desired magnetizing inductor.

$$V_{Lm1} = L_{m1}\frac{\Delta I_{Lm1}}{dT} \overset{yields}{\rightarrow} L_{m1} = \frac{dV_{in}\frac{d-1}{2d-1}}{f\Delta I_{Lm1}} \tag{41}$$

$$V_{Lm2} = L_{m2}\frac{\Delta I_{Lm2}}{dT} \overset{yields}{\rightarrow} L_{m2} = \frac{dV_{in}\frac{d-1}{2d-1}}{f\Delta I_{Lm2}} \tag{42}$$

3.3. Capacitors design

Similarly, for selecting the optimum value of capacitors, we can obtain that:

$$I_{Cin} = C_{in}\frac{\Delta V_{Cin}}{dT} \overset{yields}{\rightarrow} C_{in} = \frac{d}{f\Delta V_{Cin}}I_{in} = \frac{d}{f\Delta V_{Cin}}M_{CCM}I_o \tag{43}$$

$$I_{C1} = C_1\frac{\Delta V_{C1}}{dT} \overset{yields}{\rightarrow} C_1 = \frac{d}{f\Delta V_{C1}}\frac{(d-1)\,n_1 + dn_2}{1-2d}I_o \tag{44}$$

$$I_{C2} = C_2\frac{\Delta V_{C2}}{dT} \overset{yields}{\rightarrow} C_2 = \frac{d}{f\Delta V_{C2}}\frac{(d-1)\,n_2 + dn_1}{1-2d}I_o \tag{45}$$

$$I_{C3} = C_3\frac{\Delta V_{C3}}{dT} \overset{yields}{\rightarrow} C_3 = \frac{-dI_o}{f\Delta V_{C3}} \tag{46}$$

4. EFFICIENCY ANALYSIS

To determine the efficiency of the converter, it is necessary to consider both the switching and conduction losses of power semiconductors. However, by utilizing ultra-fast or Schottky diodes, it is possible to disregard the switching loss associated with diodes.

$$\begin{aligned} &P_Q = P_{cond} + P_{switching} = \\ &I^2_{QRMS} * R_{DS,On} + \tfrac{1}{2}V^2_Q * C_{oss} * f_{SW} = \\ &d * \tfrac{(n_1+n_2)^2}{(1-2d)^2}I_o * R_{DS,on} + \\ &\tfrac{V^2_{in}(n_1+n_2)}{(1-2d)^3}I_O * Coss * f_{SW} \end{aligned} \tag{47}$$

However, the conduction loss of switch and diodes is calculated by:

$$\begin{aligned} &P_D = P_{Din} + P_{D1} + P_{D2} = \\ &V_{D,F}\left(I_{Din,avg} + I_{D1,avg} + I_{D2,avg}\right) + \\ &R_D\left(I^2_{Din,RMS} + I^2_{D1,RMS} + I^2_{D2,RMS}\right) = \\ &V_{D,F}\left(\tfrac{MI_o}{1-d} + \tfrac{I_o}{1-d} + \tfrac{I_o}{1-d}\right) + \\ &R_D\left(\tfrac{M^2I^2_o}{1-d} + \tfrac{I^2_o}{1-d} + \tfrac{I^2_o}{1-d}\right) = \\ &\tfrac{V_{D,F}(M+2)I_o}{1-d} + \tfrac{R_D\left(M^2+2\right)I^2_o}{1-d} \end{aligned} \tag{48}$$

Fig. 12 shows the percent of total dissipated power per output power for five different values of turn ratio. Also, in Fig. 13, this comparison for different duty cycle values is presented. Fig. 14 shows the share of each efficiency parameter in dissipating output power.

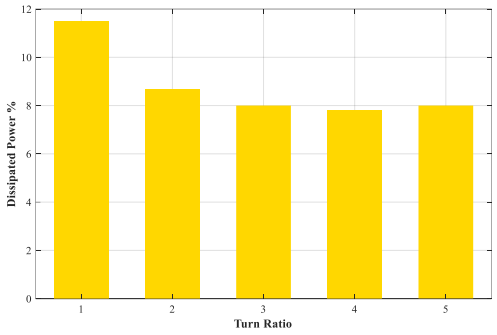

Fig. 12. Percentage of dissipated power for d $=\frac{1}{3}$ and $1 < n < 5$.

Table 3. Comparison of the proposed converter with another existing converter.

Converter	Voltage gain (G)	Magnetic cores/ Windings	Number of C	D	S	Max voltage stress on diodes	Max voltage stress on switches
[23]	$\frac{2+n+dn}{1-2d}$	2/3	5	4	1	$\frac{2G+n}{4+3n}$	$\frac{(2G+n)(1+3n)}{4+3n}$
[24]	$\frac{2+n}{1-2d}$	2/3	5	4	1	$\frac{G}{2+n}$	$\frac{G(1+n)}{2+n}$
[25]	$\frac{1+2n}{1-2d}$	1/2	3	4	2	$\frac{G}{1+2n}$	$\frac{2Gn}{1+2n}$
[21]	$\frac{2n}{1-2d}$	2/3	7	5	2	$\frac{G}{2n}$	$\frac{G}{2}$
[26]	$\frac{2-d}{1-2d}$	2/3	4	3	1	$\frac{2G-1}{3}$	$\frac{2G-1}{3}$
[27]	$\frac{3-2d}{1-2d}$	2/3	5	4	1	$\frac{G-1}{2}$	$\frac{G-1}{2}$
[28]	$\frac{2}{1-2d}$	1/1	4	5	2	$\frac{G}{2}$	$\frac{G}{2}$
[29]	$\frac{2d+n-1}{(1-d)^2}$	2/4	4	4	2	$\frac{n+d-1}{n+2d-1}G$	$\frac{1-d}{2d+n-1}G$
[30]	$\frac{1+nd}{1-d}$	1/3	3	2	1	$\frac{n(G+n)}{n+1}$	$\frac{1}{1-d}$
[31]	$\frac{1+2n+d}{(1-d)n}$	2/4	5	4	1	$\frac{(1+n)(1+nG)}{2n+2n^2}$	$\frac{1+nG}{2+2n}$
[32]	$\frac{4+2d}{1-d}$	3/3	7	6	1	$\frac{2G}{4+2d}$	$\frac{2G}{4+2d}$
[33]	$\frac{1+n}{1-d}$	1/2	3	3	1	$\frac{1}{1+n}$	$\frac{n}{1+n}$
[34]	$1+\frac{1+3n+2dn}{1-d}$	2/6	8	9	2	$\frac{n+1}{2+3n+2dn-d}$	$\frac{1}{2+3n+2dn-d}$
[22]	$\frac{3-2d}{1-2d}$	3/3	6	4	1	$\frac{1}{3-2d}$	$\frac{1}{3-2d}$
Proposed	$1+\left(\frac{2nd}{1-2d}\right))$	2/4	4	3	1	$\frac{2nd+0.5}{1-2d}$	$\frac{1}{1-2d}$

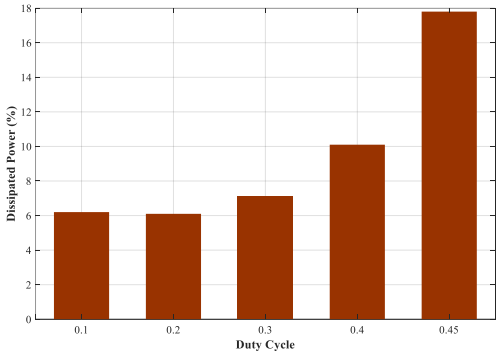

Fig. 13. Percentage of dissipated power for $n = 4$ and $0.1 < d < 0.45$.

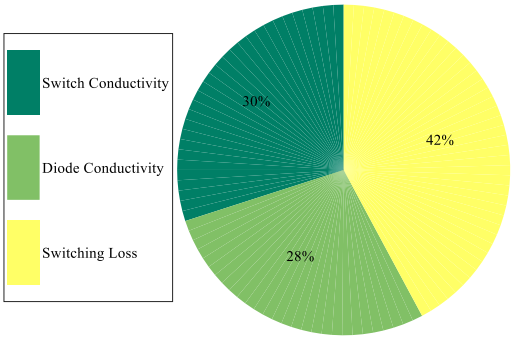

Fig. 14. Share of each parameter in dissipated power for $n = 4$ and $d = \frac{1}{3}$.

5. SMALL SIGNAL ANALYSIS OF PROPOSED CONVERTER

5.1. State Space Averaging technique

State-Space Averaging (SSA) is a mathematical technique for small-signal analysis of DC-DC converters. It is used to simplify the analysis of these circuits by transforming the original nonlinear circuit into an equivalent linear system. The technique assumes that the converter operates in a steady state and that small-signal variations are superimposed on it.

The SSA technique has several advantages over other methods, such as the small-signal equivalent circuit model. Firstly, it provides a more accurate representation of the converter dynamics since it considers the effect of the switching on the circuit behavior. Secondly, it allows for a more efficient circuit analysis, while it reduces the number of variables and equations required to describe the circuit. It makes the analysis more computationally efficient and easier to understand.

5.2. SSA of the proposed converter

By utilizing the differential equations for both operating modes and employing the averaging technique to analyze these equations over a single switching period, we obtain:

$$I_{C1} = -dI_{Lm1} + (1-d) * \left(I_{Lm2} - \frac{n_2(I_{Lm1}+I_{Lm2})}{n_1-n_2-1}\right) + \frac{V_{C3}^2}{RV_{in}(n_1-n_2-1)} \tag{49}$$

$$I_{C2} = -dI_{Lm2} + (1-d)\left(I_{Lm1} - \frac{n_1(I_{Lm1}+I_{Lm2})}{n_1-n_2-1}\right) + \frac{V_{C3}^2}{RV_{in}(n_1-n_2-1)} \tag{50}$$

$$I_{C3} = -d\frac{V_{C3}}{R} + (1-d)\left(\frac{I_{Lm1}+I_{Lm2}}{n_1-n_2-1} - V_{C3}\right) - \frac{V_{C3}^2}{RV_{in}(n_1-n_2-1)} \tag{51}$$

$$V_{Lm1} = dV_{C1} + (1-d)(V_{in} - V_{C2}) \tag{52}$$

$$V_{Lm2} = dV_{C2} + (1-d)(V_{in} - V_{C1}) \tag{53}$$

To express the SSA representation of the suggested converter in matrix form, we can linearize Eqs. (49)- (53) around the previously determined equilibrium point. By doing so, we can streamline the analysis and design process for the converter and gain a better understanding of its dynamic characteristics. The SSA of the proposed converter can be obtained in matrix form through the following derivation:

$$\begin{cases} \dot{x} = A\hat{x} + B\hat{u} \\ y = C\hat{x} \end{cases} \tag{54}$$

Table 4. Specifications and values of components in the proposed converter.

Desired Parameter	Value	Designed Parameter	Value
$Frequency$	100 KHz	$n_1,\ n_2$	4
V_in	50 V	$Duty\ Cycle$	0.33
V_out	450 V	$L_m1,\ L_m2$	330 μH
$Power$	450 W	$C_1,\ C_2$	130 μF
$\Delta I_{Lm1},\ \Delta I_{Lm2}$	1 A	C_3	10 μF
$\Delta V_{C1},\ \Delta V_{C2}$	0.3 V	R	450 Ω
ΔV_{C3}	0.5V		

Where the subscript Λ denotes the linearized terms of the state and input variables and:

$$\hat{x}^T = \begin{bmatrix} V_{C1} & V_{C2} & V_{C3} & I_{Lm1} & I_{Lm2} \end{bmatrix} \tag{55}$$

$$\hat{u}^T = \begin{bmatrix} d & V_{in} \end{bmatrix} \tag{56}$$

$$G_{vod} = C\left(SI - A\right)^{-1} B \tag{57}$$

$$\begin{bmatrix} 0 & 0 & \frac{2V_{C3}}{RV_{in}(n_1-n_2-1)C_1} & \frac{(d-1)n_2}{n_1-n_2-1}-d & \frac{(1-d)(n_1-2n_2-1)}{(n_1-n_2-1)C_1} \\ 0 & 0 & \frac{2V_{C3}}{RV_{in}(n_1-n_2-1)C_2} & \frac{(d-1)(n_2+1)}{(n_1-n_2-1)C_2} & \frac{n_1(d-1)}{n_1-n_2-1}-d \\ 0 & 0 & -\frac{1}{RC_3}-\frac{2V_{C3}}{RV_{in}(n_1-n_2-1)C_3} & \frac{1-d}{(n_1-n_2-1)C_3} & \frac{1-d}{(n_1-n_2-1)C_3} \\ \frac{d}{L_{m1}} & \frac{(d-1)}{L_{m1}} & 0 & 0 & 0 \\ \frac{d-1}{L_{m2}} & \frac{d}{L_{m2}} & 0 & 0 & 0 \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{(\frac{2n_2-n_1+1}{n_1-n_2-1})(I_{Lm1}+I_{Lm2})}{C_1} & 0 \\ \frac{n_2+1}{n_1-n_2-1}(I_{Lm1}+I_{Lm2})\frac{1}{C_2} & 0 \\ -\frac{I_{Lm2}+I_{Lm1}}{\frac{n_1-n_2-1}{C_3}} & 0 \\ \frac{V_{C2}+V_{C1}}{L_{m1}} & \frac{1-d}{L_{m1}} \\ \frac{V_{C2}+V_{C1}}{L_{m2}} & \frac{1-d}{L_{m2}} \end{bmatrix}, \quad C = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \end{bmatrix} \tag{58}$$

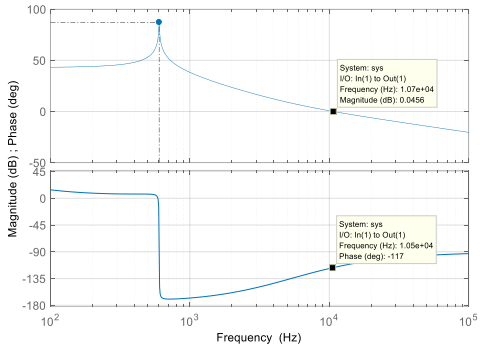

Fig. 15. Control-to-output transfer function bode diagram of the proposed converter.

So, by obtaining A, B and C, the control to output transfer function can be resulted. Fig. 15 provides the Bode diagram of the converter's control-to-output transfer function. This diagram demonstrates that the phase margin of the proposed converter is greater than 45 degrees, signifying a major enhancement in the stability compared to other converters. Analyzing the small signal stability is crucial to ensure the reliable performance of power

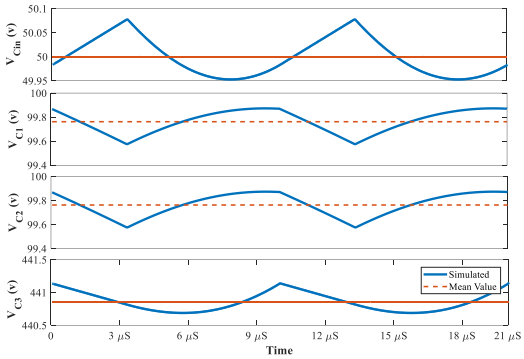

Fig. 16. Voltage of capacitors of the converter in simulation.

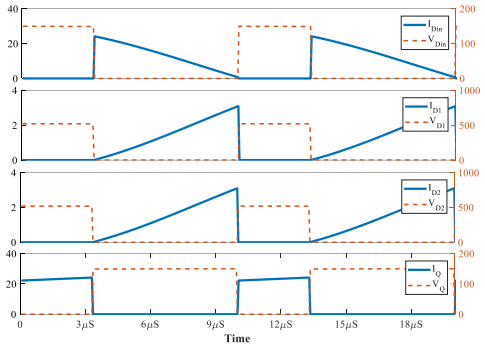

Fig. 17. Current stress of semiconductor devices of the converter in simulation.

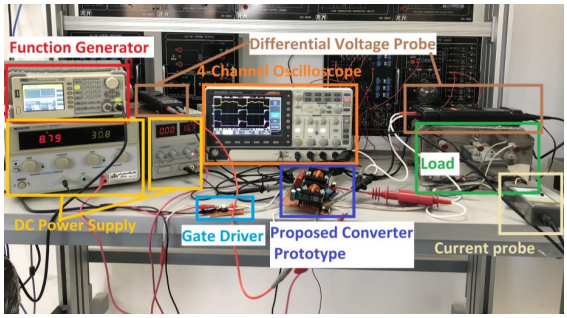

Fig. 18. Laboratory set-up for verifying performance of the proposed converter.

Table 5. Prototype specifications and elements.

Desired output power	150W
Desired gain	5
Input voltage	30V
Transformers (Core, N_2/N_1)	ETD39, 62/31
Duty cycle	0.33
Capacity and voltage of C_1 and C_3	47μF, 100V
Capacity and voltage of C_3	22μF, 250V
Inductance of magnetizing inductor L_m	330μH
Diodes D_1 and D_2	MBR10B200CRH
Mosfet	IRFP260N
Nominal load	150 Ω

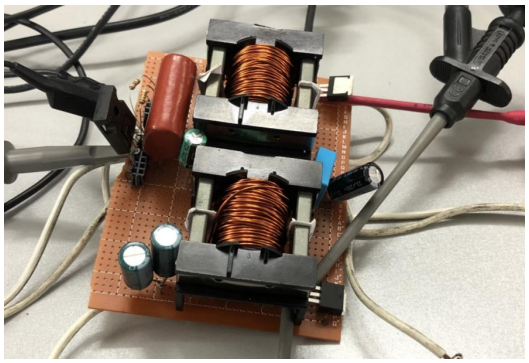

Fig. 19. Prototype of proposed converter.

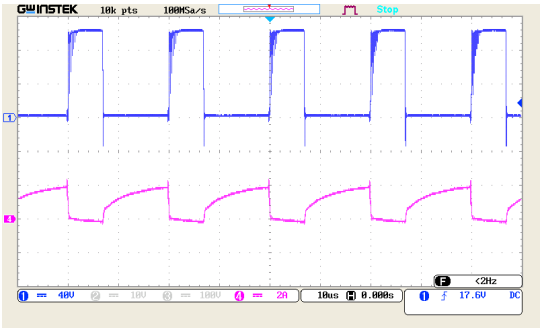

Fig. 20. Voltage and current of D_1. Channel 1 : V_{D1}, Channel 4 : I_{D1}.

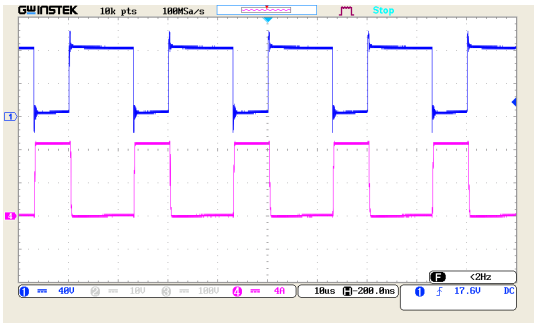

Fig. 21. Voltage and current across mosfet. Channel 1 : V_{DS}, Channel 4 : I_Q.

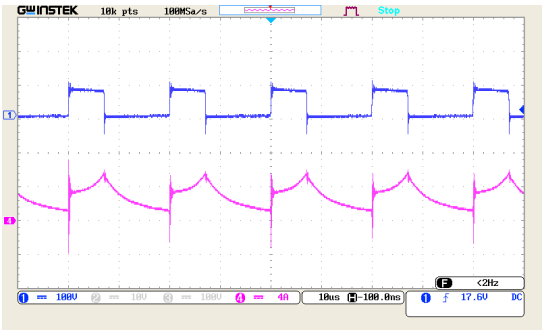

Fig. 22. Voltage and current across primary of transformer. Channel 1 : V_{N11}, Channel 4 : I_{N11}.

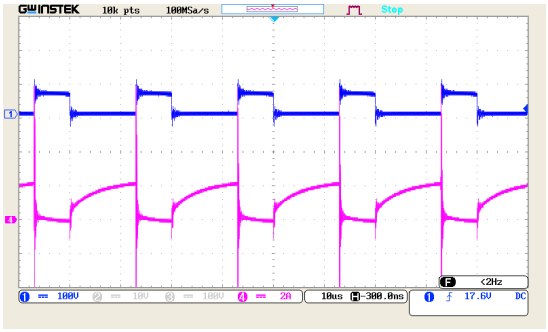

Fig. 23. Voltage and Current across secondary of transformer. Channel 1 : V_{N12}, Channel 4 : I_{N12}.

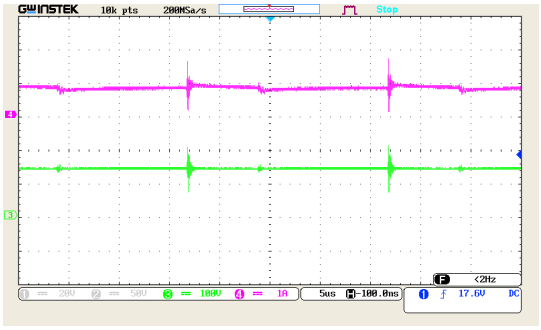

Fig. 24. Voltage and current of output. Channel 3 : V_o, Channel 4 : I_o.

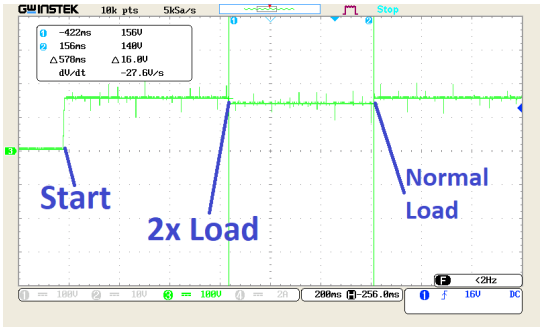

Fig. 25. Dynamic response of output voltage with changing load.

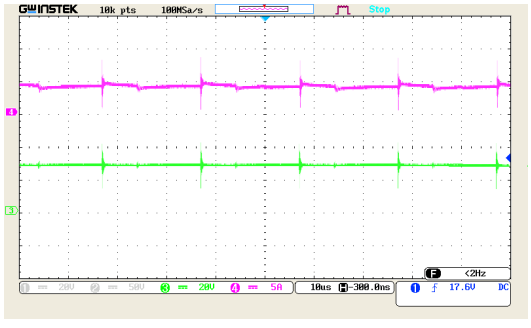

Fig. 26. Voltage and current of input DC source.

electronic converters.

The pole-zero plot for the converter transfer function model additionally verifies the stability traits. Specifically, there are two poles located on the Y-axis and two more poles to the left-hand side of the plot. Poles in the left half of the complex plane correlate to stable system dynamics. With multiple poles in

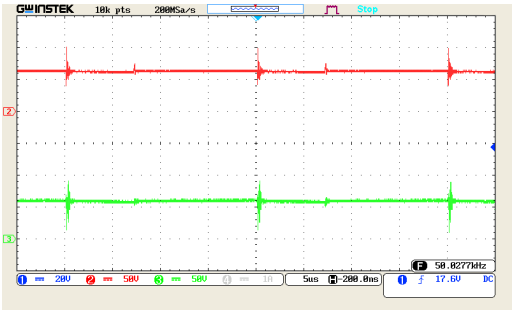

Fig. 27. Voltage of capacitor C_1 and C_2.

stable locations, the pole-zero configuration substantially improves stability robustness.

In summary, the Bode diagram and pole-zero plot illustrate superior small signal stability behavior, with ample design margin characterized by the large 45+ degree phase margin. The stability analysis confirms the proposed converter has highly favorable stability dynamics, setting it apart from prior converter designs that may have lacked small signal analysis or exhibited poorer stability performance.

6. SIMULATION RESULTS

The proposed converter's performance and validity were evaluated by simulating it in PSIM. Table 4 shows desired values of converter parameters and also designed values based on design considerations mentioned in Eqs. (40)- (46).

In Fig. 16, simulated voltage of C_1, C_2, C_3 and C_{in} is shown. According to Eqs. (10)- (13), expected voltage for C_{in} is 50V. V_{C1} and V_{C2} are identical and it is about 100V. Voltage of C_3 is as like as output voltage and expected value is 450V. Also Fig. 17 shows current of semiconductor devices across a period. According to Eqs. (34)- (36), I_{Din} should be 9A, $I_{D1,2}$ is 1A and equal to output current. Also, the switch current is 9A and approved in simulation.

7. EXPERIMENTAL VERIFICATION

To verify performance and effectiveness of the proposed converter, a 150W prototype with gain of 5 is provided. Input voltage of this sample is 30V and output is 150V with a 1A load. Fig. 18 shows the laboratory set-up and prototype of the converter. To obtain the desired voltage gain, the turns ratio of the transformers was configured to 2:1 and the duty cycle was set to 0.35. Switching frequency is selected 50KHz and desired pulse generated with a GPS-2125 function generator. Based on these parameters, we can consider capacity of C_1 and C_2 and inductance of L_{m1} and L_{m2} and accordingly transformers core and other parameters can be designed. Also based on operational parameters we can select semiconductor devices. Selected components and operating parameters are represented in Table 5 Also Fig. 19 represents prototype of the proposed circuit.

We used a GWInstek GDS-2104E 4-channel storage oscilloscope with a 1GS/s sampling rate to demonstrate signals. GWInstek PA-677 current probe, GWInstek GDP-025 and GDP-100 differential voltage probes, and GWInstek GTP070 Voltage probe were employed to present waveform of currents and voltages of the circuit.

Fig. 20 shows the voltage and current of D_1. The waveform of D_1 is similar to that of D_2 due to the symmetrical nature of the circuit. Fig. 21 presents voltage and current across mosfet. Respectively, Fig. 22 and Fig. 23 shows current in primary and secondary of the transformer. Voltage and current across the load are represented in Fig. 24.

To verify the dynamic operation of the converter, the load was changed from 300 ohms to 150 ohms and then returned to the initial 300 ohms value. Fig. 25 represents the results of this test. The output voltage changed by about 10% under the heavier load.

Fig. 26 represents voltage and current of input DC source. also Fig. 27 shows voltage of switched capacitors (C_1 and C_2).

8. CONCLUSION

This paper has presented a novel Z-source DC-DC converter topology integrated with built-in transformers to achieve high voltage step-up conversion suitable for PV applications. The proposed converter combines the switched inductor technique with an innovative Z-source network configuration, addressing limitations in prior arts related to gain, voltage stresses, efficiency, stability, and complexity. The detailed steady-state analysis indicates the converter can readily achieve considerable voltage gains, exceeding most referenced topologies, without sacrificing reasonable voltage stress levels. This superior gain is enabled by the integrated transformer windings and optimized positioning of capacitors and diodes. Furthermore, the built-in transformer provides two degrees of control freedom to flexibly tune the voltage conversion ratio.

The efficiency and loss analysis highlights the low conduction losses in the converter, with the switch loss being the dominant factor. However, even with light loading, the efficiency remains high due to the low current stress. The comprehensive comparison also verifies the reduced voltage stress on diodes and superior gain. The small signal modeling proves the converter's stability robustness, evident by the high 45 degree phase margin. The pole-zero plot further confirms stable system dynamics. This analysis ensures reliable performance without oscillations or distortions. Extensive simulations validate the theoretical analysis and design considerations over a wide operating range. The experimental prototype confirms functionality and the unique advantages of high gain, high efficiency, and flexibility furnished by the proposed topology. The proposed converter indicates several promising directions for further investigation of enabling technologies for next-generation PV systems:

1) Exploration of alternative control schemes like peak current mode control to enhance dynamic response.
2) Quantification of efficiency improvements utilizing latest wide bandgap MOSFETs and GaN diodes to minimize losses.
3) Reducing voltage stress on semiconductor devices specially switches.
4) Feasibility assessment of transformer integration approaches like matrix transformers to further improve power density.

REFERENCES

[1] K. Alluhaybi, I. Batarseh, and H. Hu, "Comprehensive review and comparison of single-phase grid-tied photovoltaic microinverters," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 8, no. 2, pp. 1310–1329, 2019.

[2] G. Palumbo and D. Pappalardo, "Charge pump circuits: An overview on design strategies and topologies," *IEEE Circuits Syst. Mag.*, vol. 10, no. 1, pp. 31–45, 2010.

[3] R. Beiranvand, "Regulating the output voltage of the resonant switched-capacitor converters below their resonant frequencies," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5236–5249, 2017.

[4] G. Tan, J. Wang, and Y. Ji, "Soft-switching flyback inverter with enhanced power decoupling for photovoltaic applications," *IET Electr. Power Appl.*, vol. 1, no. 2, pp. 264–274, 2007.

[5] K. Yari, H. Mojallali, and S. H. Shahalami, "A new coupled-inductor-based buck–boost dc–dc converter for pv applications," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 687–699, 2021.

[6] B. Allahverdinejad, S. A. Modaberi, and A. Ajami, "A non-isolated buck-boost dc–dc converter with continuous input current and wide conversion ratio range for photovoltaic applications," in *2022 13th Power Electron. Drive Syst. Technol. Conf.*, pp. 491–497, IEEE, 2022.

[7] S. Habibi, R. Rahimi, M. Ferdowsi, and P. Shamsi, "Coupled inductor-based single-switch quadratic high step-up dc–dc converters with reduced voltage stress on switch," *IEEE J. Emerging Sel. Top. Ind. Electron.*, vol. 4, no. 2, pp. 434–446, 2022.

[8] J. Ai, M. Lin, and M. Yin, "A family of high step-up cascade dc–dc converters with clamped circuits," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4819–4834, 2019.

[9] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, 2003.

[10] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion part i: A topological review," *IEEE Trans. power Electron.*, vol. 30, no. 2, pp. 699–716, 2014.

[11] B. Zhao, Q. Yu, Z. Leng, and X. Chen, "Switched z-source isolated bidirectional dc–dc converter and its phase-shifting shoot-through bivariate coordinated control strategy," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4657–4670, 2011.

[12] M. Zhu, K. Yu, and F. L. Luo, "Switched inductor z-source inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 2150–2158, 2010.

[13] H. Shen, B. Zhang, D. Qiu, and L. Zhou, "A common grounded z-source dc–dc converter with high voltage gain," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2925–2935, 2016.

[14] A. Chub, O. Husev, D. Vinnikov, and F. Blaabjerg, "Novel family of quasi-z-source dc/dc converters derived from current-fed push-pull converters," in *2014 16th Eur. Conf. Power Electron. Appl.*, pp. 1–10, IEEE, 2014.

[15] M. Veerachary and P. Kumar, "Analysis and design of sixth order quasi-z-source dc-dc boost converter," in *2019 IEEE Int. Conf. Sustainable Energy Technol. Syst.*, pp. 347–352, IEEE, 2019.

[16] Y. Zhang, J. Shi, L. Zhou, J. Li, M. Sumner, P. Wang, and C. Xia, "Wide input-voltage range boost three-level dc–dc converter with quasi-z source for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6728–6738, 2016.

[17] H. Shen, B. Zhang, and D. Qiu, "Hybrid z-source boost dc–dc converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 310–319, 2016.

[18] T. Takiguchi and H. Koizumi, "Quasi-z-source dc-dc converter with voltage-lift technique," in *IECON 2013-39th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 1191–1196, IEEE, 2013.

[19] M. M. Haji-Esmaeili, E. Babaei, and M. Sabahi, "High step-up quasi-z source dc–dc converter," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10563–10571, 2018.

[20] Y. Wang, Q. Bian, X. Hu, Y. Guan, and D. Xu, "A high-performance impedance-source converter with switched inductor," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3384–3396, 2018.

[21] A. Nafari and R. Beiranvand, "An extendable interleaved quasi z-source high step-up dc–dc converter," *IEEE Trans. Power Electron.*, vol. 38, no. 4, pp. 5065–5076, 2023.

[22] R. Rahimi, S. Habibi, M. Ferdowsi, and P. Shamsi, "Z-source-based high step-up dc–dc converters for photovoltaic applications," *IEEE J. Emerging Sel. Top. Power Electron.*, vol. 10, no. 4, pp. 4783–4796, 2021.

[23] A. Samadian, S. H. Hosseini, and M. Sabahi, "A new three-winding coupled inductor nonisolated quasi-z-source high step-up dc–dc converter," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11523–11531, 2021.

[24] A. Samadian, S. H. Hosseini, M. Sabahi, and M. Maalandish, "A new coupled inductor nonisolated high step-up quasi z-source dc–dc converter," *IEEE Trans. Ind. Electron.*, vol. 67, no. 7, pp. 5389–5397, 2019.

[25] N. Yang, J. Zeng, R. Hu, and J. Liu, "Novel non-isolated high step-up converter with fewer passive devices and low voltage stress of power switches," *IET Power Electron.*, vol. 13, no. 11, pp. 2302–2311, 2020.

[26] G. Zhang, Z. Wu, S. Y. Shenglong, H. Trinh, and Y. Zhang, "Four novel embedded z-source dc–dc converters," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 607–616, 2021.

[27] S. Rostami, V. Abbasi, and T. Kerekes, "Switched capacitor based z-source dc–dc converter," *IET Power Electron.*, vol. 12, no. 13, pp. 3582–3589, 2019.

[28] V. F. Pires, A. Cordeiro, D. Foito, and J. F. Silva, "A dc-dc converter with capability to support the voltage balance of dc bipolar microgrids," in *2022 11th Int. Conf. Renewable Energy Res. Appl.*, pp. 50–55, IEEE, 2022.

[29] S. Hasanpour and T. Nouri, "New coupled-inductor high-gain dc/dc converter with bipolar outputs," *IEEE Trans. Ind. Electr.*, vol. 71, no. 3, pp. 2601–2613, 2023.

[30] T. Yao, Y. Cheng, Y. Guan, W. Wang, Y. Wang, and D. Xu, "A family of high step-up dc-dc converters based on enhanced boost cells with coupled inductor," *IEEE Trans. Power Electron.*, 2023.

[31] M. Yang, Y. Weng, H. Li, J. Lin, X. Yan, and T. Jin, "A novel three-winding coupled inductor-based high gain dc-dc converter with low switch stress and continuous input current," *IEEE Trans. Power Electron.*, 2023.

[32] E. Naderi, S. Seyedshenava, and H. Shayeghi, "High gain dc/dc converter implemented with mppt algorithm for dc microgrid system," *J. Oper. Autom. Power Eng.*, vol. 11, no. 3, pp. 213–222, 2023.

[33] H. Shayeghi, S. Pourjafar, S. Hashemzadeh, and F. Sedaghati, "A dc-dc converter with high voltage conversion ratio recommended for renewable energy application," *J. Oper. Autom. Power Eng.*, vol. 12, no. 3, pp. 186–194, 2024.

[34] S. M. Salehi, S. M. Dehghan, and S. Hasanzadeh, "Interleaved-input series-output ultra-high voltage gain dc–dc converter," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3397–3406, 2018.