Journal of Operation and Automation in Power Engineering

Vol. 14, No. 3, Aug. 2026, Pages: 233-240

http://joape.uma.ac.ir

Research Paper

Predictive Current Control of PMSM Drive Supplied with 4-Level Diode-Clamped Inverter

Pegah Hamedani [1, *] and *Sajad Sadr* [2]

[1]*Department of Railway Engineering and Transportation Planning, University of Isfahan, Isfahan, Iran.*
[2]*Faculty of Electrical Engineering, Tafresh University, Tafresh, Iran.*

Abstract— *A mandatory issue in the control of a permanent magnet synchronous motor (PMSM) drive is to overcome its nonlinear dynamic characteristics. This challenge becomes more severe when a multilevel diode-clamped inverter (DCI) is used for supplying the PMSM drive. In this case, it is indispensable to provide an accurate speed tracking performance as well as the capacitor voltage balance. The model predictive control (MPC) approach can properly solve this issue by considering different objectives in the cost function of the controller. This paper concentrates on the model predictive current control (MPCC) of the PMSM drive fed through a 4-level DCI. A comparative assessment of the 4-level DCI and 2-level VSI is performed in the PMSM drive with the MPCC approach. Different objectives are considered in the MPCC process including the d-q current control, limitation of the stator currents, voltage balance of capacitors, mitigating of the CM voltage, and reduction of the switching frequency. Simulation results reveal the superior dynamic performance and capacitor voltage balance in the suggested MPCC of PMSM drive with the 4-level DCI. Results manifest that the current total harmonic distortion (THD) and the torque ripple are lower in the PMSM drive with a 4-level DCI than with the 2-level VSI. The current THD is reduced from 8.61% in the 2-level VSI to 4.59% in the 4-level DCI. Moreover, the torque ripple is reduced from 1.2 Nm in the 2-level VSI to 0.32 Nm in the 4-level DCI.*

Keywords—Capacitor voltage balance, diode-clamped inverter, model predictive current control, permanent magnet synchronous motor, weighting factor.

1. INTRODUCTION

Permanent magnet synchronous motor (PMSM) offers significant privileges including high power density, high efficiency, and simple controllability [1]. Therefore, it is a beloved motor type in multifarious industries such as electric transportation. PMSMs have been the subject of lots of research studies [2]. In [3], a novel structure for the PMSM is suggested that yields higher efficiency and reliability and reduces the torque ripples. Results manifest that the torque ripple is alleviated from 36% to 4%. In [4], a new configuration is proposed for noteworthy attenuation of the cogging force and considerable improvement of the back EMF waveform. In this structure, the rectangular magnets are replaced by segmented magnets. Genetic algorithm has been utilized to determine the optimal width of the magnets and decrease the amount of magnets used.

Until now, different control methods have been developed for PMSM drives [5]. Traditionally, field-oriented control (FOC) and direct torque control (DTC) have been utilized for PMSM drives [6]. Modern control methods such as sliding mode control (SMC) have been adopted for PMSM drives. In [7], a modified super-twisting sliding mode controller is developed to improve the dynamic speed response of the PMSM drive. In addition, the model predictive control is utilized in the current control loop to mitigate the chattering issue. Experimental results reveal faster speed response and lower overshoot in different operating conditions. In [8], a new sliding mode control has been designed for the PMSM drive by applying the hybrid reaching law. Experimental results show a considerable faster speed response and lower chattering. In recent years, new control strategies have been developed for PMSM drives. In [9], a new robust gain-scheduled control method has been suggested for PMSM drives. The proposed controller has been designed using the linear matrix inequalities and yields superior dynamic performance as well as robustness under parameter uncertainties and disturbances. In addition, model predictive control (MPC) [10] has been successfully applied for PMSM drives. MPC can be classified into various types:

- Model predictive current control (MPCC) [11]
- Model predictive torque control (MPTC) [12]
- Model predictive speed control methods (MPSC) [13]
- Model predictive flux control (MPFC) [10]

Generally, the MPCC is simpler and offers better dynamic performance. The FOC of the PMSM drive has two control loops. The outer control loop is responsible for the speed control of the PMSM drive while the inner control loop is related to the current control of the PMSM. In the MPCC method, the MPC is utilized as the current controller.

On the other hand, multilevel inverters (MLIs) are beloved inverter structures in different industrial applications that aim to produce low-distorted voltage and current [14]. In a specific

Received: 28 Aug. 2024
Revised: 29 Nov. 2024
Accepted: 01 Dec. 2024
*Corresponding author:
E-mail: p.hamedani@eng.ui.ac.ir (P. Hamedani)
DOI: 10.22098/joape.2025.15727.2209

switching frequency, an MLI can offer greater voltage ratings and has lower dv/dt on the switches than a two-level VSI. The most popular MLI structures are:

- Diode-clamped inverters (DCIs) [15]
- Flying capacitor inverters [16]
- Cascaded H-bridge inverters [17]

The efficiency in the DCI is high. The DCI doesn't need many capacitors and has low stress on power electronic switches. Consequently, DCIs can be suitably utilized in a large variety of industrial applications. Therefore, the focus of this work is on the 4-level DCI. On the other hand, the combination of MPC and DCI has been studied for various applications [18]. In [19], a new predictive control is proposed based on a multirate improving approach for multi-level DCIs. The suggested strategy results in a significant reduction of the calculation burden and makes it appropriate for practical applications. This method is validated on 3- and 5-level DCIs with a resistive-inductive load. The performance of the proposed predictive control in the case of motor loads was not studied in this work. In [20], a modified MPC strategy is developed for 4-level DCIs. The proposed strategy is simpler in comparison to the traditional MPC and results in 19.56% lower computational time with the same accuracy. Moreover, the THD index and switching frequency are significantly lower in the proposed MPC method than in the traditional MPC. However, the proposed method was only tested on the 4-level DCI with resistive-inductive loads. Thus, this strategy was not applied to electrical motor drives. On the other hand, a particular privilege of the MPC approach is the possibility of considering multifarious objective terms in the cost function. In [21], various objectives are introduced which can be optimized during the MPC process including voltage balancing, switching states, common mode voltage, and reactive power. In [22], a multistep prediction strategy has been applied for performance improvement of the DCI. In addition to the tracking behavior and capacitor voltage balance, the switching frequency and CM voltage have been investigated in different horizon lengths. Results revealed the superior dynamic characteristics of the 4-level DCI controlled by the MPC with a horizon of 2. Nevertheless, the results were only provided for a resistive-inductive load. Thus, further investigations must be performed on the electrical motor drives fed through multi-level DCIs. It is noteworthy that most of the previous research on the MPC of DCIs is focused on resistive-inductive loads and a research gap exists in the case of MPC of electrical motor drives supplied with DCIs. Inspired by the foregoing discussions, this paper endeavors to study the MPCC of the PMSM drive supplied with a 4-level DCI. A discrete PI regulator with anti-windup is used as the speed controller. Results are compared with the MPCC of the PMSM drive fed through the conventional 2-level VSI. The main contributions of this study are:

The main advantages of the proposed MPCC approach for the PMSM drive supplied with 4-level DCI are:

- Fast and accurate dynamic in the motor start, speed reversal, and load change conditions
- Low current THD and torque ripple
- Voltage balance of the capacitors in the motor start, speed reversal, and load change conditions

This manuscript is structured as follows: Section 2 describes the mathematical model of the four-level DCI. Section 3 explains the discrete-time model of the PMSM. Section 4 presents the MPCC strategy for the PMSM drive. Section 5 provides the simulation results of the MPCC for the PMSM drive supplied by the four-level DCI. Finally, Section 6 concludes the paper.

2. Mathematical Model of The 4-Level DCI

The structure of a three-phase 4-level DCI is shown in Fig. 1 The three-phase 4-level DCI includes eighteen IGBT switches with anti-parallel diodes, eighteen clamping diodes, and three capacitors. The IGBTs are arranged in up and down groups and obtain complementary gate signals [23].

The structure of a three-phase 4-level DCI is shown in Fig. 1. The three-phase 4-level DCI includes eighteen IGBT switches with anti-parallel diodes, eighteen clamping diodes, and three capacitors. The IGBTs are arranged in up and down groups and obtain complementary gate signals [23].

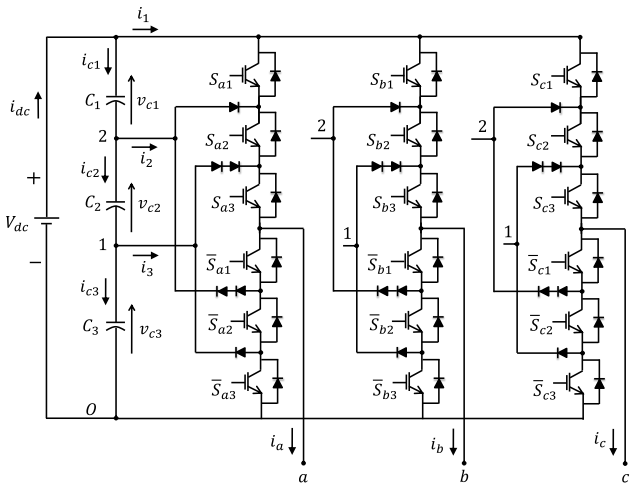

Fig. 1. The general topology of the 3-phase 4-level DCI [22].

According to Table 1, a single-phase 4-level DCI has 4 different switching states for generating 4 voltage levels. In consequence, $4^3 = 64$ different switching combinations exist in the three-phase 4-level DCI.

Table 1. Switching conditions of the 4-level DCI [23].

S_x	Voltage level	Switching signal		
		S_{x3}	S_{x2}	S_{x1}
0	0	0	0	0
1	v_{c3}	1	0	0
2	$v_{c2} + v_{c3}$	1	1	0
3	$v_{c1} + v_{c2} + v_{c3}$	1	1	1

The DCI phase voltages with respect to the negative DC-Link (v_{aO}, v_{bO}, and v_{cO}) can be expressed as a function of the switching signals [22]:

$$\begin{aligned} v_{aO} &= (v_{C1} + v_{C2} + v_{C3}) \cdot S_{a1}S_{a2}S_{a3} + \\ &(v_{C2} + v_{C3}) \cdot \bar{S}_{a1}S_{a2}S_{a3} + v_{C3} \cdot \bar{S}_{a1}\bar{S}_{a2}S_{a3} \\ v_{bO} &= (v_{C1} + v_{C2} + v_{C3}) \cdot S_{b1}S_{b2}S_{b3} + \\ &(v_{C2} + v_{C3}) \cdot \bar{S}_{b1}S_{b2}S_{b3} + v_{C3} \cdot \bar{S}_{b1}\bar{S}_{b2}S_{b3} \\ v_{cO} &= (v_{C1} + v_{C2} + v_{C3}) \cdot S_{c1}S_{c2}S_{c3} + \\ &(v_{C2} + v_{C3}) \cdot \bar{S}_{c1}S_{c2}S_{c3} + v_{C3} \cdot \bar{S}_{c1}\bar{S}_{c2}S_{c3} \end{aligned} \quad (1)$$

where v_{cj} is the j-th capacitor voltage ($j \in \{1, 2, 3\}$). S_{xy} is the switching signal of the y-th IGBT ($y \in \{1, 2, 3\}$) in phase x ($x \in \{a, b, c\}$) of the DCI (according to Fig. 1).

The phase voltages with respect to the load neutral (v_{an}, v_{bn}, and v_{cn}) are expressed as [22]:

$$\begin{aligned} v_{an} &= v_{aO} - v_{nO} \\ v_{bn} &= v_{bO} - v_{nO} \\ v_{cn} &= v_{cO} - v_{nO} \end{aligned} \quad (2)$$

where O is the negative DC-Link and n is the neutral point of the load. Moreover, the common-mode voltage v_{nO} can be calculated as [22]:

$$v_{nO} = \frac{v_{aO} + v_{bO} + v_{cO}}{3} \tag{3}$$

The discrete-time model of the capacitor voltages is given by [23]:

$$v_{c1}(k+1) = v_{c1}(k) + \frac{T_s}{C_1} i_{c1}(k) \tag{4}$$

$$v_{c2}(k+1) = v_{c2}(k) + \frac{T_s}{C_2} i_{c2}(k) \tag{5}$$

$$v_{c3}(k+1) = v_{c3}(k) + \frac{T_s}{C_3} i_{c3}(k) \tag{6}$$

in which $v_{c1}(k)$, $v_{c2}(k)$, and $v_{c3}(k)$ are the capacitor voltages. C_1, C_2, and C_3 are the capacitors of the DCI, and T_s is the sampling time. $i_{c1}(k)$, $i_{c2}(k)$, and $i_{c3}(k)$ are the capacitor currents and can be computed as [23]:

$$\begin{aligned} \mathrm{i_{c1}(k)} &= -\mathrm{i_1(k)} \\ \mathrm{i_{c2}(k)} &= -\mathrm{i_1(k)} - \mathrm{i_2(k)} \\ \mathrm{i_{c3}(k)} &= -\mathrm{i_1(k)} - \mathrm{i_2(k)} - \mathrm{i_3(k)} \end{aligned} \tag{7}$$

where

$$\begin{aligned} i_1(k) &= K_{a1}\, i_a(k) + K_{b1}\, i_b(k) + K_{c1}\, i_c(k) \\ i_2(k) &= K_{a2}\, i_a(k) + K_{b2}\, i_b(k) + K_{c2}\, i_c(k) \\ i_3(k) &= K_{a3}\, i_a(k) + K_{b3}\, i_b(k) + K_{c3}\, i_c(k) \end{aligned} \tag{8}$$

where K_{xy} $(x \in \{a, b, c\}, y \in \{1, 2, 3\})$ and is described as [23].

$$\begin{aligned} K_{x1} &= S_{x1}\, S_{x2}\, S_{x3} \\ K_{x2} &= \bar{S}_{x1}\, S_{x2}\, S_{x3} \\ K_{x3} &= \bar{S}_{x1}\, \bar{S}_{x2}\, S_{x3} \end{aligned} \tag{9}$$

in which S_x is defined in Table 1.

3. Discrete-Time Model of PMSM

In the a-b-c reference frame, the stator voltages of a three-phase PMSM can be expressed as [7]:

$$V_s = R_s\, i_s + L_s \frac{d\psi_s}{dt} \tag{10}$$

where $\mathbf{V}_s$, $\mathbf{i}_s$, and $\boldsymbol{\psi}_s$ are the stator voltage, stator current, and stator flux linkage vectors, respectively. R_s and L_s are the resistance and inductance matrices of the stator, respectively. Using Park's transformation, the stator voltage equations can be derived in the d–q rotating reference frame [7]:

$$v_{ds} = R_s i_{ds} + L_s \frac{di_{ds}}{dt} - L_s \omega_r i_{qs} \tag{11}$$

$$v_{qs} = R_s\, i_{qs} + L_s \frac{di_{qs}}{dt} + L_s\, \omega_r\, i_{ds} + \psi_m\, \omega_r \tag{12}$$

where ω_r and ψ_m are the rotor speed and rotor flux, respectively. R_s and L_s are the stator resistance and stator inductance, respectively. i_{ds} and i_{qs} are the stator d- and q-axis currents, respectively. v_{ds} and v_{qs} are the stator d- and q-axis voltages, respectively.

The electromagnetic torque T_{em} can be characterized as [7]:

$$T_{em} = \frac{3}{2}\, p\, \psi_m\, i_{qs} \tag{13}$$

where p is the PMSM pole pairs.

Utilizing the Euler forward approximation [24] and from Eqs. (11)-(12), the prediction of d-q stator currents in the (k+1)-th sampling instant can be obtained as [11]:

$$\begin{aligned} i_{ds}(k+1) = &\left(1 - \tfrac{R_s T_s}{L_s}\right) i_{ds}(k) + \\ &T_s \omega_r i_{qs}(k) + \tfrac{T_s}{L_s} v_{ds}(k) \end{aligned} \tag{14}$$

$$\begin{aligned} i_{qs}(k+1) = &\left(1 - \tfrac{R_s T_s}{L_s}\right) i_{qs}(k) - T_s \omega_r i_{ds}(k) + \\ &\tfrac{T_s}{L_s} v_{qs}(k) - \tfrac{T_s}{L_s} \psi_m \omega_r \end{aligned} \tag{15}$$

4. Model Predictive Current Control of PMSM Drive

MPCC of the PMSM drive is performed in the d-q rotating reference frame. Using Park's transformation, the stator voltages and stator currents can be converter from a-b-c stationary reference frame to d-q rotating reference frame:

$$\begin{bmatrix} v_{ds} \\ v_{qs} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{16}$$

$$\begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{17}$$

where θ is the rotor angle. Fig. 2 shows the MPCC scheme for the PMSM drive fed with a 4-level DCI. A discrete PI controller with anti-windup has been utilized as a speed regulator and generates the q-axis reference current, i^*_{qs}. MPCC is responsible for the current tracking behavior of the PMSM drive. Accordingly, the MPCC diagram predicts the future value of the stator currents. A cost function is defined to evaluate the predicted and reference values of the stator currents. All 64 possible switching combinations are taken into account. The switching state that minimizes the cost function is applied to the DCI in the next sampling instant. In this work, the delay compensation strategy is utilized to compensate the perdition error due to the practical computation burden. In the delay compensation strategy, the predictions are made for the (k+2)-th sampling instant.

The prediction of d-q stator currents in the (k+2)-th sampling instant is derived from Eqs. (14)-(15) [10]:

$$\begin{aligned} i_{ds}\,(k+2) = &\left(1 - \left(\tfrac{R_s T_s}{L_s}\right)\right) i_{ds}\,(k+1) - \\ &T_s \omega_r i_{qs} + \tfrac{T_s}{L_s} v_{ds}\,(k+1) \end{aligned} \tag{18}$$

$$\begin{aligned} i_{qs}\,(k+2) = &\left(1 - \left(\tfrac{R_s T_s}{L_s}\right)\right) i_{qs}\,(k+1) - \\ &T_s \omega_r i_{ds} + \tfrac{T_s}{L_s} v_{qs}\,(k+1) - \psi_m \omega_r \tfrac{T_s}{L_s} \end{aligned} \tag{19}$$

The overall objective function is defined as:

$$\begin{aligned} g = &\left(i_{ds}(k+2)\right)^2 + \left(i^*_{qs} - i_{qs}(k+2)\right)^2 + \\ &\hat{f}\left(i_{ds}(k+2), i_{qs}(k+2)\right) + \lambda_V g_{vc}(k+2) + \\ &\lambda_S g_{sw}(k+2) + \lambda_{CM} g_{CM}(k+2) \end{aligned} \tag{20}$$

g_{v_c} and λ_V are the objective function term and the weighting factor that adjusts the voltage balance of the capacitors, respectively. g_{v_c} is defined as [22]:

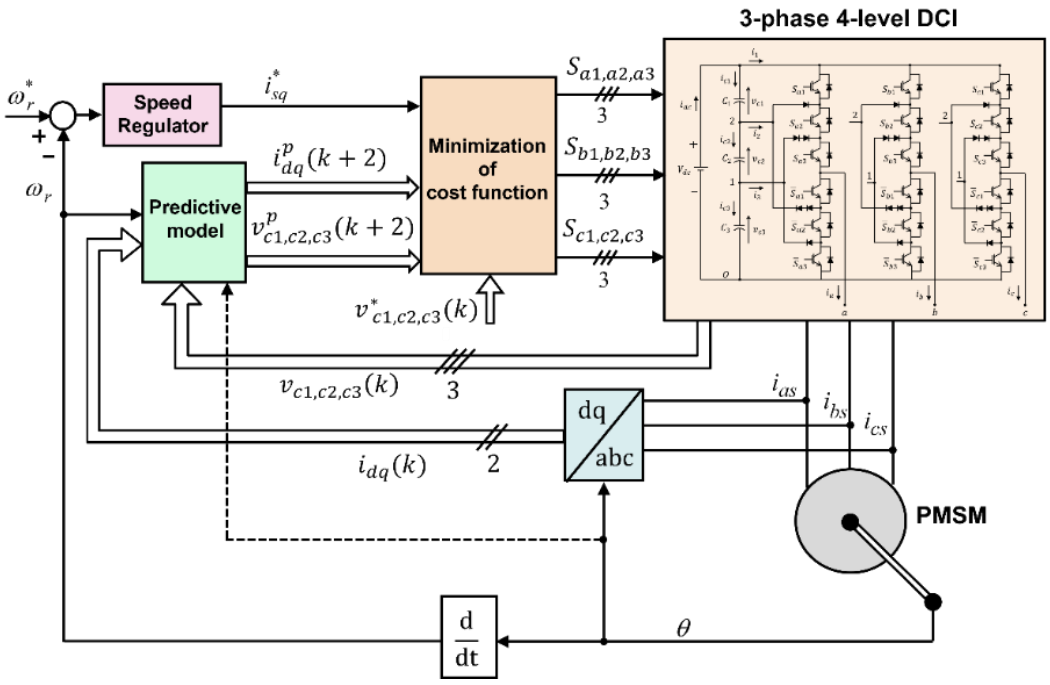

Fig. 2. MPCC of the PMSM drive fed through the 3-phase 4-level DCI.

$$g_{v_c}(k+2) = \sum_{j=1,\,2,\,3} \left(v^*_{cj} - v_{cj}(k+2)\right)^2 \tag{21}$$

where v^*_{c1}, v^*_{c2}, and v^*_{c3} are the reference voltages of the capacitors:

$$v^*_{c1} = v^*_{c2} = v^*_{c3} = \frac{V_{dc}}{3} \tag{22}$$

The capacitor voltages are predicted for the (k+2)-th sampling instant [10]:

$$\begin{aligned} v_{c1}(k+2) &= v_{c1}(k+1) + \tfrac{T_s}{C_1}\, i_{c1}(k+1) \\ v_{c2}(k+2) &= v_{c2}(k+1) + \tfrac{T_s}{C_2}\, i_{c2}(k+1) \\ v_{c3}(k+2) &= v_{c3}(k+1) + \tfrac{T_s}{C_3}\, i_{c3}(k+1) \end{aligned} \tag{23}$$

Note that $\hat{f}$ is the objective function term for the limitation of the stator current amplitude:

$$\hat{f}(i_{ds}(k+2), i_{qs}(k+2)) = \begin{cases} \infty & \text{if} |i_{ds}| > i_{\max} \text{or} |i_{qs}| > i_{\max} \\ 0 & \text{if} |i_{ds}| \le i_{\max} \text{and} |i_{qs}| \le i_{\max} \end{cases} \tag{24}$$

Moreover, g_{sw} and λ_S are the objective function term and the weighting factor related to the number of switching commutations, respectively. g_{sw} can be calculated as [22]:

$$g_{\text{sw}}(k+2) = \left(\sum_{x\in\{a,b,c\}} \sum_{j=1}^{3} |S_{xj}(k+2) - S_{xj}(k+1)| \right)^2 \tag{25}$$

In addition, g_{CM} and λ_{CM} are the objective function term and the weighting factor related to the CM voltage, respectively. g_{CM} can be calculated using Eq. (3):

$$g_{\text{CM}}(k+2) = \left(v_{\text{nO}}(k+2)\right)^2 \tag{26}$$

Fig. 3 depicts the flowchart of the MPCC for the PMSM drive fed with a 4-level DCI with delay compensation.

First, the present value of the load currents, capacitor voltages, motor speed, and angular frequency are measured. Next, the capacitor voltages and the d-q stator currents are predicted in the (k+1)-th sampling instant. Then, for all 64 possible switching combinations, the capacitor voltages and the d-q stator currents are predicted in the (k+2)-th sampling instant. Accordingly, the cost function is computed and evaluated. The switching state that minimizes the cost function is applied to the DCI in the next sampling instant.

5. Results and Discussion

To validate the merit of the proposed strategy, the MPCC of the PMSM drive supplied with a 4-level DCI has been simulated by Matlab/Simulink. The simulation parameters are listed in Table 2.

Table 2. Simulation parameters.

Parameter	Value	Parameter	Value
V_{dc}	520 [V]	B	0.001
C_1, C_2, C_3	2200 [μF]	Stator flux	0.125 [Wb]
R_s	0.3 [Ω]	$i_{q,nom}$	20 [A]
L_s	8.2 [mH]	$i_{d,nom}$	1 [A]
L_d	6.2 [mH]	time step	5 [μsec]
L_q	10.2 [mH]	K_i	5
p	3	PI gain K_p	1
J	0.004 [Kg·m^2]	T_{sw}	0.002

Fig. 4 shows the simulation results of the PMSM drive supplied with 4-level DCI with MPCC strategy. In Figs. 4 (a)-(d), actual and reference speed, electromagnetic and load torque, actual and reference q-axis current, and stator currents have been presented. The reference speed is changed from 1000 rpm to -1000 rpm at t=0.15 sec. The PMSM starts at no-load. A 5 Nm torque is applied to the PMSM drive at t=0.3 sec. The sampling time is considered as T_s=50 μs. The weighting factor λ_V is set to 0.1. The weighting factors λ_S and λ_{CM} are set to zero. From Fig. 4 (a), we can obviously observe that the motor speed has a fast dynamic and

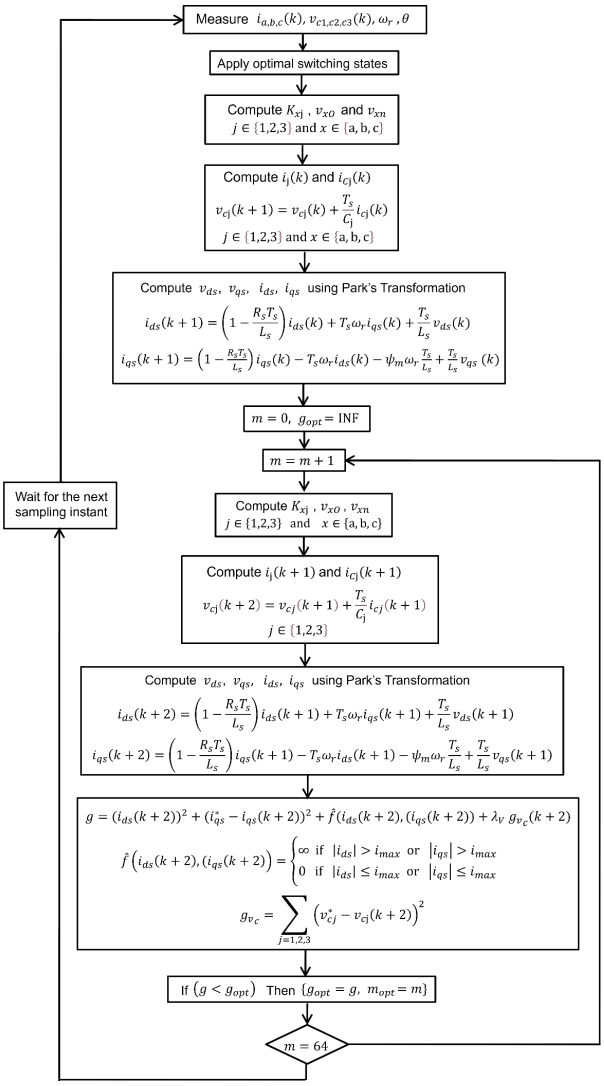

Fig. 3. Flowchart of the MPCC of PMSM drive fed through a 4-level DCI.

is not affected by the load change. By observing Figs. 4 (b)-(c), it is clear that the electromagnetic torque and q-axis current track their references and correspond to the motor start, speed reverse, and load change conditions. As depicted in Fig. 4 (d), the stator currents correspond with loading conditions. Moreover, the distortion of the stator currents is low. Fig. 5 illustrates the simulation results of the PMSM drive fed with 2-level VSI under the same operating conditions as in Fig. 4. It is obvious that the total harmonic distortion (THD) of the stator current and the torque ripple is lower in the PMSM drive with 4-level DCI than in 2-level VSI. The current THD is reduced from 8.61% in 2-level VSI to 4.59% in 4-level DCI.

Table 3. Comparison of the PMSM drive performance with the 4-level DCI and 2-level VSI.

Parameter	2-level VSI	4-level DCI
Rise Time [sec]	0.042	0.042
Current THD [%]	8.61	4.59
Torque Ripple [Nm]	1.2	0.32
Current Ripple [A]	1.9	0.58

Table 3 compares the performance of MPCC of PMSM drive with 4-level DCI and 2-level VSI. It is visible that in the 4-level

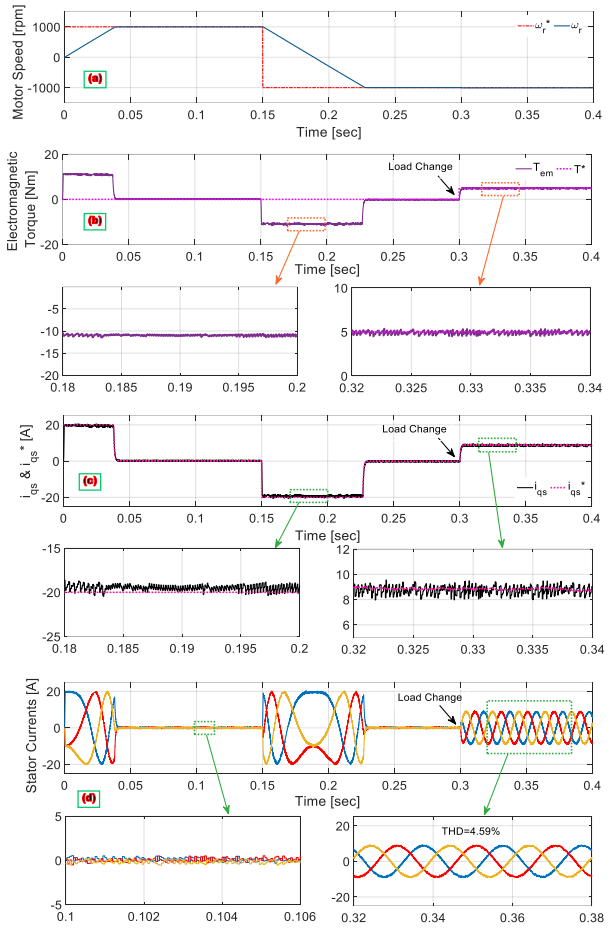

Fig. 4. MPCC of PMSM drive with 4-level DCI: (a) Motor speed; (b) electromagnetic torque; (c) q-axis current; (d) stator currents.

DCI, the torque ripple, current ripple, and current THD are lower than the 2-level VSI.

Fig. 6 exhibits the stator currents and DC capacitor voltages of the 4-level DCI during the motor start, speed reversal, and load change conditions. The PMSM starts at no-load. A 5 Nm torque is applied to the PMSM drive at t=0.1 sec. Other simulation parameters are identical to the ones in Fig. 4. Results confirm that the DC capacitor voltages (v_{C1}, v_{C2}, v_{C3}) are balanced and they are not affected by the speed reversal and load change conditions. Moreover, the voltage ripple is higher in the transitions and reduces in the steady-state conditions.

Next, the impacts of choosing different weighting factors in the MPCC objective function in the PMSM drive are studied. The corresponding results are illustrated in Figs. 7-9. The reference speed is 1000 rpm and a 5 Nm load is applied to the PMSM. The weighting factors are changed in the steady-state condition of the machine. The sampling time T_s is 80 μsec.

Fig. 7 depicts the effect of λ_V on the performance of the PMSM drive with 4-level DCI. The weighting factors λ_S and λ_{CM} are set to zero. λ_V is changed from 10 to zero at t=0.2 sec and from zero to 10 at t=0.25 sec. Figs. 7 (a)-(f) present the DC capacitor voltages, actual and reference speed, electromagnetic torque, stator currents, gate pulse S_{a1}, and CM voltage, respectively. It is visible that when λ_V is not considered in the objective function, severe unbalance can happen in the PMSM drive (according to Fig. 7 (a)). Consequently, to maintain the voltage balance of the capacitors in the DCI and ensure the correct performance of the drive, it is necessary to include λ_V in the objective function of MPCC. From Figs. 7 (b)-(d), we can clearly find that the voltage unbalance

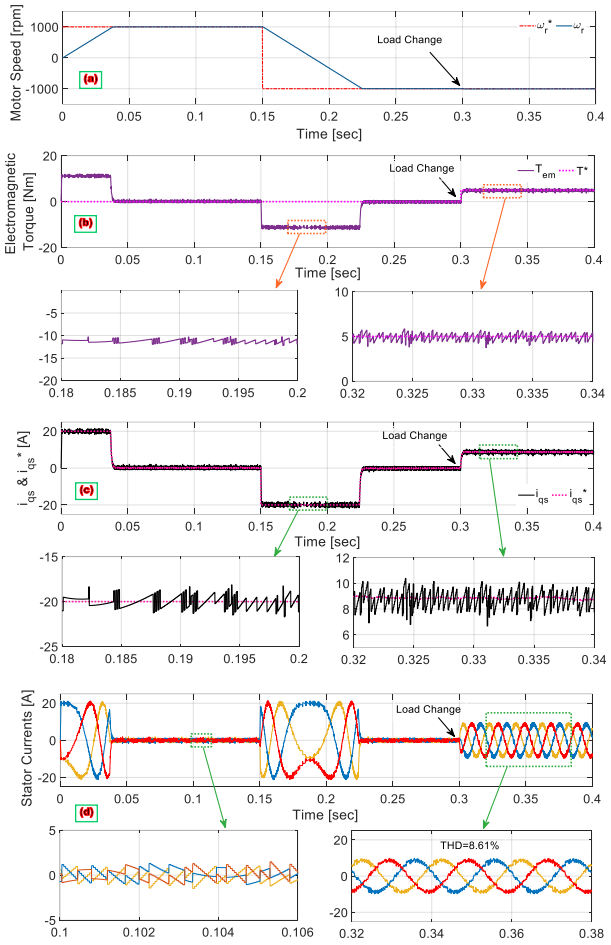

Fig. 5. MPCC of PMSM drive with 2-level VSI: (a) motor speed; (b) electromagnetic torque; (c) q-axis current; (d) stator currents.

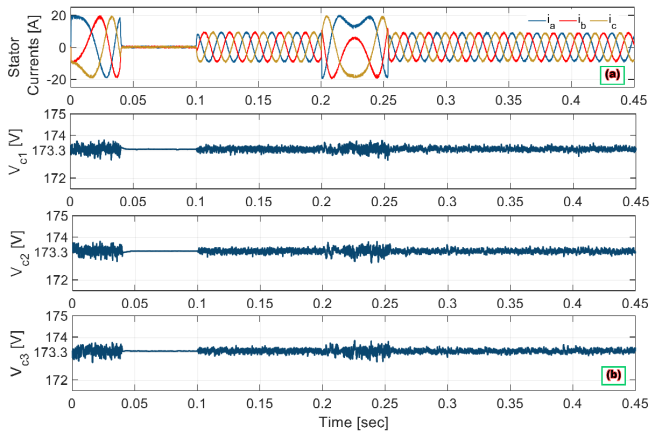

Fig. 6. The effect of starting, load change, and speed reversal in PMSM drive with 4-level DCI: (a) stator currents; (b) DC capacitor voltages.

leads to extreme variations in the electromagnetic torque and stator currents while the motor speed is not affected much. Moreover, as shown in Figs. 7 (e)-(f), the number of switching commutations and the CM voltage are not controlled since they are not included in the objective function.

Fig. 8 illustrates the effect of λ_S on the performance of the PMSM drive with 4-level DCI. The value of λ_S is changed

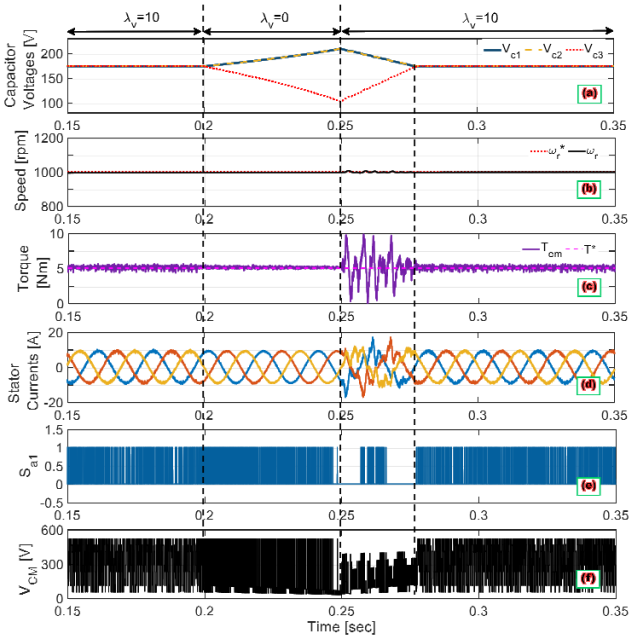

Fig. 7. Effect of λ_V on the performance of the PMSM drive with 4-level DCI: (a) gate pulse S_{a1}; (b) DC capacitor voltages; (c) actual and reference speed; (d) torque; (e) stator currents; (f) CM voltage.

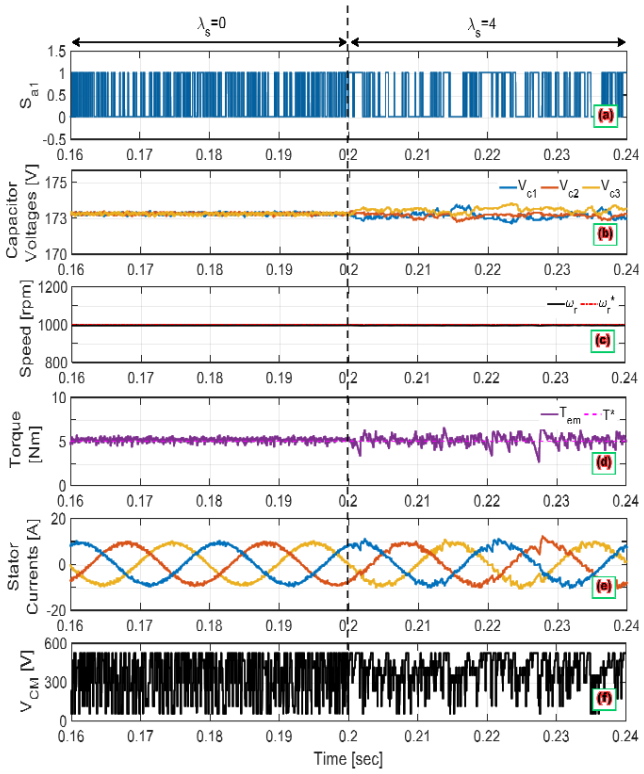

Fig. 8. Effect of λ_s on the performance of the PMSM drive with 4-level DCI: (a) gate pulse S_{a1}; (b) DC capacitor voltages; (c) actual and reference speed; (d) torque; (e) stator currents; (f) CM voltage.

from zero to 4 at t=0.2 sec. Herein, λ_V is set to 10 and λ_{CM} is set to zero. Figs. 8 (a)-(f) present the gate pulse S_{a1}, DC capacitor voltages (v_{C1}, v_{C2}, v_{C3}), actual and reference speed, electromagnetic torque, stator currents, and CM voltage, respectively. From Fig. 8 (a), we can observe that it is possible

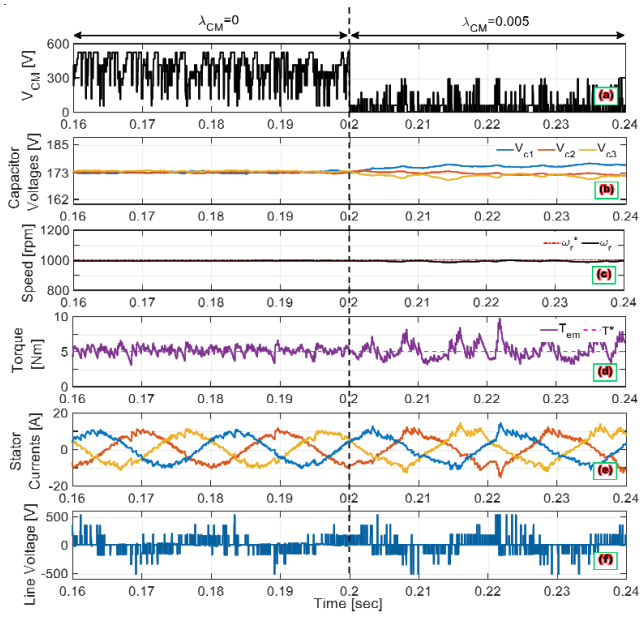

Fig. 9. Effect of λ_{CM} on the performance of the PMSM drive with 4-level DCI: (a) CM voltage; (b) DC capacitor voltages; (c) speed and reference speed; (d) electromagnetic torque; (e) stator currents; (f) line voltage V_{ab}.

to decrease the switching frequency by including the number of switching commutations in the objective function of MPCC using the weighting factor λ_S. According to Figs. 8 (b)-(e), increasing the value of λ_S leads to an increase in voltage unbalance, torque ripple, and current distortion. Nevertheless, by increasing the value of λ_S, the motor speed can track the reference as before. The CM voltage is high since it is not included in the objective function (as shown in Fig. 8 (f)).

Fig. 9 represents the effect of λ_{CM} on the performance of the PMSM drive with 4-level DCI. The value of λ_{CM} is changed from zero to 0.0006 at t=0.2 sec. λ_V is set to 10 and λ_S is set to 4. Figs. 9 (a)-(f) display the CM voltage (V_{CM}), DC capacitor voltages (v_{C1}, v_{C2}, v_{C3}), actual and reference speed, electromagnetic torque, stator currents, and line-to-line voltage (V_{ab}), respectively. From Fig. 9 (a), it is visible that by including the CM voltage in the objective function of MPCC using the weighting factor λ_{CM}, the CM voltage can be significantly reduced. In contrast, reducing the CM voltage leads to higher voltage unbalance, torque ripple, and distortion of current and voltage (see Figs. 9 (b)-(f)). Moreover, by increasing the value of λ_{CM}, the motor speed can track the reference with small fluctuations.

To check the validation of simulation results, the performance of the PMSM drive fed through the 2-level VSI can be compared with the results given in the literature [24]. Fig. 10 presents the results of the PMSM drive fed with the 2-level DCI given in [24] and the present work under similar simulating conditions. As it is clear, the results are compatible.

6. Conclusion

This paper concentrates on the MPCC of PMSM drive supplied with 4-level DCI. The suggested MPCC scheme reveals excellent dynamic behavior of the PMSM drive while ensuring the DC-link capacitor voltage balance in the 4-level DCI during the motor start, speed reversal, and load change conditions. To attain a more comprehensive evaluation, the dynamic behavior of the understudy system is compared to the MPCC of the PMSM drive with the conventional 2-level VSI. Results manifest that the PMSM drive with 4-level DCI has lower current THD and torque ripple than the PMSM drive with 2-level VSI. The current THD is reduced from 8.61% in 2-level VSI to 4.59% in 4-level DCI. The torque ripple

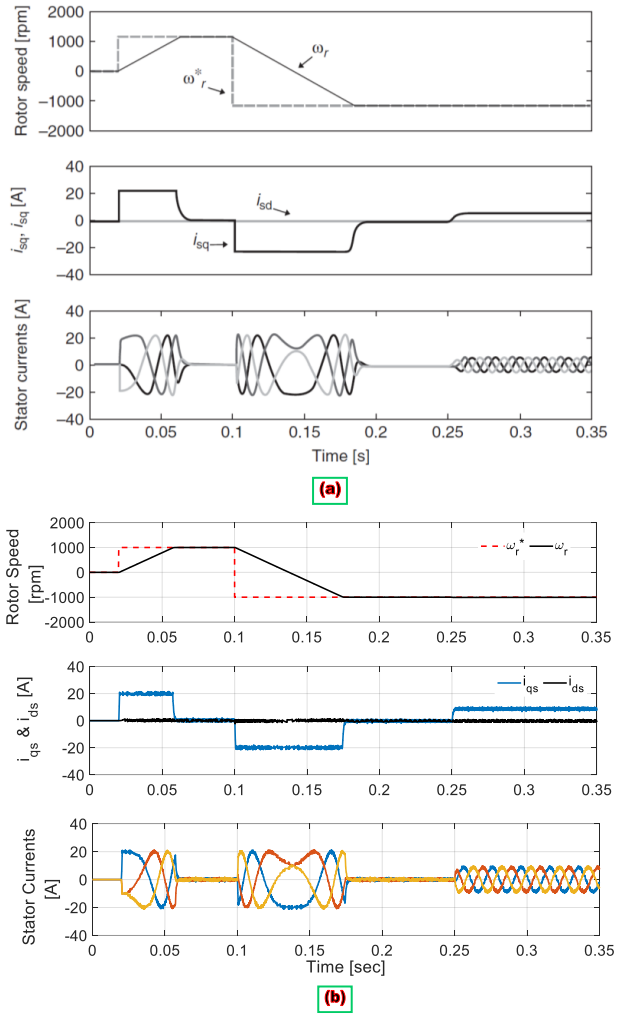

Fig. 10. Simulation results of the PMSM drive fed with the 2-level DCI: (a) results from [24]; (b) results from the present work.

is reduced from 1.2 Nm in 2-level VSI to 0.32 Nm in 4-level DCI. To yield a more valuable assessment, the switching frequency and common mode (CM) voltage have been included in the objective function of the MPCC scheme. The impact of different values of weighting factors is investigated on the performance of PMSM drive with 4-level DCI. According to the results, to ensure the correct performance of the drive, it is necessary to maintain the voltage balance of the capacitors in the DCI by considering λ_V in the objective function of the MPCC. The voltage unbalance causes extreme large ripples in the electromagnetic torque and stator currents. Besides, it is possible to control the switching frequency by tuning the weighting factor λ_S in the objective function of the MPCC. Nevertheless, increasing the value of λ_S enhances the voltage unbalance, torque ripple, and current distortion. Additionally, by choosing the suitable weighting factor λ_{CM} in the objective function of the MPCC, the CM voltage can be significantly reduced. According to the results, mitigating the CM voltage results in higher voltage unbalance, torque ripple, and current distortion and causes small fluctuations in the motor speed. Consequently, it is not possible to meet all objectives and simultaneously maintain the quality of drive performance. Future works can concentrate on optimizing the weighting factors in the MPCC objective function for the PMSM drive with 4-level DCI according to the aim and application.

REFERENCES

[1] M. Megrini, A. Gaga, and Y. Mehdaoui, "Review of electric vehicle traction motors, control systems, and various implementation cards," *J. Oper. Autom. Power Eng.*, vol. 13, no. 3, pp. 238–247, 2025.

[2] X. Sun, N. Xu, M. Yao, F. Cai, and M. Wu, "Efficient feedback linearization control for an ipmsm of evs based on improved firefly algorithm," *ISA Trans.*, vol. 134, pp. 431–441, 2023.

[3] V. Naeini and N. Sadeghi, "Optimum design of the outer rotor brushless dc permanent magnet motor with minimum torque ripples," *J. Oper. Autom. Power Eng.*, 2024.

[4] N. Rostami, A. A. Kadhim, and M. B. Bannae-Sharifian, "Cogging force reduction in pmlsms using segmented magnets," *J. Oper. Autom. Power Eng.*, pp. 206–211, 2025.

[5] K. Kakouche, A. Oubelaid, S. Mezani, D. Rekioua, and T. Rekioua, "Different control techniques of permanent magnet synchronous motor with fuzzy logic for electric vehicles: Analysis, modelling, and comparison," *Energies*, vol. 16, no. 7, p. 3116, 2023.

[6] A. Shinohara, Y. Inoue, S. Morimoto, and M. Sanada, "Maximum torque per ampere control in stator flux linkage synchronous frame for dtc-based pmsm drives without using q-axis inductance," *IEEE Trans. Ind. Appl.*, vol. 53, no. 4, pp. 3663–3671, 2017.

[7] J. Hu, H. Lu, B. Zheng, and Y. Zhang, "Predictive control of permanent magnet synchronous motor based on super-twisting sliding mode," *Energy Sci. Eng.*, vol. 11, pp. 3173–3184, 2023.

[8] X. Sun, J. Cao, G. Lei, Y. Guo, and J. Zhu, "A composite sliding mode control for spmsm drives based on a new hybrid reaching law with disturbance compensation," *IEEE Trans. Transp. Electrific.*, vol. 7, no. 3, pp. 1427–1436, 2021.

[9] M. H. Mousavi, M. E. Karami, and M. Ahmadi, "Robust speed controller design for permanent magnet synchronous motor based on gain-scheduled control method via lmi approach," *SN Appl. Sci.*, vol. 2, no. 1699, 2020.

[10] J. Peng and M. Yao, "Overview of predictive control technology for permanent magnet synchronous motor system," *Appl. Sci.*, vol. 13, no. 10, p. 6255, 2023.

[11] X. Sun, M. Wu, G. Lei, Y. Guo, and J. Zhu, "An improved model predictive current control for pmsm drives based on current track circle," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 3782–3793, 2021.

[12] O. Sandre-Hernandez, J. Rangel-Magdaleno, and R. M. aporal, "Modified model predictive torque control for a pmsm-drive with torque ripple minimization," *IET Power Electron.*, vol. 12, pp. 1033–1042, 2019.

[13] M. Liu, K. W. Chan, J. Hu, W. Xu, and J. Rodriguez, "Model predictive direct speed control with torque oscillation reduction for pmsm drives," *IEEE Trans. Ind. Informat.*, vol. 15, no. 9, pp. 4944–4956, 2019.

[14] M. Alemi-Rostami and G. Rezazadeh, "Selective harmonic elimination of a multilevel voltage source inverter using whale optimization algorithm," *Int. J. Eng.*, vol. 34, no. 8, pp. 1898–1904, 2021.

[15] A. Rajabloo, H. Lesani, S. Y. Mousazadeh Mousavi, and S. B. Mozafari, "Second order sliding mode control of three phase neutral point clamped inverter in stationary frame," *Int. J. Eng.*, vol. 37, no. 8, pp. 1466–1474, 2024.

[16] P. Hamedani and M. Changizian, "A new hybrid predictive-pwm control for flying capacitor multilevel inverter," *J. Electr. Comput. Eng. Innov.*, vol. 12, no. 2, pp. 353–362, 2024.

[17] P. Hamedani and A. Shoulaei, "Utilization of chb multilevel inverter for harmonic reduction in fuzzy logic controlled multiphase lim drives," *J. Electr. Comput. Eng. Innov.*, vol. 8, no. 1, pp. 19–30, 2020.

[18] V. Yaramasu, A. Dekka, M. Rivera, S. Kouro, and J. Rodriguez, *Multilevel Inverters: Control Methods and Advanced Power Electronic Applications*. Academic Press, 2021.

[19] J. G. Ordonez, D. Limon, and F. Gordillo, "Multirate predictive control for diode clamped inverters with data-based learning implementation," *IFAC-PapersOnLine*, vol. 56, no. 2, pp. 6388–6393, 2023.

[20] R. Atif *et al.*, "Simplified model predictive current control of four-level nested neutral point clamped converter," *Sustainability*, vol. 15, no. 2, p. 955, 2023.

[21] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: Advances and trends," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 935–947, 2017.

[22] P. Hamedani, "Multistep model predictive control of diode-clamped multilevel inverter," *J. Electr. Comput. Eng. Innov.*, vol. 13, no. 1, pp. 117–128, 2025.

[23] E. Kabalcı, *Multilevel Inverters Control Methods and Advanced Power Electronic Applications*. Elsevier, 2021.

[24] J. Rodriguez and P. Cortes, *Predictive control of power converters and electrical drives*. John Wiley Sons, 2012.