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Research Paper

Study on a High Step-Up DC-DC Converter Based on Built-in Transformer for Photovoltaic Applications

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Abstract— *This paper presents and investigates a high step-up non-isolated DC-DC converter with an integrated transformer for photovoltaic applications. Unlike most non-isolated DC-DC converters that rely on coupled inductors, the proposed converter uses an integrated transformer combined with a modified voltage multiplier cell to achieve a high voltage conversion ratio. Additionally, a passive voltage clamp is employed to reduce voltage stress across the switch and recycle energy stored in the leakage inductance of the integrated transformer. This approach allows for the use of a switch with low on-resistance (RDS-ON). Other notable advantages of the proposed structure include continuous input current with low ripple and a shared common ground between the input source, switch, and load, making it an attractive solution for photovoltaic-based systems. The relatively low voltage across the diodes also mitigates reverse recovery issues. The proposed topology is derived from the SEPIC converter and is studied in detail. Furthermore, the proposed configuration is compared to various previously presented DC-DC converters to demonstrate its advantages. Finally, a 250-W laboratory prototype is developed, and experimental results are presented. These results validate the theoretical analysis and confirm the functionality and feasibility of the proposed converter.*

Keywords—Continuous input current, built-in transformer, high gain, non-isolated converter, SEPIC-based DC-DC converter.

1. INTRODUCTION

Fossil fuels are easily accessible, cost-effective, and have a high energy density. However, they are non-renewable resources, and the greenhouse gas emissions produced by burning fossil fuels are a primary contributor to global warming. As a result, the global shift towards renewable energy sources (RES) and a reduction in fossil fuel dependence are steadily increasing. Among all RES, the photovoltaic (PV) industry is witnessing unprecedented growth, driven by advances in PV technology and a decrease in installation costs. The unique characteristics of PV systems, such as their long lifespan, high reliability, low maintenance costs, minimal noise pollution, environmental friendliness, and zero carbon emissions, position them as a promising alternative to fossil fuels. However, the initial installation cost remains high, and the output voltage of PV panels is relatively low, requiring boosting before it can be connected to grid-tied inverters and loads [1], [2]. The literature addresses the technical design criteria of DC-DC structures for PV applications [3], [4]. High voltage gain and continuous input current with minimum ripple from the PV source are the most imperative ones. Moreover, higher efficiency and lower cost, size, and weight are the other required standards to be considered when drafting DC-DC topologies for PV systems [5], [6]. Compared to isolated DC-DC structures, non-isolated DC-DC converters are preferred in high-voltage applications and where galvanic isolation is unnecessary due to their low cost, size, and voltage stresses on semiconductors [7], [8]. Non-isolated structures are derived from either conventional structures such as buck, boost, and buck-boost converters or two-stage topologies like single-ended primary-inductor converter (SEPIC), Ćuk, and Zeta converters [9], [10]. Researchers have employed various methods, including switched capacitors and inductors, Z-source, voltage lift, and voltage multiplier (VM), to increase the voltage conversion ratios of DC-DC structures to an acceptable level [11, 12]. Another technique that has been widely used to increase voltage gain in DC-DC structures is utilizing a coupled inductor (CI) along with the mentioned methods [13–15]. In [16], [17], and [18], three different high step-up CI-based structures have been presented. Designed converters have utilized the switched capacitor technique and different VM cells to raise the output voltage level. However, they all suffer from high input current ripples and are unsuitable for PV-based systems. From [19–22], authors have developed different DC-DC converters based on Z-source and quasi Z-source. In all of them, the duty ratio could not exceed 0.5. Hence, they suffer from duty ratio limitation. Furthermore, in [19], the input current of the presented structure is discontinuous and could not be suitable for PV applications. Meanwhile, the input current ripple is high in the structure presented in [20]. Converters studied in [23], [24], and [25], have employed VM cells along with CI to achieve high voltage conversion ratios. Proposed structures have reached high efficiency by utilizing zero voltage switching (ZVS) and zero current switching (ZCS). Continuous input current with low ripple are other merits of presented converters. However, considering the number of utilized components, the achieved voltage gain is not satisfying. Another method to increase voltage gain and efficiency of high step-up DC-DC converters is utilizing a built-in transformer (BIT) [26], [27]. As the average current value flowing through windings of BIT is zero, core magnetic

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flux is balanced and its saturation capability is improved [28]. Moreover, in comparison with CI-based structures, core size, and conduction losses are reduced in BIT-based structures. In [29], another high step-up non-isolated DC-DC converter has been presented. The converter is based on the voltage-switching cell and has a continuous input current. However, regarding the number of components, voltage gain is still low and needs to be boosted for PV applications. Authors have designed another structure in [30]. The converter is based on the VM cell and the CI. The structure has a simple structure. However, the voltage conversion ratio is low and the input current ripple is high for PV-based systems. This paper presents and studies a novel non-isolated BIT-based DC-DC converter for PV applications. The proposed topology is drafted from the SEPIC structure and benefits from various features, including continuous input current with very low ripple and high voltage conversion ratio, making the designed structure desirable for PV-based systems. Draining continuous and low-ripple input current is achieved by utilizing an input inductor in series with the voltage source. Unlike most CI-based DC-DC structures, the designed converter utilizes a BIT and an improved VM cell to gain high voltage. Compared to conventional VM cells in which capacitors are charged only by the secondary side of CI, capacitors of the proposed VM module are charged by both sides of the BIT. Meanwhile, a passive voltage clamp is utilized to recycle energy stored in the leakage inductance of the BIT and clamp voltage stress on the switch. Hence, a low on-resistance switch can be used that reduces cost and conduction losses and increases efficiency. Meanwhile, shared common ground between input, output, and switch results in reduced common noise, improved gate driving, and enhanced overall stability and performance of the converter. Thanks to the relatively low voltage across diodes, their reverse recovery problems are alleviated. In the following, the operating principles of the proposed structure along with relative analysis are described.

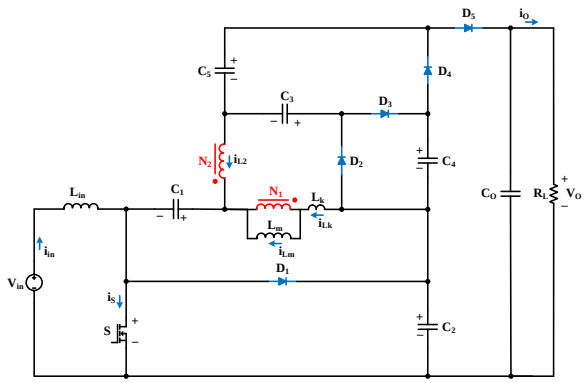


Fig. 1. Equivalent power circuit of the proposed DC-DC converter.

2. OPERATING PRINCIPLES AND STEADY STATE ANALYSIS OF THE PROPOSED CONVERTER

The equivalent circuit of the proposed high step-up DC-DC converter is depicted in Fig. 1. Unlike most high step-up DC-DC structures based on the CI, the presented structure is based on BIT which provides lower core volume and conduction losses. As illustrated in this Fig., the structure comprises a switch S, an input inductor L_in, a two-winding BIT with winding turn ratios of n, five diodes D_1-D_5, and six capacitors including C_1-C_5 and output capacitor C_O. The diode D_1 and the capacitor C_2 form a passive voltage clamp to reduce the voltage stress on switch S and recycle the stored energy in the leakage inductance of the BIT. Furthermore, in this Fig., L_k and L_m represent leakage and magnetizing inductances of the BIT, respectively. Meanwhile, N_1 and N_2 are the primary and the secondary winding turn numbers of the BIT.

The following assumptions are taken into account to simplify the steady-state analysis of the proposed converter.

1) All inductors and capacitors are large enough. Hence, there is no ripple in their currents and voltages, respectively.

2) Semiconductors are ideal without parasitic elements and non-ideal components.

A) CCM operation

The continuous conduction mode (CCM) operation of the presented DC-DC converter includes five time intervals in one switching cycle. Moreover, the current flow paths and main waveforms of operating modes are depicted in Fig. 2 and Fig. 3, respectively. These modes are described in the following.

Mode I [t_0–t_1]: The first mode begins by turning switch S on at $t = t_0$. The leakage inductance of the BIT (L_k) decreases the slope of the current flowing through the switch S ($\mathrm{d}i_S/\mathrm{d}t$) at the turn-on instant. During this mode, diodes D_3 and D_5 are remained on. While, diodes D_1, D_2, and D_4 are reverse-biased. The input voltage source charges the input inductor L_{in}. The energies of the BIT and capacitors are transferred to the output capacitor C_O and the load. Thanks to the low value of the leakage inductance of the BIT and the high voltage across it, the duration of this mode is too short. This mode ends when the current flowing through the leakage inductance of the BIT reaches the current flowing through magnetizing inductance of the BIT ($i_{L_k} = i_{L_m}$) at $t = t_1$. Fig. 2-(a) shows the relative current-flow path of this mode.

Mode II [t_1–t_2]: At $t = t_1$, the current flowing through the secondary side of the BIT reaches zero. Hence, diodes D_3 and D_5 turn off and D_2 and D_4 are forward-biased. Switch S is still conducting. However, diode D_1 remains off during this mode. Like Mode I, input inductor L_{in} is charged by the input voltage source through the switch S. Capacitor C_3 is charged by both the primary and secondary sides of the BIT. Meanwhile, energy stored in capacitor C_4 along with both primary and secondary sides of the BIT charges the capacitor C_5. In this mode, the output capacitor C_O supplies the load. Fig. 2-(b) shows the relative current-flow path of this mode. The following equations could be obtained for currents of capacitors in this mode.

$$i_{C1} = -i_{C2} = i_{Lm} + (n+1)\,(i_{D2} + i_{D4}) \tag{1}$$

$$i_{C3} = i_{D2} \tag{2}$$

$$i_{C5} = -i_{C4} = i_{D4} \tag{3}$$

Applying KVL and KCL laws in the circuit yields to:

$$i_{L1} = i_{Lk} - i_{Lm} = n i_{L2} = n\,(i_{D2} + i_{D4}) \tag{4}$$

$$v_{Lin} = V_{in} \tag{5}$$

$$v_{Lm} = V_{C2} - V_{C1} - V_{Lk}^{II} \tag{6}$$

$$V_{C5} = V_{C3} + V_{C4} \tag{7}$$

$$V_{C3} = (n+1)\,(V_{C2} - V_{C1}) - n V_{Lk}^{II} \tag{8}$$

where $V_{L_k}^{\mathrm{II}}$ represents the voltage of the leakage inductance L_k in Mode II and could be given by:

$$V_{Lk}^{II} = \frac{i_{Lk(t2)} - i_{Lk(t1)}}{DT_s} L_k \tag{9}$$

$$i_{LK} = i_{Lm} + n\left(i_{D2} + i_{D4}\right) \tag{10}$$

Mode III $[t_2 - t_3]$: This mode starts when switch S is turned off at $t = t_2$. Clamp diode D_1 is forward-biased at the turn-off instant of switch S. Therefore, the stored energy in input inductor L_{in} and the voltage source charge capacitor C_2 through clamp diode D_1. Meanwhile, the voltage across switch S is clamped to the voltage of capacitor C_2. During this mode, diodes D_2 and D_4 are still on. However, diodes D_3 and D_5 remain off. Like the previous mode, capacitor C_3 is charged by both the primary and secondary sides of the BIT. Meanwhile, energy stored in capacitor C_4 and both primary and secondary sides of the BIT charge the capacitor C_5. Moreover, the output capacitor supplies the load. The voltage across the secondary side of the BIT is negative. Hence, leakage inductance L_k is demagnetized. As the leakage inductance of the BIT has a low value, like the first mode, the duration of this mode is too short. Fig. 2-(c) shows the relative current-flow path of this mode. Currents flowing through diodes can be obtained as follows:

$$i_{D1} = i_{in} + i_{Lk} + i_{L2} \tag{11}$$

$$i_{D2} + i_{D4} = i_{L2} \tag{12}$$

where i_{L_2} is the current flowing through the secondary side of the BIT and could be formulated as follows:

$$i_{L2} = \frac{i_{Lm} - i_{Lk}}{n} \tag{13}$$

Mode IV $[t_3 - t_4]$: At $t = t_3$, the current flowing through the secondary side of the BIT reaches zero. As a consequence, diodes D_2 and D_4 turn off, and diodes D_3 and D_5 turn on. During this mode, clamp diode D_1 remains on, while switch S is still off. Like the previous mode, recycling of the energy stored in the leakage inductance of the BIT continues. Meanwhile, the input voltage source and inductor L_{in} charge capacitor C_2. Capacitor C_3, along with the primary and secondary sides of the BIT, charges capacitor C_4. Meanwhile, energy stored in capacitor C_1 is transferred to the BIT via clamp diode D_1. Fig. 2-(d) shows the relative current-flow path of this mode. The following equations could be given for currents of capacitors.

$$i_{C1} = i_{D1} - i_{in} \tag{14}$$

$$i_{C4} = -i_{C3} = i_{D3} \tag{15}$$

$$i_{C5} = -i_{D5} = -\left(i_{CO} + I_O\right) = i_{C2} - i_{in} \tag{16}$$

Applying KCL law in the circuit yields:

$$i_{D1} = i_{in} + i_{Lm} - (n+1)\left(i_{D3} + i_{D5}\right) \tag{17}$$

By applying KVL law in the circuit, the following equations could be obtained.

$$V_{Lin} = V_{in} - V_{C2} \tag{18}$$

$$V_{Lm} = -V_{C1} - V_{Lk}^{IV} \tag{19}$$

$$V_{C4} = V_{C3} + (n+1)\, V_{C1} + nV_{Lk}^{IV} \tag{20}$$

$$V_O = V_{C5} + V_{C4} - V_{C3} + V_{C2} \tag{21}$$

Where $V_{L_k}^{\mathrm{IV}}$ represents voltage across leakage inductance of the BIT in mode IV. This voltage could be calculated from:

$$V_{Lk}^{IV} = \frac{i_{Lk(t4)} - i_{Lk(t3)}}{d_4 T_s} L_k \tag{22}$$

Where d_4 and i_{Lk} are the duration of mode IV and current flowing through the leakage inductance of the BIT during this mode, respectively. This current could be obtained as follows:

$$i_{LK} = i_{Lm} - n\left(i_{D3} + i_{D5}\right) \tag{23}$$

Mode V $[t_4 - t_5]$: The last mode begins when clamp diode D_1 turns off under the ZCS condition. Switch S and diodes D_2 and D_4 are in the off-state as well. However, diodes D_3 and D_5 are forward-biased. Capacitor C_4 is charged by both the primary and secondary sides of the BIT and capacitor C_3. Meanwhile, energy stored in input inductor L_{in} and the BIT, along with the voltage source, supply the output capacitor C_O and the load. Fig. 2-(e) shows the relative current-flow path of this mode. Assuming that currents flowing through input inductor L_{in} and the magnetizing inductance of the BIT are ripple-free, the slopes of the currents flowing through the leakage inductance of the BIT along with diodes D_3 and D_5 are almost zero. Hence, during this mode, the voltage across the leakage inductance of the BIT is zero. Applying KVL in the circuit yields:

$$V_{Lin} = V_{in} - V_{C2} \tag{24}$$

$$V_{Lm} = -V_{C1} = \frac{V_{C3} - V_{C4}}{n+1} \tag{25}$$

Assuming that capacitors are large enough and their currents are ripple-free, currents flowing through diodes D_3 and D_5 are equal and could be formulated as:

$$i_{D3} = i_{D5} = \frac{i_{L2}}{2} \tag{26}$$

Where i_{L2} is the current flowing through the secondary side of the BIT and could be obtained as follows:

$$i_{L2} = -\frac{i_{in} + i_{Lm}}{n+1} \tag{27}$$

Short time intervals (modes I and III) could be ignored to simplify the steady-state analysis of the presented topology. Applying volt-second balance principles on inductors yields to:

$$\langle v_{Lm} \rangle = 0 \Rightarrow V_{C1} = \frac{D}{1-D} V_{in} - DV_{Lk}^{II} - d_4 V_{Lk}^{IV} \tag{28}$$

$$\langle v_{Lin} \rangle = 0 \Rightarrow V_{C2} = \frac{V_{in}}{1-D} \tag{29}$$

$$\langle v_{Lk} \rangle = 0 \Rightarrow V_{LK}^{IV} = -\frac{D}{d_4} V_{Lk}^{II} \tag{30}$$

Supposing that the BIT is ideal and its leakage inductance L_k is ignorable, by substituting Eqs. (7), (8), (20), (28), and (29) into Eq. (21), the ideal voltage gain of the proposed BIT-based DC-DC converter could be formulated as:

$$M = \frac{V_O}{V_{in}} = \frac{I_{in}}{I_O} = \frac{3+2n}{1-D} \tag{31}$$

To achieve the real voltage conversion ratio of the proposed structure, the duration of the fourth mode D_4, along with voltages across the leakage inductance of the BIT in modes II and IV, should be calculated. By applying capacitor-charge balance principles on capacitors, it can be proved that the average currents flowing through all diodes are equal to the output current I_O. Assuming that input and output currents and the current flowing through the magnetizing inductance of the BIT are ripple-free, the maximum current flowing through diodes D_2 and D_4 could be formulated as follows:

$$\langle i_{D2} \rangle = \langle i_{D4} \rangle = I_O \Rightarrow i_{D2,peak} = i_{D4,peak} = \frac{2I_O}{D} \tag{32}$$

Hence, the voltage across the leakage inductance of the BIT in mode II could be formulated as follows:

$$V_{Lk}^{II} = \frac{4nQ}{D^2} V_O, Q = \frac{f_S L_k}{R_L} \tag{33}$$

Where f_s and R_L are the switching frequency of switch S and the load, respectively. Applying amp-second balance principals on capacitor C_1, the average current flowing through the magnetizing inductance of the BIT could be calculated as:

$$\begin{array}{l} \langle i_{C1} \rangle = 0 \Rightarrow 2\,(n+1)\,I_O + \\ DI_{Lm} + I_O - (1-D)MI_O = 0 \\ \Rightarrow I_{Lm} = 0 \end{array} \tag{34}$$

Since the average current of the magnetizing inductance of BIT is zero, the core size of BIT will be reduced significantly. Hence, core losses will be decreased as well. This is one of the major advantages of the proposed structure. Utilizing the average current of diode D_1, the duration of mode IV could be given by:

$$\begin{array}{l} \langle i_{D1} \rangle = I_O \Rightarrow \frac{1}{2}\,(I_{in} + I_{Lm})\,d_4 = I_O \\ \frac{MI_O d_4}{2} = I_O \Rightarrow d_4 = \frac{2}{M} = \frac{2(1-D)}{3+2n} \end{array} \tag{35}$$

Substituting Eqs. (33) and (35) into Eq. (30), yields to:

$$V_{Lk}^{IV} = -\frac{2MnQ}{D} V_O = -\frac{2(3+2n)nQ}{D(1-D)} V_O \tag{36}$$

Substituting Eqs. (33), (35), and (36) into Eq. (28), the voltage of capacitor C_1 could be achieved as follows:

$$V_{C1} = \frac{D}{1-D} V_{in} \tag{37}$$

Substituting Eqs. (29), (33), (36) and (37) into Eqs. (7), (8), and (20), voltages of capacitors C_3, C_4, and C_5 could be given by:

$$V_{C3} = \left(n + 1 - \frac{4n^2 MQ}{D^2} \right) V_{in} \tag{38}$$

$$V_{C4} = \left(\frac{n+1}{1-D} - \frac{2n^2 MQ}{D} \left(M + \frac{2}{D} \right) \right) V_{in} \tag{39}$$

$$V_{C5} = \left(\frac{(2-D)(n+1)}{1-D} - \frac{2n^2 MQ}{D} \left(M + \frac{4}{D} \right) \right) V_{in} \tag{40}$$

The real voltage conversion ratio of the presented BIT-based DC-DC converter could be achieved by substituting Eqs. (29), (38), (39) and (40) into Eq. (21).

$$G_{CCM} = \frac{2n+3}{1-D} - \frac{4n^2 MQ}{D} \left(M + \frac{2}{D} \right) \tag{41}$$

Where G_{CCM} is the real voltage gain of the proposed converter. If the leakage inductance of the BIT is ignorable, the values of L_k and Q will be zero, and Eqs. (31) and (40) will be equal.

B) DCM operation

To simplify the discontinuous conduction mode (DCM) analysis of the presented structure, leakage inductance of the BIT is neglected. Hence, three different modes happen during one complete switching cycle. Fig. 4 shows the typical current flow paths of the operating modes.

Mode I [0<t<DT_S]: This mode begins when switch S is turned on. During this mode, input inductor L_{in} and magnetizing inductance of the BIT are charged through the switch S. Following equations could be formulated based on Fig. 4-(a).

$$v_{Lin} = V_{in} \tag{42}$$

$$v_{Lm} = V_{C2} - V_{C1} \tag{43}$$

Furthermore, voltages across capacitors C_3 and C_5 could be given by:

$$V_{C3} = (n+1)\,(V_{C2} - V_{C1}) \tag{44}$$

$$V_{C5} = V_{C3} + V_{C4} \tag{45}$$

Mode II [DT_S<t<$D_L T_S$]: The second mode begins when switch S is turned off. In this time interval, following equations could be obtained based on Fig. 4-(b).

$$v_{Lin} = V_{in} - V_{C2} \tag{46}$$

$$v_{Lm} = -V_{C1} \tag{47}$$

Moreover, voltage of capacitor C4 could be formulated as follows:

$$V_{C4} = V_{C3} + (n+1)\,V_{C1} \tag{48}$$

Mode III [$(D + D_L)T_S$<t<T_S]: The last mode begins when the current flowing through Diode D_5 reaches zero. During this mode, the current of inductors L_{in} and L_m are equal. This mode ends when switch S is turned on. Following equations could be formulated based on Fig. 4-(c).

$$v_{Lin} = v_{Lm} = 0 \tag{49}$$

By applying volt-second balance principles on inductors, voltages of capacitors C_1 and C_2 could be achieved as follows:

$$\langle v_{Lm} \rangle = 0 \Rightarrow V_{C1} = \frac{D}{D_L} V_{in} \tag{50}$$

$$\langle v_{Lin} \rangle = 0 \Rightarrow V_{C2} = \frac{D + D_L}{D_L} V_{in} \tag{51}$$

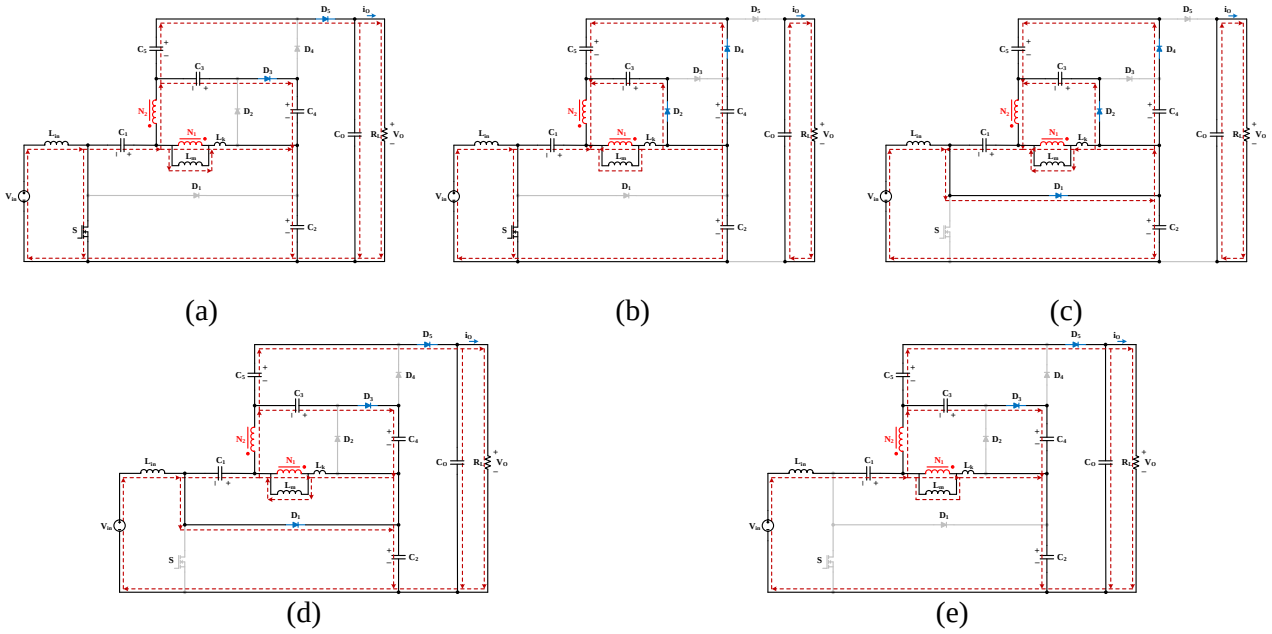


Fig. 2. Current-flow path of operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

Where D_L is the duty cycle of mode II. Substituting Eqs. (50) and (51) into Eqs. (44), (45) and (48), voltages across capacitors C_3 to C_5 could be obtained.

$$V_{C3} = (n+1)\,V_{in} \tag{52}$$

$$V_{C4} = \frac{(D+D_L)\,(n+1)}{D_L} V_{in} \tag{53}$$

$$V_{C5} = \frac{(D+2D_L)\,(n+1)}{D_L} V_{in} \tag{54}$$

Substituting Eqs. (51) to (54) into Eq. (21), output voltage V_O could be formulated as follows:

$$V_O = \frac{(D+D_L)\,(2n+3)}{D_L} V_{in} \tag{55}$$

According to Eq. (55), the duty cycle D_L could be obtained as follows:

$$D_L = \frac{D\,(2n+3)\,V_{in}}{V_O - (2n+3)\,V_{in}} \tag{56}$$

Applying KCL in different modes of the DCM operation of the structure and amp-second balance principals on capacitors, current of output capacitor C_O could be achieved as follows:

$$I_{CO} = \frac{DD_L V_{in} T_S}{4(n+1)V_{in}} \left(\frac{1}{L_{in}} + \frac{1}{L_m}\right) - I_O \tag{57}$$

By substituting Eq. (56) into Eq. (57) and regarding that average currents of capacitors are equal to zero under steady state, Eq. (57) could be rewritten as follows:

$$\frac{V_O}{R_L} = \frac{D^2 V_{in}^2 (3+2n) T_S}{4(n+1)[V_O-(3+2n)V_{in}]} \left(\frac{1}{L_{in}} + \frac{1}{L_m}\right) \tag{58}$$

Then, the normalized input inductor and magnetizing inductor time constants are defined as:

$$\tau_{Lin} = \frac{L_{in}}{R_L T_S} = \frac{L_{in} f_S}{R_L} \tag{59}$$

$$\tau_{Lm} = \frac{L_m}{R_L T_S} = \frac{L_m f_S}{R_L} \tag{60}$$

Substituting Eqs. (59) and (60) into Eq. (58), voltage gain of the converter under DCM operation could be formulated as follows:

$$M_{DCM} = \frac{V_O}{V_{in}} = \frac{3+2n}{2} + \sqrt{\frac{(3+2n)^2}{4} + \frac{D^2(3+2n)}{4(n+1)}\left(\frac{1}{\tau_{Lin}} + \frac{1}{\tau_{Lm}}\right)} \tag{61}$$

3. DESIGN OF THE PROPOSED CONVERTER

Slow dynamic response, high current stress of semiconductors, the dependence of the converter on frequency, output power, and the value of inductors are the main drawbacks of operating the converter in discontinuous conduction mode [15]. The current ripples of input inductor L_{in} and magnetizing inductance of the BIT could be formulated as:

$$\Delta i_{Lin} = \frac{V_{in} D}{L_{in} f_S} \;\&\; \Delta i_{Lm} = \frac{(V_{C2}-V_{C1})D}{L_m f_S} = \frac{V_{in} D}{L_m f_S} \tag{62}$$

To operate the converter in CCM, average current values of inductors L_{in} and L_m have to be more than half of their ripples. Ignoring voltage across the leakage inductance of the BIT, the following inequality could be achieved for the value of input inductor L_{in}.

$$L_{in} \geq \frac{DR_L}{2M^2 f_S} \tag{63}$$

Supposing boundary conduction mode (BCM) operation of the structure, currents flowing through the input inductor and

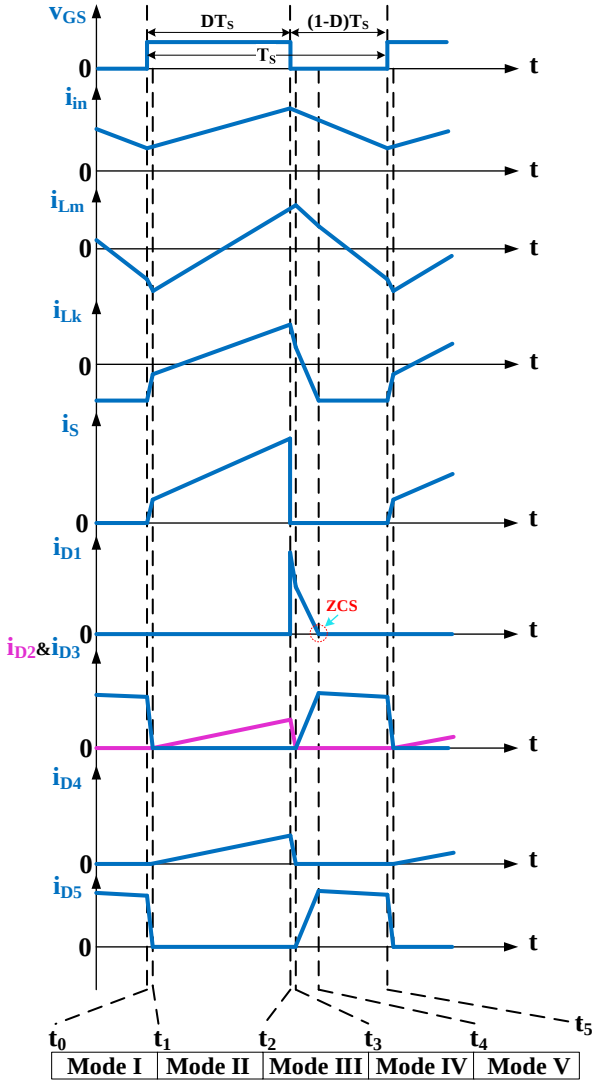


Fig. 3. Typical current waveforms of the proposed converter at CCM mode.

magnetizing inductance of the BIT will be equal at the end of one complete switching period [15]. It yields to:

$$\begin{aligned} i_{Lm_\min} = -i_{in_\min} \Rightarrow \\ I_{Lm} - \frac{\Delta i_{Lm}}{2} = \frac{\Delta i_{in}}{2} - I_{in} \end{aligned} \tag{64}$$

To ensure CCM operation of the designed structure, the following condition has to be satisfied as well.

$$I_{Lm} - \frac{\Delta i_{Lm}}{2} \geq \frac{\Delta i_{in}}{2} - I_{in} \tag{65}$$

The average current value of the magnetizing inductance of the BIT is zero. Hence, substituting Eq. (62) into Eq. (65) yields to:

$$L_m \geq \frac{DR_L L_{in}}{2M^2 L_{in} f_s - DR_L} \tag{66}$$

The designed structure will operate in CCM mode by satisfying the conditions of Eqs. (63) and (66). Ignoring Mode I, diode D_4 is reverse-biased when switch S is turned on. Hence, the current of output capacitor C_O is equal to the output current I_O until switch S is conducting. Neglecting output current ripple and the ESR of the output capacitor yields:

$$\begin{aligned} I_O = \frac{C_O|\Delta V_{CO}|}{DT_S} \Rightarrow \\ C_O = \frac{DV_O}{|\Delta V_{CO}|R_L f_S} \end{aligned} \tag{67}$$

Output capacitor value could be calculated from Eq. (67) by selecting the desirable output voltage ripple and switching frequency. The voltage and current stresses on switch S and diodes D_1-D_5 can be attained as:

$$V_{DS} = V_{D1} = V_{C2} = \frac{V_{in}}{1-D} \tag{68}$$

$$\begin{aligned} V_{D2} = V_{D3} = V_{D4} = \\ V_{D5} = V_{C4} = \frac{1+n}{1-D} V_{in} \end{aligned} \tag{69}$$

Regarding Eq. (69), the voltage stress on output diode D_5 is much less than the output voltage value. Hence, its reverse recovery problem is eliminated thoroughly. This is one of the major characteristics of the presented topology. Peak currents of diodes D_2 and D_4 are given by Eq. (34). The peak currents of the switch and the other three diodes can be formulated as:

$$\begin{aligned} i_{S,peak} = i_{D1,peak} = i_{in} + i_{Lk(t2)} + \\ 2i_{D2,peak} = \left(\frac{4(n+1)-D(2n+1)}{D(1-D)}\right) I_O \end{aligned} \tag{70}$$

$$i_{D3,peak} = i_{D5,peak} = \left(\frac{3+2n}{2\,(1+n)\,(1-D)}\right) I_O \tag{71}$$

4. THE CSF ANALYSIS AND COMPARISON STUDY

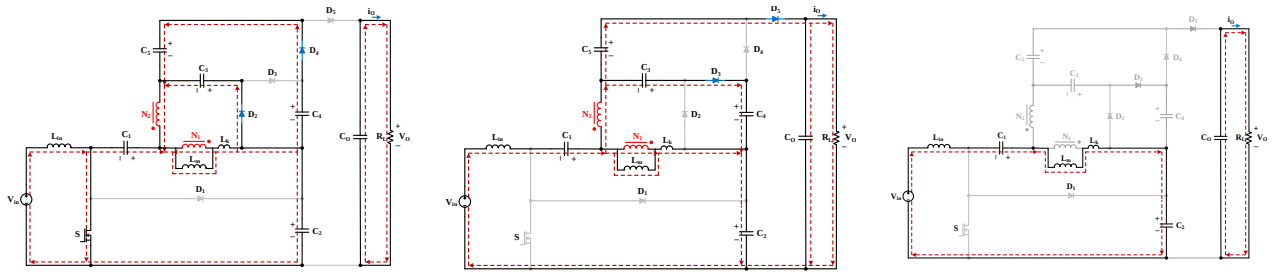
In Table 1, the presented converter is compared with some other structures presented recently in terms of the number of components, soft switching performance of semiconductors, continuity of input current, voltage gain, and voltage stresses on semiconductors. Moreover, voltage conversion ratios of some of the topologies mentioned in Table 1 are compared in Fig. 5 and Fig. 6.

According to Fig. 5, the designed converter has the highest voltage gain in comparison with other structures for duty ratios of more than 0.5. According to Fig. 6, compared to other structures, the proposed converter has higher voltage gain for turns ratios less than 3 at duty cycles of 0.6 and 0.7. However, for turns ratios of more than 3, converters in [17] and [26] have higher voltage gains. It is worth noting that voltage gains of the designed structure are about 22 and 32 for duty cycles 0.6 and 0.7 at n=3, respectively. The voltage gain of 16 is enough for single-phase PV applications. Hence, the presented converter is a suitable and feasible solution for PV applications.

To evaluate voltage stresses on semiconductors of structures mentioned in Table 1, component stress factor (CSF) analysis is utilized. This method considers maximum voltage and root mean square (RMS) values of currents flowing through components of the structure in a specific set of conditions and output power. Consequently, it gives a quantitative measure of the converter performance [31]. This procedure is similar to component load factor (CLF) analysis. However, they differ in how total and individual component factors are calculated.

To apply the CSF analysis, it is supposed that structures under study have the same resources of silicon, magnetic winding area, and capacitor volume. Hence, CSF analysis consists of three different parts: Semiconductor component stress factor (SCSF), winding component stress factor (WCSF), and capacitor component stress factor (CCSF). These parameters could be formulated as follows [32]:

$$SCSF_i = \frac{\sum_j W_j}{W_i} . \frac{V_{\max}^2 . I_{rms}^2}{P_O^2} \tag{72}$$



(a) (b) (c)

Fig. 4. Current-flow path of operating modes during one switching period at DCM operation. (a) Mode I. (b) Mode II. (c) Mode III.

Table 1. Comparison of presented converter with some step-up DC-DC structures.

Ref.	Number of components					L.I.C.R	S.S	Voltage gain	Voltage stress	$\sum V_D$
	S	D	C	M.C	T					
P.C	1	5	6	2	14	YES	YES	$\frac{3+2n}{1-D}$	$\frac{M}{3+2n}V_{in}$	$\frac{5+4n}{3+2n}MV_{in}$
[16]	1	8	8	2	19	NO	NO	$\frac{4+n(2-D)-D}{1-D}$	$\frac{M-n-1}{3+n}V_{in}$	$\frac{4M-1+n(2M-n-2)}{3+n}V_{in}$
[17]	1	5	5	1	12	NO	YES	$\frac{2+n(3-D)}{1-D}$	$\frac{M-n}{2(1+n)}V_{in}$	$\frac{(M-n)(3+5n)}{2(1+n)}V_{in}$
[18]	1	7	7	1	16	NO	NO	$\frac{3+n(2-D)}{1-D}$	$\frac{M-n}{3+n}V_{in}$	$\frac{(M-n)(5+3n)}{3+n}V_{in}$
[19]	1	5	7	3	16	NO	YES	$\frac{1+2n-D}{1-2D}$	$\frac{2M-1}{M+2n}V_{in}$	$\frac{(2M-1)(1+4n)}{M+2n}V_{in}$
[20]	1	5	6	1	13	NO	YES	$\frac{2+n(2-D)}{1-2D}$	$\frac{2M-n}{4+3n}V_{in}$	$\frac{(2M-n)(5+3n)}{4+3n}V_{in}$
[21]	2	5	5	2	14	YES	NO	$\frac{3+n-D}{1-3D+D^2}$	$\frac{(M+1+A)MV_{in}}{3M+2nM+1+A}$	$\frac{((2+2n)M+3+3A)MV_{in}}{3M+2nM+1+A}$
[22]	2	3	6	3	14	YES	YES	$\frac{2+n}{1-2D}$	$\frac{2+M+n}{2+n}V_{in}$	$\frac{3+2M+2n}{2+n}V_{in}$
[23]	2	6	6	2	16	YES	YES	$\frac{3+2n}{1-D}$	$\frac{2M}{3+2n}V_{in}$	$\frac{4+5n}{3+2n}MV_{in}$
[24]	2	4	6	2	14	YES	NO	$\frac{2(1+D)+2n(1-D)}{1-D}$	$\frac{2+M-2n}{2}V_{in}$	$\frac{2+2M+nM-2n^2}{2}V_{in}$
[25]	2	7	5	3	17	YES	YES	$\frac{2+D(n-1)}{1-D}$	$\frac{1+nM-n}{n+1}V_{in}$	$\frac{5M+4n-4+nM}{n+1}V_{in}$
[26]	1	6	6	2	15	YES	YES	$\frac{2+n_2+2n_3-n_3D}{1-D}$	$\frac{MV_{in}}{2+n_2+2n_3-n_3D}$	$\frac{(3+2n_2+n_3)MV_{in}}{2+n_2+2n_3-n_3D}$
[27]	2	4	5	3	14	NO	YES	$\frac{2+2n}{1-D}$	$\frac{M}{2n+2}V_{in}$	$\frac{4n+3}{2n+2}MV_{in}$

D: Diode, S: Switch, C: Capacitor, M.C: Magnet Core,
T: Total, S.S: Soft Switching, L.I.C.R: Low Input Current Ripple, $A=\sqrt{5M^2+(6+4n)M+1}$;

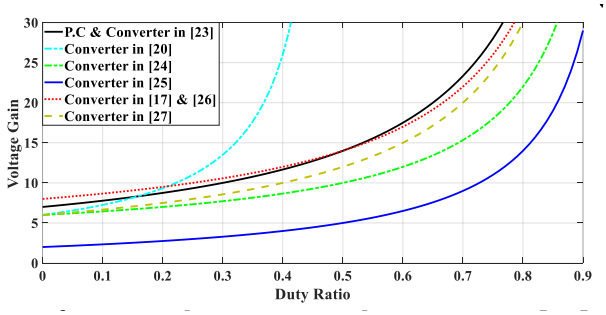


Fig. 5. Voltage gains of presented converter and structures in [17], [20], [23–27], n=2.

$$WCSF_i = \frac{\sum_j W_j}{W_i}.\frac{V_{\max}^2.I_{rms}^2}{P_O^2} \tag{73}$$

$$CCSF_i = \frac{\sum_j W_j}{W_i}.\frac{V_{pk}^2.I_{rms}^2}{P_O^2} \tag{74}$$

where $SCSF_i$, $WCSF_i$, and $CCSF_i$ are the CSF values of each semiconductor, inductor, and capacitor, respectively. Coefficients W_j and $\sum_j W_j$ represent the weight assigned to component i and the sum of weights assigned to components of the same type, respectively. The total CSF of each component of the same type could be calculated as follows:

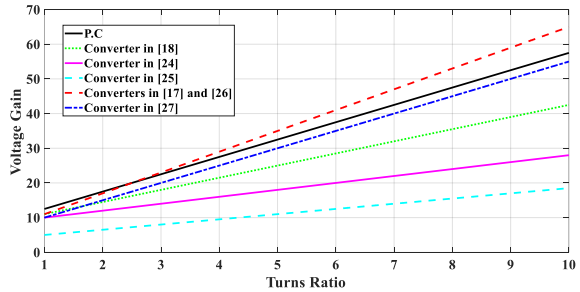
$$SCSF = \sum_{N_S} SCSF_i \tag{75}$$

$$WCSF = \sum_{N_W} WCSF_i \tag{76}$$

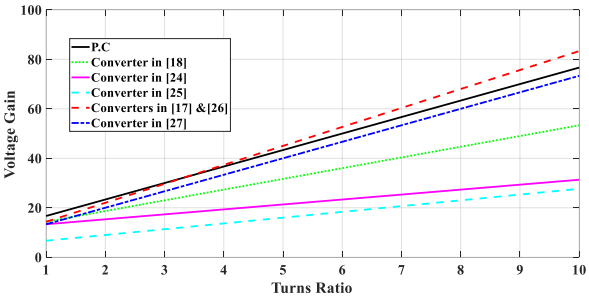
$$CCSF = \sum_{N_C} CCSF_i \tag{77}$$

Where N_S, N_W, and N_C symbolize numbers of semiconductors, inductors, and capacitors, respectively. To reduce the complexity of the analysis, it is assumed that: 1) capacitors and inductors are large enough without any ripples in their voltages and currents, respectively and 2) there is no power dissipation in components of the converter.

This analysis could also be used to find the best operating point of the converter in terms of lower stresses. Fig. 7 shows the SCSF as a function of duty ratio for n=2. As shown in this Fig., the SCSF has its lowest value at D=0.5. In other words, to minimize stresses on semiconductors, the converter has to operate at a 50% duty cycle.



(a) D=0.6



(b) D=0.7

Fig. 6. Voltage gains of presented converter and structures in [17], [18], [24–27].

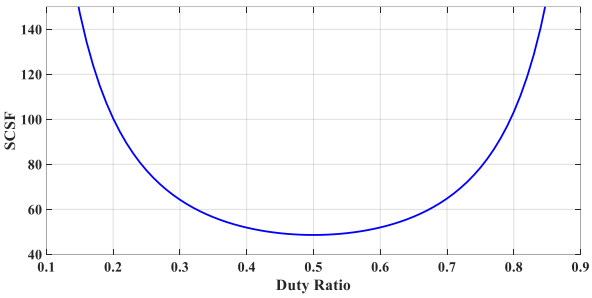


Fig. 7. Semiconductors CSF of proposed structure versus duty ratio, n=2.

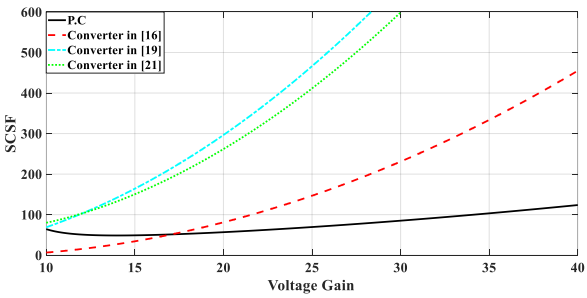


Fig. 8. Semiconductors CSF of presented topology and structures in [16], [19] and [21], n=2.

In Fig. 8, the $SCSF$ of the proposed converter and some of the structures mentioned in Table 1 are compared. The $SCSF$ of each structure is calculated with the same weighting factor. For simplicity, the weighting coefficient $\sum_j W_j$ is assumed to be unity and distributed equally among the semiconductors of each converter. As illustrated in this figure, the designed topology has a lower SCSF for voltage gains greater than 17.

5. EFFICIENCY ANALYSIS

The power losses of a converter are due to parasitic parameters of the circuit components. The equivalent circuit of the proposed converter considering parasitic parameters is depicted in Fig. 9. The efficiency of the proposed topology can be formulated by:

$$\eta = \frac{P_O}{P_O + P_{loss}} \tag{78}$$

Where PO is the output power and Ploss is the total power losses of the presented structure and includes power dissipations in semiconductor and passive components of the converter. Total power losses could be calculated by the sum of individual power dissipations in each component. It yields to:

$$P_{loss} = P_S^{loss} + P_D^{loss} + P_{Ca}^{loss} + P_I^{loss} \tag{79}$$

To simplify efficiency analysis, it is assumed that currents flowing through inductors are ripple-free. Hence, the RMS values of inductor currents will be equal to their average currents. Moreover, short transition modes I and III are neglected as well. The switch losses include switching and conduction losses and could be obtained by:

$$P_S^{loss} = P_{SW} + P_{C,S} \tag{80}$$

Where PSW and PC,S are switching and conduction losses of switch S, respectively and could be formulated as follows:

$$P_{SW} = f_S C_S V_S^2 \tag{81}$$

$$P_{C,S} = I_{S,rms}^2 R_{DS_ON} \tag{82}$$

Where VS and IS,rms are the maximum voltage across switch S and the current RMS value of switch S, respectively. Neglecting mode I, switch current could be formulated as:

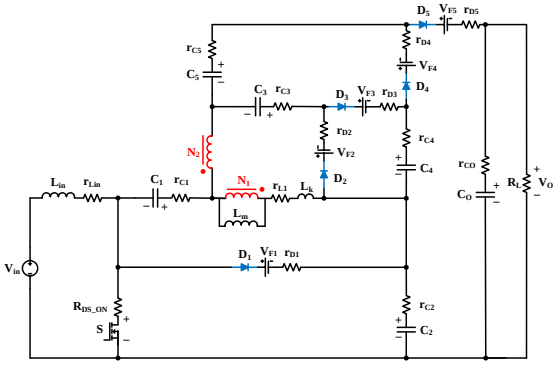


Fig. 9. Circuit diagram of the proposed converter considering parasitic parameters.

$$i_S = \frac{i_{S,peak}}{DT_S} \mathrm{t0} \leq t < DT_S \tag{83}$$

Where TS is the time length of one switching cycle. The current RMS value of switch S could be obtained as follows:

$$I_{S,rms} = \sqrt{\frac{D}{3}} \left(\frac{4\,(n+1) - D\,(2n+1)}{D\,(1-D)} \right) I_O \tag{84}$$

Hence, switch power losses could be calculated by substituting Eqs. (68) and (84) into Eqs. (81) and (82) and utilizing the

characteristics of the chosen switch. Since all diodes turn off under ZCS conditions, they have only conduction losses. Assuming that all diodes are the same, power dissipations in each diode could be formulated as:

$$P_D = I_{D,rms}^2 r_D + V_F I_{D,avg} \tag{85}$$

Where $I_{D,rms}$ and $I_{D,avg}$ represent the RMS and average current values of currents flowing through each diode, respectively. Meanwhile, r_D and V_F symbolize the conduction resistance and voltage drop of each diode, respectively. Currents flowing through diodes could be achieved as follows:

$$i_{D1} = i_{D1,peak}\left(1 - \frac{t}{d_4 T_S}\right) 0 \le t \le d_4 T_S \tag{86}$$

$$i_{D2} = i_{D4} = i_{D2,peak}\left(\frac{t}{DT_S}\right) 0 \le t \le DT_S \tag{87}$$

$$i_{D3} = i_{D5} = i_{D3,peak}\begin{cases} \frac{t}{d_4 T_S} 0 \le t < d_4 T_S \\ 1 d_4 T_S \le t < (1-D)\, T_S \end{cases} \tag{88}$$

The average currents of all diodes are equal to the output current I_O. Utilizing Eqs. (86) to (88), RMS values of diodes could be calculated as follows:

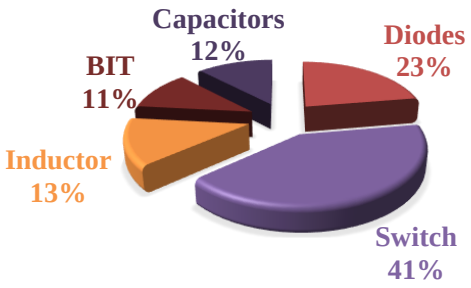


Fig. 10. Contribution of structures' components in total power losses. P_O=250W, V_O=400V, f_S=50kHz, n=2

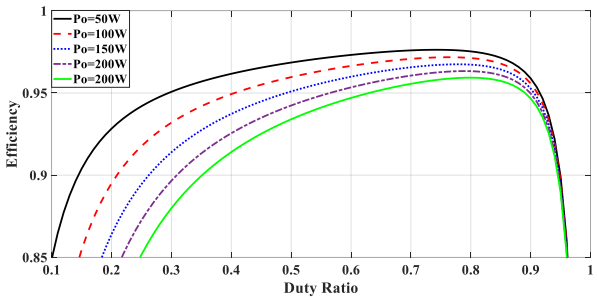


Fig. 11. Efficiency of presented structure as a function of duty ratio, n=2.

$$I_{D1,rms} = \sqrt{\frac{d_4}{3}}\left(\frac{4(n+1) - D(2n+1)}{D(1-D)}\right) I_O \tag{89}$$

$$I_{D2,rms} = I_{D4,rms} = \frac{2I_O}{\sqrt{3D}} \tag{90}$$

$$I_{D3,rms} = I_{D5,rms} = \sqrt{1 - D - \frac{2d_4}{3}}\left(\frac{3+2n}{2(1+n)(1-D)}\right) I_O \tag{91}$$

Power dissipation in each diode is obtained by substituting Eqs. (89) to (91) into Eq. (85) and utilizing characteristics of the selected diode. The total power losses of diodes could be calculated by:

$$P_D^{loss} = \sum_{k=1}^{5} P_{Dk} \tag{92}$$

Capacitor and inductor losses are caused by their ESR (r_C) and DC resistance, respectively. Their relative power losses could be formulated as follows:

$$P_{Ca}^{loss} = r_C \sum_{k=1}^{6} I_{C,rms_k}^2 \tag{93}$$

$$P_I^{loss} = r_{Lin} I_{Lin,rms}^2 + r_{L1} I_{Lk,rms}^2 \tag{94}$$

where $I_{C,\mathrm{rms}}$ is the RMS value of the capacitor current. $r_{L_{in}}$ and r_{L_1} symbolize the DC resistances of the input inductor L_{in} and the BIT, respectively. Meanwhile, $I_{L_{in},\mathrm{rms}}$ and $I_{L_k,\mathrm{rms}}$ represent the RMS values of the input inductor and BIT currents, respectively. The RMS values of currents flowing through capacitors and inductors are as follows:

$$I_{C1,rms} = I_O\left(\sqrt{\frac{16(n+1)^2}{3D} + \frac{(3+2n)^2}{1-D}} + \sqrt{\frac{d_4}{3}\left(\frac{4(n+1)-D(2n+1)}{D(1-D)}\right)^2}\right) \tag{95}$$

$$I_{C2,rms} = I_O\left(\sqrt{\frac{16(n+1)^2}{3D} + \frac{(3+2n)^2}{1-D}} + \sqrt{\left(1 - D - \frac{2d_4}{3}\right)\left(\frac{3+2n}{2(1+n)(1-D)}\right)^2}\right) \tag{96}$$

$$I_{C3,rms} = I_{C4,rms} = I_{C5,rms} = I_O\sqrt{\frac{4}{3D} + \left(1 - D - \frac{2d_4}{3}\right)\left(\frac{3+2n}{2(1+n)(1-D)}\right)^2} \tag{97}$$

$$I_{CO,rms} = I_O\sqrt{1 + \left(1 - D - \frac{2d_4}{3}\right)\left(\frac{3+2n}{2(1+n)(1-D)}\right)^2} \tag{98}$$

The power losses of capacitors could be calculated by substituting Eqs. (65) to (98) into Eq. (93). The RMS values of currents flowing through input inductor L_{in} and BIT can be given by:

$$I_{Lin,rms} = MI_O \tag{99}$$

$$I_{Lk,rms} = I_O\left(\sqrt{\frac{d_4}{3}\left(\frac{4(n+1)-D(2n+1)}{D(1-D)}\right)^2 + \frac{(3+2n)^2}{(1-D)}} + \sqrt{\frac{16n^2}{3D} + \left(1 - D - \frac{2d_4}{3}\right)\left(\frac{3+2n}{2(1+n)(1-D)}\right)^2}\right) \tag{100}$$

The contribution of components of the designed topology in total power losses at the output power of 250 W is depicted in Fig. 10. According to this Fig., major losses of the structure are caused by switch losses. Meanwhile, BIT has the lowest portion in losses. The total power loss value of the presented structure could be achieved by substituting Eqs. (80), and (92) to (94) into Eq. (79). Finally, the converter efficiency could be calculated by Eq. (78).

$$\eta = \frac{R_L}{\left(M^2+1\right)r_C+\left(\frac{5V_F}{V_O}+1\right)R_L+A_1+f_S C_S\left(\frac{R_L}{3+2n}\right)^2+A_2+3M^2(1-D)r_L+\frac{8}{3D}\left(r_D+\left(4(n+1)^2+1\right)r_C\right)} \quad (101)$$

Where R_L is the output load, and A_1 and A_2 are as follows:

$$A_1 = \left(DR_{DS_ON}+\frac{2(r_D+r_C+r_L)}{M}\right)\left(\frac{4(1+n)-D(1+2n)}{3D(1-D)}\right)^2 \quad (102)$$

$$A_2 = (2r_D+5r_C+r_L)\left(\frac{(3+2n)(5+6n)}{12(1-D)(1+n)^2}\right) \quad (103)$$

According to Eq. (101), the converter efficiency decreases by increasing the switching frequency and BIT turns ratio. In case the output voltage remains constant, the efficiency will rise by increasing the input voltage. Furthermore, the efficiency of the studied structure at different output powers is depicted in Fig. 11. As shown in this Fig., by increasing the duty ratio, efficiency increases until it reaches D=0.8. For duty ratios of more than 0.85, there is a sharp fall in efficiency. Hence, in practice, the duty cycle of the structure is limited to 0.85.

The theoretical and measured efficiencies of the proposed converter are also depicted in Fig. 12. As illustrated in this Fig., by raising output power, efficiency lowers slightly. According to this Fig., efficiency reaches a peak of 95.2% at the output power of 125 W.

6. EXPERIMENTAL RESULTS

To confirm the theoretical analysis and practicability of the designed structure, a 250-W prototype topology operating at the frequency of 50 kHz is implemented and examined. Fig. 13 shows the experimental prototype of the proposed converter. Different components are named in this Fig. as well.

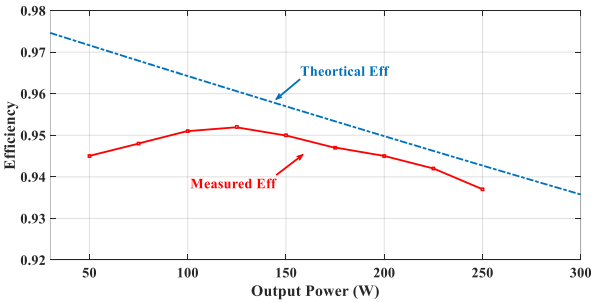


Fig. 12. Theoretical and measured efficiency of presented structure as a function of output power. n=2, r_C=r_D=10mΩ, r_{Lin}=r_{L1}=20mΩ, R_{DS_ON}=40mΩ, C_S=600pF, V_F=1V, f_S=50kHz.

The components are designed to boost an input voltage of 25 V to an output voltage of 400 V at the output power of 250 W. Hence, the ideal voltage gain, the output current, and load value could be calculated as follows:

$$M = \frac{V_O}{V_{in}} = 16 \quad (104)$$

$$I_O = \frac{P_O}{V_O} = 0.625A \quad (105)$$

$$R_L = \frac{V_O^2}{P_O} = 640\Omega \quad (106)$$

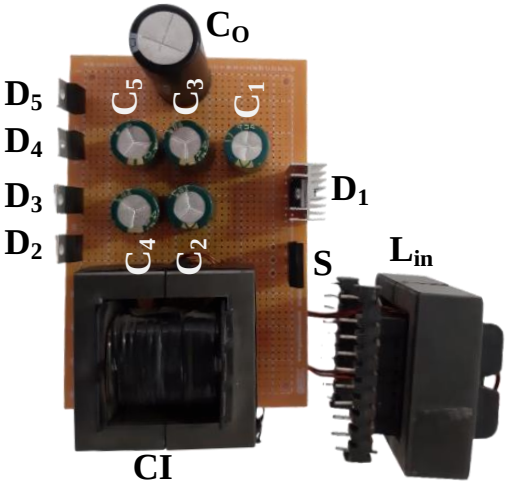


Fig. 13. Experimental prototype of the proposed converter.

Table 2. Circuit parameters of the implemented prototype.

Parameter	Value
Input voltage (V_{in})	25V
Output voltage (V_O)	400V
Output power (P_O)	250W
Output load (R_L)	640Ω
Capacitors ($C_1 - C_5$)	$47\mu H$
Output capacitor (C_O)	$180\mu H$
Input inductor (L_{in})	$320\mu H$
Magnetizing inductance of BIT (L_m)	$100\mu H$
Turns ratio of BIT (n)	n=2
Switching frequency (f_S)	50kHz
Power switch (S)	IRFP260n
Diodes ($D_1 - D_5$)	MUR1560

Fig. 5 shows the variation of the voltage gain vs. the duty ratio for n=2. According to this Fig., for M=16 and n=2, duty ratio D is close to 0.6. As this value is desirable, the turns ratio of the BIT is selected to be 2. Hence, the ideal duty ratio could be calculated by Eq. (31).

$$D = \frac{M-3-2n}{M} \simeq 0.57 \quad (107)$$

Semiconductors: According to Eqs. (32), and (68) to Eq. (71), the voltage and the current stresses of the switch and diodes could be calculated as follows:

$$V_{DS} = V_{D1} \simeq 58.5V \quad (108)$$

$$V_{D2} = V_{D3} = V_{D4} = V_{D5} \simeq 175.5V \quad (109)$$

$$i_{S,peak} = i_{D1,peak} \simeq 23.5A \quad (110)$$

$$i_{D2,peak} = i_{D4,peak} \simeq 2.2A \quad (111)$$

$$i_{D3,peak} = i_{D5,peak} \simeq 1.7A \quad (112)$$

Hence, suitable semiconductor components could be selected by utilizing the aforementioned equations.

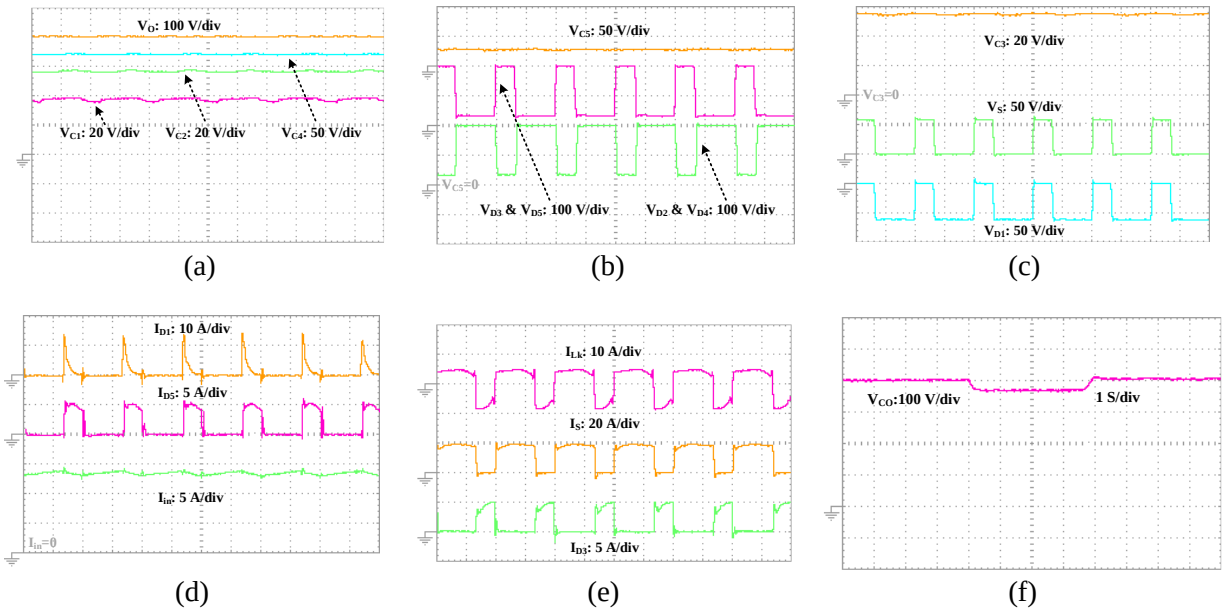


Fig. 14. Experimental result of the prototype converter (Time/Div=10us). (a) voltages of capacitors C_1, C_2, C_4, and output voltage, (b) voltage of capacitor C_5 and voltages across diodes D_2 to D_5, (c) voltage of capacitor C_3, voltages across switch S and diode D_1, (d) Input current and currents flowing through diodes D_1 and D_5, (e) currents flowing through switch S, BIT and diode D_3, (f) dynamic performance to step change of output voltage.

Capacitors: To have a voltage with the lowest possible ripple, the voltage ripple of 0.05% of the voltage on the capacitor is selected. Therefore, the minimum suitable value for capacitors is calculated as follows:

$$C \simeq 35.5\mu F \tag{113}$$

Hence, values of capacitors C_1 to C_5 are selected to be 47 μF and the output capacitor value is selected to be 180 μF to guarantee the lowest ripple for output voltage.

Inductors: Utilizing Eq. (63), the minimum value of the input inductor could be given by:

$$L_{in} \geq 14.25\mu H \tag{114}$$

To reduce the input ripple current, the value of the input inductor L_{in} is selected to be 320 μH. The minimum value of magnetizing inductance of the BIT could be achieved as follows:

$$L_m \geq 14.95\mu H \tag{115}$$

Like the procedure of selecting the input inductor value, the value of magnetizing inductance of the BIT is selected to be 100 μH. Specifications of the constructed converter are listed in Table 2. At the end, steady-state waveforms of components are depicted in Fig. 14.

Fig. 14-(a) shows the voltages of capacitors C_1, C_2, C_4 and the output voltage V_O. In Fig. 14-(b), the voltage of capacitor C_5 and voltages across diodes D_2, to D_5 are depicted. This Fig. shows that diodes D_3 and D_5 voltages are equal. Meanwhile, the voltages of diodes D_2 and D_4 are the same. The voltage stress of output diode D_5 is about 170 V, much lower than output voltage. Fig. 14-(c) represents the voltage of capacitor C_3 and voltages across switch S and clamp diode D_1. Currents flowing through diodes D_1 and D_5 along with input current are depicted in Fig. 14-(d). As shown in this Fig., the input current ripple is less than 1 A. Moreover, according to this Fig., diode D_1 turn off under ZCS conditions. In Fig. 14-(e), currents of switch S, diode D_3, and BIT are illustrated. According to this Fig., the mean value of BIT current is zero. Fig. 14-(f) depicts the dynamic performance of the presented structure to a step change of output voltage. As shown in this Fig., output voltage is decreased by about 50 V and raised again to 400 V. As it is seen, it takes a short time (about 30ms) for the converter to follow the output change.

7. Conclusion

This paper presents and thoroughly analyzes a non-isolated high-gain BIT-based DC-DC converter for PV applications. Unlike most DC-DC converters that use coupled inductors (CIs), the proposed structure employs a BIT and an improved voltage multiplier (VM) cell to enhance voltage gain. Compared to CI-based DC-DC converters, BIT-based converters offer several advantages, including balanced core magnetic flux, improved saturation capability, reduced core size, and lower conduction losses. Additionally, a passive voltage clamp is used to recycle energy stored in the leakage inductance of the BIT, reducing voltage stress on the switch. As a result, a switch with low on-resistance is chosen for the implementation of the structure. The converter also provides continuous input current with minimal ripple and a shared common ground between the input, switch, and load—further improving the design. The use of BIT enhances the converter's efficiency while reducing core size. Since the voltage stress on the output diode is relatively low and it turns off under zero-current switching (ZCS) conditions, the reverse recovery problem is eliminated. A detailed steady-state analysis of the structure is provided, with design considerations for components, such as semiconductors, inductors, and capacitors, discussed in detail. Additionally, a CSF analysis of the proposed converter is conducted, and the structure is compared with other recent topologies. The results of the comparison highlight the advantages of the proposed configuration over other converters. Finally, a 250-W laboratory prototype is built, and experimental results are presented to validate the theoretical analysis and demonstrate the practical viability of the structure. The results confirm the accuracy of the analysis and affirm the converter's potential for use in PV systems.

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