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Research Paper

Asynchronous Motor Drive Using an Inverter with Adjustable DC-Link Voltage

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Abstract— *With a fixed DC-link voltage, the high-frequency harmonic content of an inverter's output voltage and current increases significantly compared to the fundamental component. In electric motor drives, however, the output voltage magnitude varies over a wide range depending on the speed command, which can range from zero to the rated speed. As a result, when the motor operates at speeds well below the rated value, the fundamental component of the output voltage is low, leading to a high total harmonic distortion (THD). To address this issue, this study proposes an inverter with an adjustable DC-link voltage for asynchronous motor drives. The inverter switches between two predefined DC-link voltage levels: a higher voltage for high-speed operation and a lower voltage (half of the full DC voltage) for low-speed operation. Consequently, in the lower speed range—approximately up to half of the rated speed—the THD of the output voltage and current is significantly reduced. In addition, the harmonic modeling of the motor and power loss analysis of the drive system are presented. The proposed approach, unlike other similar concepts, is simple and feasible for implementation in real-world applications. Simulation results obtained using MATLAB/Simulink confirm the effectiveness of the proposed method in reducing harmonic content in asynchronous motor drives.*

Keywords—Asynchronous motor drive, total harmonic distortion (THD), adjustable DC-link.

1. INTRODUCTION

1.1. Background and motivation

Asynchronous motors play a vital role in various industries by providing the required motion for different applications. They are currently favored over other types of motors due to several industry-friendly characteristics. Unlike in past decades, modern applications often require precise control of motor speed and torque. As a result, asynchronous motors are commonly paired with drive systems to meet these control demands. The performance of the motor drive system has a significant impact on the overall operation of the electric motor. Consequently, the performance of motor drives has been widely studied, and numerous control strategies and power circuit designs have been proposed in the literature to improve their efficiency and reliability. Although extensive research has been conducted on asynchronous motor drives, there remain specific gaps in the field that warrant further investigation. One major issue is the poor output power quality—particularly in terms of voltage and current harmonics—during low-speed operation. While a few studies have addressed this challenge, they each have their own limitations. The primary motivation of this research is to tackle the issue of degraded output power quality in motor drive systems operating at low speeds with a simple and realistic method that is feasible for practical implementation.

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1.2. Literature review

In [1], determination of the zero sequence signal injection to the reference signal in pulse-width modulation (PWM) for a split-phase induction motor drive is presented. In this work, the value of the injected zero-sequence signal is determined in a way that the total harmonic distortion (THD) of the current is reduced considerably. In [2], the low switching frequency operation of induction motor drive is investigated and the torque harmonics are evaluated analytically, then, the optimal switching angles are calculated to minimize the torque harmonics. The method is suitable for high-power motor drives where the switching frequency has limits. The high-resolution switched-capacitor multilevel inverter and its space vector PWM (SVPWM) for an open end winding induction motor drive is studied in [3]. As the resolution of the voltage is high enough, the switching frequency and hence the switching losses are minimized. In [4], a modified three-phase inverter called H10 inverter is proposed for three-phase induction motor drive. This inverter consists of a standard three-phase inverter and four extra power electronic switches on the DC side to form a switched DC-link voltage. The primary aim is to limit the common-mode voltage, however, the output current THD is also reduced. Another so called H8 inverter has been presented in [5] for motor drive applications. Using the extra vectors available in this inverter, the common mode voltage and the output current THD is reduced. It is notable that this inverter is a variant of the H10 inverter mentioned earlier. Ref. [6] studies a split power converter structure for an open end winding motor drive which can generate 24-sided polygon voltage apace vectors. As the voltage space vectors are increased, the switching frequency is reduced, and the output current harmonics are also reduced. In high-power motor drives, the switching frequency is strictly limited to reduce the switching power losses. In this condition, the number of pulses per cycle and their arrangement and widths are very important. In [7], the optimal switching angles of a low switching frequency operated motor

drive is studied in order to reduce the output current harmonics. Two modified modulation methods are presented in [8] for a motor drive based on three-phase three-level H-bridge inverter. The results indicate lower current harmonics and torque ripples using these PWM methods. Ref. [9] presents an induction motor drive using the four switch three-phase inverter and fuzzy logic to improve its harmonic performance when operating at low speeds. A multilevel inverter-based drive for an open-end winding induction motor has been presented in [10]. It is shown that when using a three-level neutral point clamped (NPC) inverter accompanied with a two-level standard inverter instead of a five-level NPC inverter, the harmonics and power losses are reduced. In [11] a hybrid cascaded multilevel inverter, consisting of a five-level NPC and a three-level H-bridge inverter in each phase, is used for a motor drive application. The switching angles are obtained to minimize the current THD. In [12], a split multilevel inverter based open-end induction motor drive is presented. It is a hybrid asymmetric multilevel inverter with 24 voltage steps which improve the output current quality significantly. However, the topology is complicated and providing the DC voltage sources with the required values is challenging. Similar research has been presented in [13] where a split-phase induction motor drive using a hybrid multilevel inverter is investigated. In this case also, the topology of the converter is complicated, and it is necessary to provide DC voltage sources with different values. A multilevel inverter induction motor drive is presented in [14]. In this work, a switched capacitor based multilevel inverter is presented for the drive application. The multilevel inverter uses lower components, however, as for the other multilevel inverter based drive systems, the harmonics of the output voltage and current increase when the motor operates in low-mid speed range. Another hybrid multilevel inverter is presented in [15] for the medium voltage induction motor drives. As it uses the multilevel inverter, the harmonics of the output current is reduced, however, it does not discuss improving the current harmonics in low-speed operation of the motor. a similar research is presented in [16]. An open-end winding induction motor drive is presented in [17, 18] in which the second inverter is operating at variable DC-link voltage to improve the drive performance. However, it requires two VSIs and the total DC-link voltage is semi-controlled because only the DC-link voltage of the second inverter is controlled.

A great deal of effort devoted to reducing the drive output current harmonics as well as the torque ripples in the literature including the papers mentioned above. However, less research works address the THD and torque ripple mitigation in variable speed operation, especially in low-speed range. The idea of making the DC-link voltage adjustable according the required output voltage in variable voltage applications has been presented in [19] and then it is applied on dynamic voltage restorer in [20]. The concept is then applied in multilevel inverter selective harmonic elimination (SHE) modulation method to get proper solution in low modulation index region [21–24].

1.3. Contribution and organization of this research

As reviewed above, substantial research has focused on enhancing motor drive performance, particularly in reducing output current harmonics. The predominant approach involves the use of multilevel or multistep converters to mitigate harmonics, which proves effective under near-nominal operating conditions. However, in low-speed operation, the output voltage levels decrease significantly, leading to a considerable increase in current harmonics. Although a few studies have attempted to address this issue, they typically rely on DC-DC converters to generate variable DC voltage—an approach that is not well-suited for motor drive applications. Examples of motor drives with DC-DC converters can be found in [25–27]. The main issue with the application of the DC-DC converters in drives to adjust the DC-link voltage is the limited power rating of the converters. In the practical applications, multiple DC-DC converters should be used which operate in parallel. This will increase the cost of the system. Other studies target multilevel inverters rather than the simple and commercially available inverter structures. The variable DC voltage concept is used in [28] to control the capacitors' voltage of a modular multilevel converters (MMC) drive. In this research it is demonstrated that using the flexible voltage control of the capacitors in MMC drive enhances the motor current quality considerably. This method can only be used in MMC drives and it cannot be integrated into conventional three-phase drives. In this paper, we propose a method that applies an adjustable DC-link voltage to a three-phase motor drive. The DC-link voltage is set to either a low or high value, corresponding to the motor's low- and high-speed operating ranges, respectively. This technique leads to notable improvements in current quality and a reduction in torque ripple during low-speed operation. Moreover, the proposed method is simple and feasible for real-world applications. The proposed method is presented in Section 2. In Section 3, the harmonic modelling of the motor is presented which can be used to analyze the performance and power losses of the motor due to the harmonics. In Section, 4, the power loss analysis of the system is presented which is later used to estimate the power losses in the proposed system. Comparisons of the proposed method with other relevant methods are conducted in Section 5. The simulation studies and discussions are given in Section 6 and finally the conclusions are presented in Section 7.

2. PROPOSED ASYNCHROUNOUS MOTOR DRIVE

2.1. Power circuit description

The basic concept behind the proposed idea is to make the DC-link voltage stepwise rather than fixed in a drive system. In a conventional drive system, the DC-link voltage is constant. Therefore, when the output voltage is low due to a low-speed command, the modulation index of the inverter becomes very low. Under these conditions, the fundamental component of the output voltage is significantly reduced, while the harmonic content at the switching frequency remains nearly constant. As a result, the total harmonic distortion (THD) of the output voltage and current becomes high at low modulation indices.

To address this issue, the DC-link voltage can be adjusted according to the required output voltage. However, continuously varying the DC-link voltage may require more complex circuitry, leading to higher costs and increased power losses. A more practical solution is to vary the DC-link voltage in discrete steps.

To implement this, a modification is made to the power circuit of a standard three-phase motor drive. The proposed power circuit topology for the asynchronous motor (ASM) drive is shown in Fig. 1. As illustrated, an auxiliary circuit is added to the standard drive circuit. This auxiliary circuit consists of four power electronic switches, labeled S_1, S_2, S_3, and S_4 in Fig. 1.

This auxiliary circuit is responsible for adjusting V_{DC2} based on the speed command and the output voltage required to provide the speed. It should be noted that if the magnitude of the three-phase AC source voltage is constant, i.e., there is no voltage dip, the value of V_{DC1} is constant. Although the auxiliary part can be employed in different ways, in this study it is used to provide two different voltage values of V_{DC1} and $0.5V_{DC1}$ assuming that the voltages $V_{DC,U}$ and $V_{DC,L}$ are balanced, and each one is $0.5V_{DC1}$. Table 1 shows the switching states and the output voltage of the auxiliary circuit in different switching combinations. When the switches S_1 and S_3 are turned on, the output voltage of the auxiliary switch is equal to $V_{DC,U}$ and in the case that the switches S_2 and S_4 are turned on, the output voltage is equal to $V_{DC,L}$. If it is assumed that $V_{DC,U} = VDC,L = 0.5V_{DC1}$, the switching states 1 and 2, in the table, are redundant states. However, if only one of these redundant states is used continuously, the voltage on the capacitors, $V_{DC,U}$ and $V_{DC,L}$, will be severely

unbalanced. Therefore, both the redundant switching states must be used to balance the capacitors' voltage. Taking advantage of the redundant switching states, the capacitors' voltage balancing can be realized. For the low-speed range, up to less than half of the rated speed, the switching states 1 and 2 are used alternatively to generate the output voltage which is equal to $0.5V_{DC1}$. In this way, in the low-speed range where low output voltage is required, the modulation index of the inverter increases resulting in higher quality of the output voltage and current in terms of the harmonic contents. For high-speed range, above half the rated speed, the switching state 3 is used to have the full DC-link voltage available at the input side of the inverter.

2.2. Advantages and drawbacks

The proposed drive has its own unique advantages. However, like any other system, it has also some drawbacks in comparison with the conventional drive. As described before, the main feature is the higher quality of the output voltage and current in the low-speed range. Also, it has lower switching power losses and lower voltage stresses on the switches in the low-speed range because of reduced (halved) voltage on the switches of the main inverter in the mentioned range. The main drawback is adding four additional power-electronic switches, which increases the cost and conduction power losses of the system. However, the voltage rating of the additional switches is half of the main switches of the inverter which reduces the cost of the additional switches dramatically. On the other hand, the switching frequency of these switches is much lower than the main inverter switching frequency (close to the fundamental frequency) which results in lower cost of them so that their switching losses are negligible. Therefore, the additional switches' cost is much lower than the main switches and considering the other prominent advantages, it makes sense, technically and economically, to use the proposed drive.

As an alternative to the proposed method, an active rectifier (instead of a diode rectifier) can be used to regulate the DC-link voltage and shape the input current. In this case, an additional three-phase converter is required, with voltage and current ratings equal to those of the inverter. This effectively increases the cost of the inverter (i.e., a 50% increase); however, it offers greater flexibility and improved performance in terms of continuous regulation of the DC-link voltage and input current quality. Also, the power losses in this case are increased by approximately %50.

On the other hand, the proposed method requires only four additional switches, each with a voltage rating equal to half that of the main switches. In other words, the cost of the inverter increases by only 25% with the proposed method.

2.3. Modified control

As the core of the proposed drive is the classic three-phase inverter, the main control of the inverter remains untouched. Therefore, all the conventional control systems including the constant Volt/Hertz (constant V/f), vector control, and the direct torque control (DTC) could be used. However, a simple control and switching method is added on the main control system to control the auxiliary circuit. The control principle used for the auxiliary circuit is simple; in the high speed range, namely above half of the rated speed, the switches S_1 and S_4 are turned on without any other consideration and in low speed range namely below half of the rated speed, the switch pairs (S_1, S_3) or (S_2, S_4) are turned on alternatively to get the output voltage of half of the DC-link voltage and to ensure the capacitors voltage balance.

Fig. 2 shows the control system adopted to control the auxiliary circuit. To guarantee the voltage balance of the capacitors, feedback from their voltage is given to a logic circuit to decide which of the auxiliary switches must be switched on. It should be noted that to prevent the unnecessary high-speed switching of the auxiliary switches, a hysteresis voltage controller is used. Based on the hysteresis band, the switching frequency of the switches

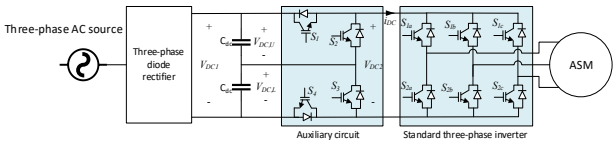


Fig. 1. The proposed asynchronous motor (ASM) drive using an inverter with adjustable DC-link voltage.

Table 1. Employed switching states of the auxiliary circuit.

Number	State of the switches				Output voltage V_{DC2}
	S_1	S_2	S_3	S_4	
1	1	0	1	0	$V_{\mathrm{DC,U}}$
2	0	1	0	1	$V_{\mathrm{DC,L}}$
3	1	0	0	1	V_{DC1}

is variable, however, this switching frequency is close to the fundamental frequency rather than the switching frequency of the main inverter. Therefore, the auxiliary switches operate at a very low switching frequency resulting in lower switching losses and lower cost of them.

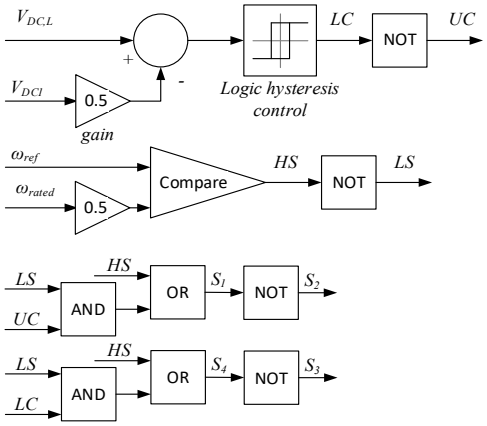


Fig. 2. Control method for the auxiliary circuit.

3. HARMONIC MODELLING OF THE ASYNCHRONOUS MACHINE

To evaluate the effect of the proposed method on the motor performance, the harmonic modelling of the motor is presented in this section. The equivalent circuit of a voltage-source-fed induction motor is shown in Fig. 3-(a) for the fundamental (h=1) and for the harmonic of order h. Using Thevenin's theorem (subscript TH), the magnetizing branch can be eliminated (Fig. 3-(b)).

According to the Thevenin equivalent circuit shown in Fig. 3-(b), the motor current can be written as follows:

$$I_{shTH} = \frac{V_{shTH}}{\left(R_{shTH} + \dfrac{R'_r}{s_h}\right) + jh\omega_1 \left(L_{slTH} + L'_{rl}\right)} \tag{1}$$

Using the previous equation, the h^{th} harmonic torque is obtained as:

$$T_{eh} = \frac{1}{\omega_{sh}} \frac{q_1 V_{shTH}^2 \dfrac{R'_r}{s_h}}{\left(R_{shTH} + \dfrac{R'_r}{s_h}\right)^2 + (h\omega_1)^2 \left(L_{slTH} + L'_{rl}\right)^2} \tag{2}$$

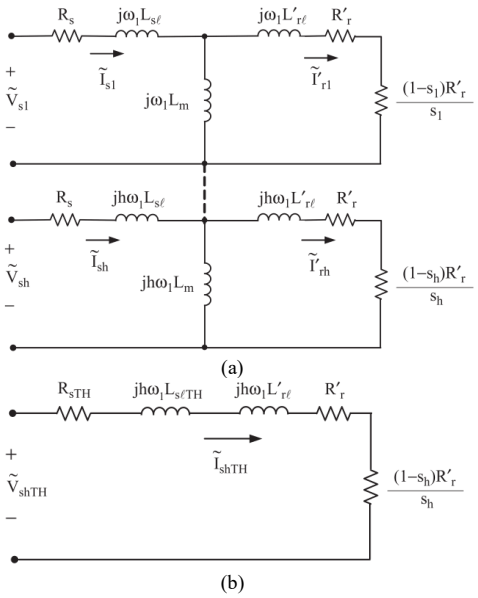


Fig. 3. (a) Per-phase equivalent circuit of three-phase induction machine for fundamental (h=1) and h^{th} harmonic fed by voltage source. (b) Thevenin (TH) adjusted per-phase equivalent.

In the equations above, s_h is harmonic slip and it is defined as:

$$s_h = \frac{h\omega_{s1} - \omega_m}{h\omega_{s1}} \tag{3}$$

In Eq. (3), ω_{s1} is the mechanical angular speed, and it is equal to $\frac{2}{p}\omega_1$, where ω_1 is the electrical angular frequency of the fundamental component. It is important to note that the value of h in the equation above is positive for the positive-sequence harmonics (e.g. 4^{th}, 7^{th}, 13^{th}) and negative for the negative-sequence harmonics (e.g. 2^{nd}, 5^{th}, 8^{th}, 11^{th}).

To clarify the parameters used in the previous equations, they are obtained using the motor per-phase parameters as follows:

$$V_{shTH} = \frac{V_{sh}\,(h\omega_1 L_m)\angle\theta_{hTH}}{\sqrt{R_s^2 + (h\omega_1 L_{sl} + h\omega_1 L_m)^2}} \tag{4}$$

$$\theta_{hTH} = \frac{\pi}{2} - \tan^{-1}\left(\frac{h\omega_1 L_{sl} + h\omega_1 L_m}{R_s}\right) \tag{5}$$

$$R_{shTH} = \frac{h^2(\omega_1 L_m)^2 R_s}{R_s^2 + (h\omega_1 L_{sl} + h\omega_1 L_m)^2} \tag{6}$$

$$h\omega_1 L_{slTH} = \frac{h(\omega_1 L_m)R_s^2 + h^2(\omega_1 L_{sl})(\omega_1 L_m)[h(\omega_1 L_{sl}) + h(\omega_1 L_m)]}{R_s^2 + (h\omega_1 L_{sl} + h\omega_1 L_m)^2} \tag{7}$$

The analysis given in this section can be used to harmonic power losses analysis in the motor.

4. POWER LOSSES ANALYSIS

4.1. Power losses in the inverter

In the inverter there are mainly two types of power losses: the conduction and the switching power losses. To calculate the conduction power losses, the output current can be approximated as a sinusoidal current with the magnitude of I_m. Let $P_{c,T}$ and $P_{c,D}$ be the conduction power losses of the transistor and the diode in an IGBT, respectively. They can be approximated as follows:

$$\begin{aligned} P_{c,T}(t) &= V_{\mathrm{on},T}\, i(t) + R_{\mathrm{on},T}\, i^2(t) \\ P_{c,D}(t) &= V_{\mathrm{on},D}\, i(t) + R_{\mathrm{on},D}\, i^2(t) \end{aligned} \tag{8}$$

In the equations above, $V_{on,T}$, $V_{on,D}$ represent the on-state voltage drops across the transistor and diode of an IGBT, respectively. Also, $R_{on,T}$ and $R_{on,D}$ denote the equivalent resistance of the transistor and diode, respectively. These parameters can be obtained from the datasheet of a specific IGBT.

Let assume that the output displacement angle is φ. Using the estimations above, the average conduction power losses in a typical leg of the three-phase inverter can be calculated as follows:

$$\begin{aligned} &P_{c,\mathrm{leg}} = \\ &\tfrac{1}{\pi}\Big[\textstyle\int_0^{\varphi} (S(t)P_{c,D}(t) + (1 - S(t))P_{c,T}(t))\,d(\omega t) + \\ &\textstyle\int_{\varphi}^{\pi} (S(t)P_{c,T}(t) + (1 - S(t))P_{c,D}(t))\,d(\omega t)\Big] \end{aligned} \tag{9}$$

here, $S(.)$ is the leg switching function which takes a binary value and depends on the switching method used. If the upper switch of the leg is ON, $S = 1$; otherwise $S = 0$.

Assuming that the energy losses in turn-on, turn-off of the transistor is denoted by E_{on} and E_{off}, respectively; and the diode reverse recovery energy losses is indicated by E_{rec}, the switching power losses of one leg of the three-phase inverter can be estimated as follows:

$$P_{sw,\mathrm{leg}} = f_s\,(E_{\mathrm{on}} + E_{\mathrm{off}} + E_{\mathrm{rec}}) \tag{10}$$

here, f_s is the switching frequency.

E_{on}, E_{off} and E_{rec} can either be obtained from the device datasheet or approximated by assuming a linear transition of voltage and current during switching.

Finally, the total power losses of the three-phase inverter can be calculated as follows:

$$P_{\mathrm{loss,inv}} = 3\,(P_{c,\mathrm{leg}} + P_{sw,\mathrm{leg}}) \tag{11}$$

In the proposed system, there are four additional switches in the auxiliary circuit which also contribute to the power losses. Two of these switches are in on-state simultaneously and their conduction power losses can be estimated as follows:

$$\begin{aligned} &P_{c,\mathrm{aux}} = \\ &\tfrac{1}{\pi}\textstyle\int_0^{\pi}\Big[HS\left(2^{\frac{1+\mathrm{sign}(i_{DC})}{2}}P_{c,T} + 2^{\frac{1-\mathrm{sign}(i_{DC})}{2}}P_{c,D}\right) + \\ &LS\,(P_{c,T} + P_{c,D})]\,d(\omega t) \end{aligned} \tag{12}$$

The equation above is derived based on the assumption that in the high-speed (HS) operating region, either two transistors (if $i_{DC} > 0$) or two diodes (if $i_{DC} < 0$) conduct simultaneously. In the low-speed (LS) operating region, regardless of the direction of the DC current, one transistor and one diode are conducting simultaneously.

Since the auxiliary circuit operates at the fundamental frequency, its switching power losses can be neglected. Therefore, the total power loss of the auxiliary circuit is equal to its conduction power loss.

Finally, the total power loss of the inverter can be written as follows:

$$P_{\mathrm{loss}} = P_{\mathrm{loss,inv}} + P_{c,\mathrm{aux}} \tag{13}$$

4.2. Power losses in the motor

The current harmonics in the motor can significantly increase its power losses. The harmonic model of the motor, presented in the previous section, is used to determine these current harmonics. Once the harmonic components are known, the power losses caused by them can be estimated. The power losses have four main components: stator and rotor copper losses, core losses, mechanical losses and stray losses. Here, only the electro-magnetic losses are analysed and the mechanical losses are not considered.

The RMS current of the motor considering the harmonics can be written as follows:

$$I_{\rm rms} = \sqrt{I_1^2 + I_5^2 + I_7^2 + \cdots} \tag{14}$$

Using Eq. (14), the stator copper losses can be obtained as:

$$P_{\rm Cu,s} = 3I_{\rm rms}^2 R_s = 3R_s \left(I_1^2 + \sum_{h=5,7,\ldots} I_h^2 \right) \tag{15}$$

The rotor copper losses can be approximated as follows:

$$P_{\rm Cu,r} \approx 3 \sum_{h=5,7,\ldots} I_h^2 R_r'(h) \tag{16}$$

where $R_r'(h)$ is rotor resistance at harmonic frequency $\times f_1$.

The harmonics severely affects the core losses in the motor. The core losses in presence of the harmonics can be estimated as:

$$P_{\rm core} \approx P_{\rm core,1} \left(1 + \sum_{h=5,7,\ldots} \left(\frac{I_h}{I_1} \right)^2 h^2 \right) \tag{17}$$

where $P_{core,1}$ denotes the core losses in the fundamental frequency and can be estimated as follows:

$$P_{\rm core,1} = k_f f_1 B_{\rm max}^{\alpha} + k_e f_1^2 B_{\rm max}^2 \tag{18}$$

It must be noted that the core loss above is per kg of the motor core weight.

Also, according to the IEEE std. 112, the stray losses of the motor can be approximately calculated by the following equation:

$$P_{\rm stray} \approx 0.005\, P_{\rm rated} \left(\frac{I_{\rm rms}}{I_{\rm rated}} \right)^2 \tag{19}$$

The equations above clearly show that current harmonics can significantly contribute to increased power losses in the motor. Using the proposed method, these harmonics are considerably reduced, and as a result, the motor's power losses are also decreased.

5. COMPARISONS

In 2, the comparison of the proposed drive with the conventional drive, the active PWM rectifier-based drive, and the DC-DC converter based drive is presented considering different key performance items. As the table indicates, although the auxiliary circuit in the proposed method increases the conduction power losses of the converter, the overall system power losses in the proposed method are lower in low-speed operation. The drives which employ DC-DC converter to adjust the DC-link voltage [25] are limited to low-power applications since the DC-DC converters cannot handle high power in practice. In this case, several DC-DC converters should be used in parallel which increases the cost and complexity of the system. As already mentioned, there are other drive structures that use the variable DC-link voltage concept [17, 18, 28]. However, their topology is based on other converters (rather than the conventional three-phase VSI), they are not included in the comparison table. They typically use versatile multilevel topologies with higher number of power-electronic switches and intended for medium-voltage (MV) high-power applications.

Considering the discussions, the proposed drive keeps a reasonable balance between the cost, complexity and performance of the system. Especially, the proposed method can be added to the conventional drive structure without bringing up considerable complexity and redesigning burden.

6. RESULTS AND DISCUSSIONS

To evaluate the proposed method for enhancing the performance of asynchronous motor drives in terms of output harmonics, simulation results obtained using MATLAB/SIMULINK are presented and discussed in this section. A 20 hp, 400 V, 50 Hz, four-pole motor with a rated speed of 1460 rpm is used for simulation studies. The motor parameters are set to the default values provided by the software. The drive is powered by a 400 V, 50 Hz, three-phase grid. The main control strategy of the drive is an open-loop constant V/f control, with the auxiliary circuit control—introduced in the previous sections—integrated into the system.

To design the DC-link capacitors, the following equation can be used:

$$\Delta V = \frac{P}{6 f C V_{DC}} \tag{20}$$

According to the equation above, the DC-link voltage ripples depend on the output power, and it is highest when the power is equal to its full-load value. Therefore, the capacitors should be designed for the full-load power. In this study, the criteria to design the capacitors is voltage ripples lower than %10. In the DC-link, two split capacitors are used, each with a capacitance of 4.7 mF. As the capacitors are in series, the equivalent DC-link capacitance is 2.35mF. In full-load condition ($P \cong 15kW$), is about 38V which is about %7 of the average DC-link voltage which accommodates the design criteria. However, in more sensitive applications this value for voltage ripples might not be acceptable. If lower voltage ripples are desired, the DC-link capacitance should be increased. Two other minor components of the voltage ripples should also be considered: voltage ripples caused by the equivalent series resistance (ESR) of the capacitor and the switching-frequency voltage ripples. Considering these voltage ripples components, the DC-link capacitors should be even higher than the calculated value in the previous equation. For example, for maximum %5 voltage ripples, each capacitor should be at least 6.6mF.

A simplified flowchart of the control implementation is shown in Fig. 4. As this figure indicates, based on the measurements and setpoints, it is decided whether to activate or not activate the auxiliary circuit. The main control of the motor remains unchanged and all the control methods including the constant V/f, vector control, and direct torque control (DTC) can be used.

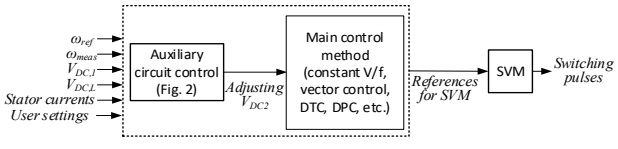


Fig. 4. The flowchart of implementation of the control method.

Table 2. Comparison of the proposed method with other variants.

Comparison criteria \ Method		Conventional drive Diode rectifier + inverter	Back-to-back drive Active rectifier + inverter	VSI + Buck Converter [25]	Proposed drive Diode rectifier + proposed inverter
Output current harmonics	Low-speed operation	High	Low	Low	Low
	High-speed operation	Low	Low	Low	Low
Number of IGBTs (excluding the brake circuit)		6	12	7	10
Total voltage rating of the IGBTs		$6V_{\mathrm{DC}}$	$12V_{\mathrm{DC}}$	$7V_{\mathrm{DC}}$	$8V_{\mathrm{DC}}$
Cost (normalized to the cost of the conventional drive)		1	1.5	1.25	1.25
Power losses in the converters (normalized to the losses of the conventional drive)	Nominal condition	1	1.5	1.5	1.3
	Low-speed condition	1	1.06	1.2	1.02
Power losses in the system (converters + motor)	Nominal condition	1	1.1	1.1	1.05
	Low-speed condition	1	0.93	0.90	0.93
Input current shaping capability		No	Yes	No	No

The pseudocode of the proposed method can be presented as follows:

Get: reference speed, measured speed, total V_{DC} before auxiliary circuit, V_{DC} of the lower capacitor after the auxiliary circuit, stator currents, settings
if (reference speed<0.5*rated speed):
Activate proposed method:
if ($V_{DC,L}$>0.5*$V_{DC,1}$+$\Delta V_{hysteresis}$):
Turn ON S_1 and S_3
else if ($V_{DC,L}$<0.5*$V_{DC,1}$-$\Delta V_{hysteresis}$)
Turn ON S_2 and S_4
else:
Keep previous switching states
else:
Activate conventional method:
Turn ON S_1 and S_4

Execute the main control loop

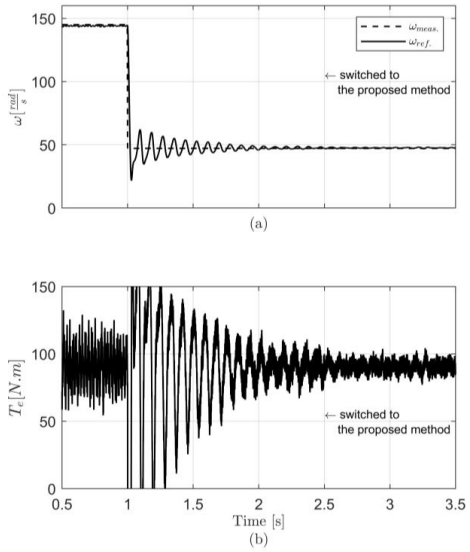


Fig. 5. (a) Reference and meausured speed in rad/s, (b) Electromagnetic torque developed by the motor.

6.1. Results for constant load torque and variable speed

The simulations are done in different conditions. In the first scenario the load applied is a constant torque of 90 N.m. The motor starts under load at a high speed of 145rad/s and then at t=1s its reference speed is reduced to 15π rad/s. In the high-speed range (up to t=1s in the simulations), the auxiliary circuit does not operate, and it has no effect on the drive performance. In the low-speed range, which starts at t=1s, up to t=2.5s the conventional method is used and in this time interval (t=1s to t=2.5s) the auxiliary circuit is still inactive. At t=2.5s in the low-speed range,

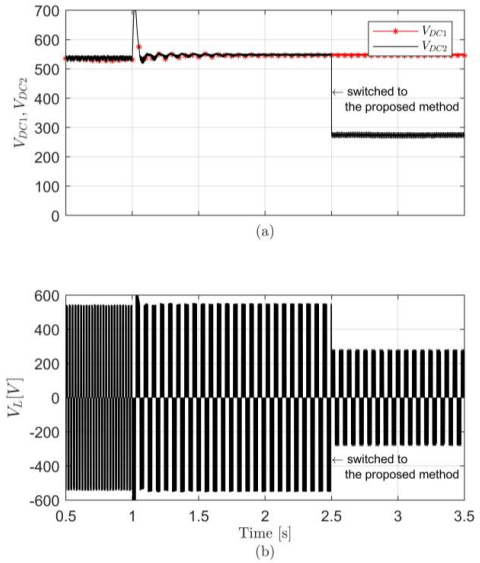


Fig. 6. (a) DC voltage before and after the auxiliary circuit, V_{DC1} and V_{DC2}, (b) Line to line voltage on the motor stator.

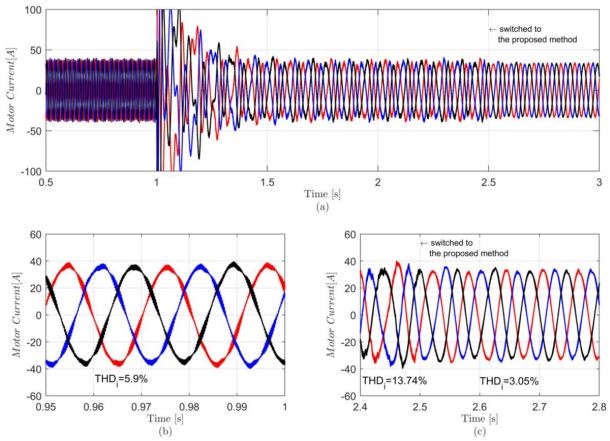


Fig. 7. Motor current, (a) Overall view, (b) Magnified view in high speed interval, (c) Magnified view in transition form the conventional method to the proposed method.

the proposed method is activated, and the auxiliary circuit plays its role to reduce the DC side voltage of the inverter, so the

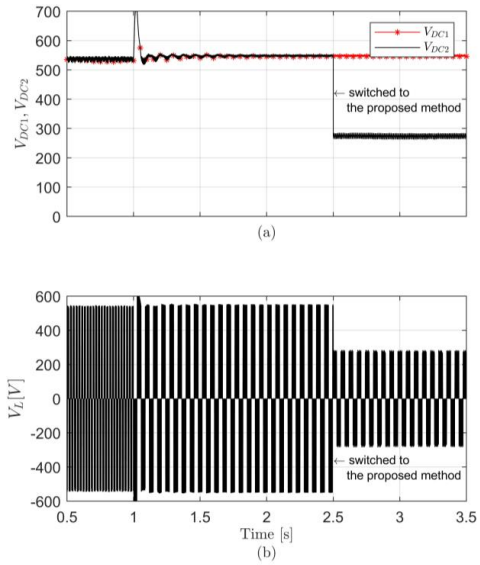


Fig. 8. Harmonic spectrum of the motor current in low-speed operation range, (a) Conventional method, (b) Proposed method, note that the fundamental frequency is 16.33Hz.

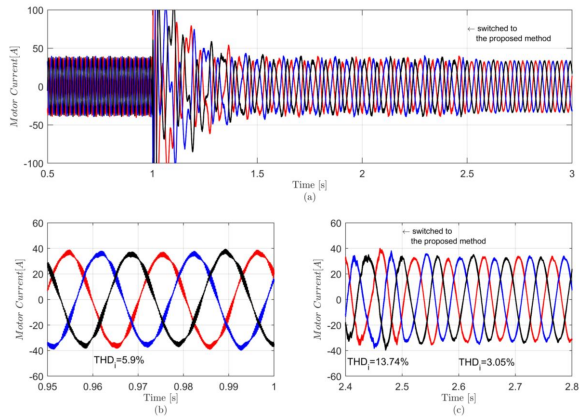


Fig. 9. The voltage on the lower and upper capacitors indicating their voltage balance.

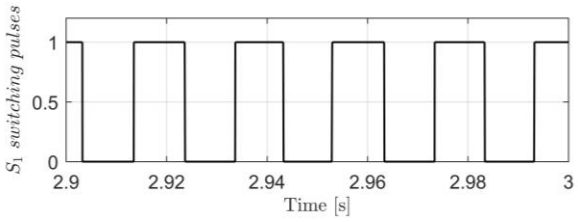


Fig. 10. The switching pulses of the switch S_1 in the auxiliary circuit.

modulation index is increased, and the quality of the output waveform is improved considerably.

Fig. 5 shows the motor speed and its electromagnetic torque. In Fig. 5-(a), the reference and the measured motor speed is shown. In both high speed and low speed range, the measured speed tracks its reference value. However, in the proposed method, the speed ripple is lower than conventional method, 2.1% compared to 3.15%. Also, the torque ripple (Fig. 5-(b)) of the proposed method is 9.7% while in the conventional method it is 12.15%.

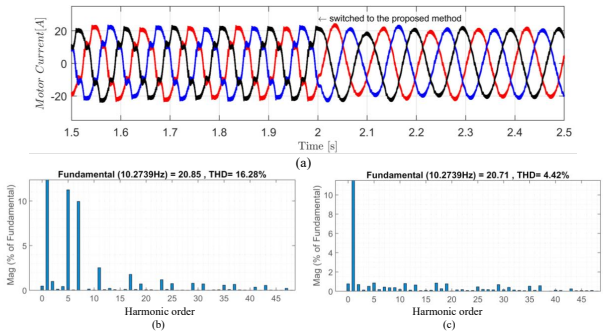


Fig. 11. Simulation results for speed-dependent torque, (a) Motor current, (b) Harmonic spectrum of the current in the conventional method, (c) Harmonic spectrum of the current in the proposed method.

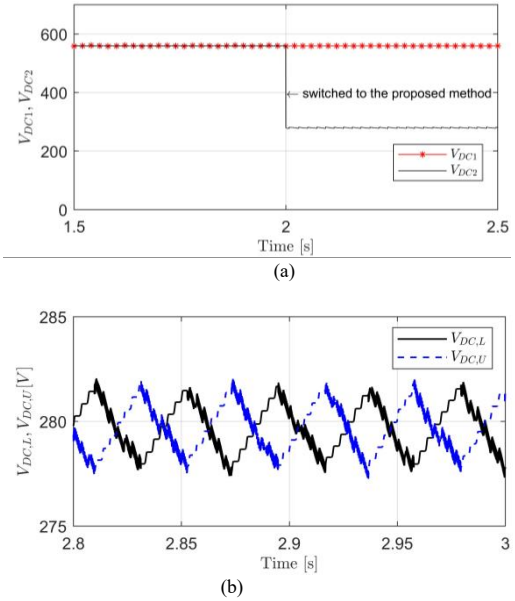


Fig. 12. (a) The DC-link voltage before and after the auxiliary circuit, (b) The upper and lower capacitor voltage indicating their voltage balance.

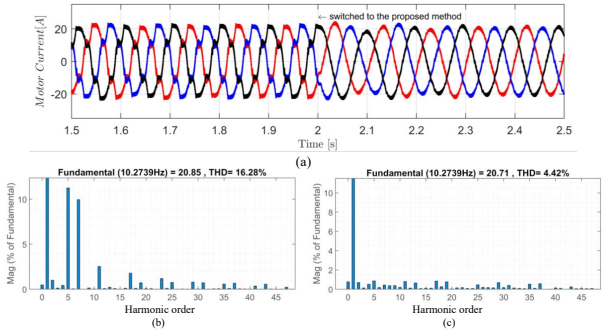
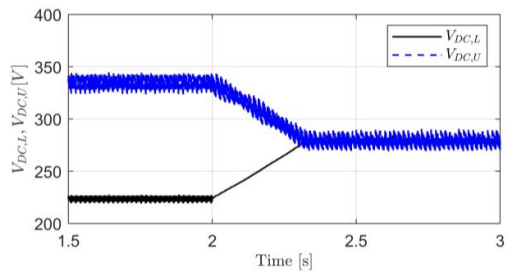
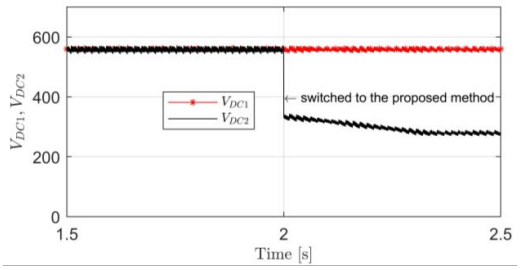


Fig. 13. (a) The reference and measured speed, (b) The electromagnetic torque of the motor.

Fig. 6 shows the DC-link voltage and the stator line to line voltage. In Fig. 6-(a), the DC-link voltage before and after the auxiliary circuit, V_{DC1} and V_{DC2}, respectively, are illustrated. As the figure indicates, up to t=2.5s, V_{DC1} and V_{DC2} are the same hence the auxiliary circuit is not working, and the DC-link voltage is not affected. At t=2.5s when it is switched to the proposed method, the auxiliary circuit starts working and adjusts V_{DC2}



(a)



(b)

Fig. 14. Simulation results to study the effcet of severly unequal capacitance and ESR of the DC-link capacitors, (a) voltage on the lower and upper capacitor, (c) sum of the voltage on the lower and upper capacitor V_{DC1} and the DC-link voltage after the auxiliary circuit (V_{DC2}).

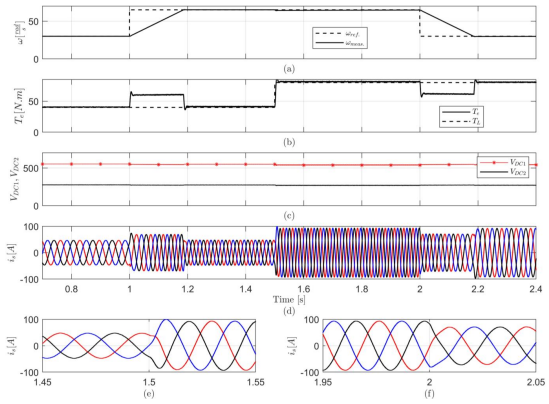


Fig. 15. Simulation results for FOC, (a) Reference and measured speed (rad/s), (b) Load torque (T_L) and motor electromagnetic torque (T_e), (c) DC-link voltage before and after the auxiliary circuit, (d) Motor current, (e) Motor current in 1.45<t<1.55, (f) Motor current in 1.95<t<2.05.

to $0.5V_{DC1}$. By adjusting the DC input voltage of the inverter, its modulation index increases resulting in higher quality of the output voltage and current. Fig. 6-(b) shows the stator line voltage (one of three line-voltages). As this figure indicates, the line voltage changes obviously according to the DC voltage change when the method is witched to the proposed method. In this way, the line voltage is synthesized by voltage pulses with lower magnitude but higher pulse width. Therefore, its harmonic contents are lower in the proposed method. Its THD in the conventional and the proposed method is 121% and 72%, respectively, proving substantial improvement of the waveform quality in the proposed method. It should be noted that for calculating the THD values the high-order harmonics (up to two times the switching frequency) are also considered.

The motor three-phase current is shown in Fig. 7. The overall view of the motor current is shown in Fig. 7-(a) which indicates the transition from the high speed, characterized by the higher frequency of the current, to the low speed at t=1s and transition from the conventional method to the proposed method at t=2.5s. To have a better sight, the magnified view of the current before turning to the low speed is shown in Fig. 7-(b). The THD of the current in this interval is 5.9%. Also, a magnified view of the motor current around t=2.5s, the instant of transition from the conventional method to the proposed method, is shown in Fig. 7-(c). This figure indicates considerable improvement in the current quality in the proposed method in comparison with the conventional method. The THD of the current in the conventional method is 13.74% while it is dramatically reduced to 3.05% in the proposed method.

Fig. 8 indicates the harmonic spectrum of the motor current in the low-speed range for both conventional method (Fig. 8(a)) and the proposed method (Fig. 8-(b)). As the figure illustrates, in the proposed method, the low-order harmonics of the current are significantly lower than those of the conventional method. In the proposed method, the magnitude of the low-order harmonics is lower than 1%, however, in the conventional method the magnitude of a specific low-order harmonics is as high as 12%. These low-order harmonics significantly affect the motor operation, power losses, torque and speed ripples.

In order to indicate the capacitors' voltage balancing using the auxiliary circuit in the proposed method, their voltage are shown in Fig. 9. As this figure illustrates, the capacitos' voltage are balanced. The voltage ripple of the capacitors' voltage is 20V exactly the same as the value used in the hysteresis control of the voltage shown in Fig. 2. If lower voltage ripple is desired, the hysteresis band could be reduced. However, this will increase the switching frequency of the auxiliary circuit.

Fig. 10 indicates the switching pulses of the switch S_1 in the auxiliary circuit. As mentioned before, the switches of the auxiliary circuit operate in a very low switching frequency. With the hystersis band of 20V, the switching frequency of S_1 (the same as for the other switches of the auxiliary circuit) is almost 50Hz. This low switching frequency of the auxiliary circuit results in negligible switching power losses of the auxiliary circuit and also inexpensive switches could be used.

During low-speed operation, the conduction power losses of both the three-phase inverter and the auxiliary circuit remain relatively low, approximately 0.41% and 0.58%, respectively. Under the same operating conditions, the conduction loss of the rectifier is around 0.3%. Regarding switching losses, the conventional method results in approximately 1.1% switching power loss in the inverter, whereas the proposed method reduces this to about 0.55%. This reduction is primarily attributed to the halving of the DC-link voltage across the switching devices in the proposed approach, which directly impacts the switching energy per cycle and thus lowers the overall switching losses.

Consequently, the total power losses in the conventional and proposed drive systems are approximately 1.81% and 1.84%, respectively, indicating a negligible difference. For comparison, the total power losses in a drive system based on an active front-end rectifier are slightly higher, around 1.92%. On a broader scale, when considering the entire system, the power losses in the conventional and proposed methods are 17.8% and 16.4%, respectively. This notable reduction in total losses demonstrates that the proposed method achieves higher overall system efficiency under low-speed operating conditions.

6.2. Results for variable load torque and variable speed

Another simulation is done assuming more practical load in which the load torque is not constant anymore, but it varies depending on the motor speed as $T = 0.004\omega_m^2 + 6$. The constants in this formula are determined in a way that the torque does not exceed the nominal torque of the motor in nominal condition. To avoid replication, the results are indicated only in low-speed

operation. In this simulation case study, the motor starts with the conventional method with the reference speed of 10π rad/s. At t=2s, the proposed method is activated. Fig. 11-(a) shows the motor current which clearly indicates the improvement in the current quality when the proposed method is activated at the same operation condition. Fig. 11-(b) and Fig. 11-(c) indicate the harmonic spectrum of the motor current in the conventional and the proposed method, respectively. As it is obvious, the current harmonics in the proposed method are dramatically lower than those of the conventional method.

Fig. 12 shows the DC-link voltage before and after the auxiliary circuit. As shown in Fig. 12-(a), up to t=2s, as the proposed method was not activated yet, the DC-link voltage before and after the auxiliary circuit are the same. At t=2s the proposed method is activated and the DC-link voltage after the auxiliary circuit is halved resulting in higher modulation index and higher output waveform quality. Fig. 12-(b) indicates the upper and lower capacitors' voltage balancing. In this case study, the hysteresis band of the voltage balancing control was set to 2V. As the results indicate, the capacitors voltage balance is maintained with a very low voltage ripple.

Fig. 13 shows the speed and torque of the motor. In Fig. 13-(a) the reference and measured speed are indicated. Also, the electromagnetic torque of the motor is shown in Fig. 13-(b). These results clearly indicate that the speed and torque ripples are reduced considerably when the proposed method is activated. Moreover, the torque waveform indicates that the load torque indicates that the load torque depends on the speed and is not constant, as in the previous simulation case study.

The power loss analysis given in the previous section is used to calculate power losses in the drive and motor. In the full-load operation at rated speed, the conduction power losses in the three-phase inverter and the auxiliary circuit are %0.41 and %0.58, respectively. Also, the conduction power loss in the rectifier is about %0.4. The switching power losses of the inverter are %1.1. Therefore, in this condition, with and without the auxiliary circuit, the total power losses are %2.49 and %1.91, respectively. On the other hand, if the active front-end rectifier is used instead of the proposed method for adjusting the DC-link voltage, the total power losses of the converter would be %3.02. In other words, both methods of adjusting the DC-link voltage result in higher power losses in the drive, however, the power losses in the proposed method are lower that of the method in which the active front-end rectifier is used for adjusting the DC-link voltage. In this condition, the total power losses in the motor (including the copper and iron losses) are %9.3.

6.3. Results for uuequal DC capacitors

To investigate the effect of the practical aspects regarding the capacitance and the equivalent series resistance (ESR) of the DC-link capacitors on the drive performance, a simulation is done in which the capacitance and ESR of the upper capacitor is 0.5Ω and 3.76mF (-%20 tolerance), respectively. For the lower capacitor, the ESR and the capacitance are 0.2Ω and 5.64mF (+%20 tolerance). These unbalanced capacitances and ESRs will affect the drive performance. Fig. 14-(a) shows the voltage on the lower and upper capacitors. Up to t=2s, the proposed method is not activated and there is no voltage balancing control and hence the average DC voltage as well as the voltage ripples on the lower and upper capacitors are different due to different capacitance and ESR. However, this would not affect the drive performance considerably because in the conventional method the drive is using the total DC-link voltage which is indicated in Fig. 14-(b) denoted by V_{DC1}. However, as the voltage ripples increase due to higher ESR, this will increase the output current harmonic slightly. As the results indicate, at t=2s, the proposed method is activated, and the voltage balancing is started and within a specific time the capacitors' voltage is fully balanced.

6.4. Results for Field-Oriented Control (FOC)

The performance of the proposed drive system is examined using the FOC. In this case study, the same motor is controlled with the FOC and a speed control loop is added. For this study the step changes in the load torque and in the reference speed are applied. The simulation results for this case study are shown in Fig. 15. It is important to note that the simulation results in this case study are shown only for the proposed method. In Fig. 15-(a) the reference and measured speed are shown. As the figure indicates the reference speed has two step-changes; first at t=1s changes from 30rad/s to 65rad/s and then the second at t=2 changes from 65rad/s to 30rad/s. In Fig. 15-(b) the load torque (T_L) and the motor electromagnetic torque (T_e) are indicated. According to the figure, the load torque has a step change in t=1.5s which changes from 40N.m to 80N.m. The motor electromagnetic torque responds to the load torque change as well as acceleration and deceleration of the motor. Fig. 15-(c) shows the DC-link voltage before and after the auxiliary circuit indication that the proposed method is active and adjusts the DC-link voltage. Figs. 15-(d-e) shows the motor current. As the waveforms indicate, the motor current has high quality due to the high-performance FOC and the proposed method.

7. CONCLUSION

A simple and practical method was proposed in this paper to enhance the performance of asynchronous motor drives. This approach involves appending a low-cost auxiliary circuit to the main drive circuit. The performance of the proposed drive system was evaluated through simulation studies. According to the results, implementing the proposed method significantly improves drive performance in the low-speed operating range. Specifically, the harmonic content of the output voltage and current was substantially reduced. For example, the total harmonic distortion (THD) of the motor current decreased from 13.74% in the conventional method to 3.05% with the proposed method—representing a reduction of approximately 77%. Additionally, speed and torque ripples were reduced compared to the conventional approach. The auxiliary circuit is controlled in such a way that it also ensures voltage balance across the capacitors. It is worth noting that the auxiliary circuit operates at a very low switching frequency—50 Hz in the case study—and the reverse voltage across its switches is only half of the DC-link voltage, making the added circuit cost-effective. A power loss analysis in both the motor and converters is presented and compared for the proposed and the conventional system. The results indicate that the power losses of the system are almost equal for the proposed and the conventional drive in high-speed operation. In low-speed operation, the power losses of the proposed system are lower than the conventional method. This is due to the lower harmonic core losses in the proposed method.

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