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# Performance Improvement of Single-Phase Transformer less Grid-Connected PV Inverters Regarding the CMV and LVRT

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***Abstract-*** *The single-phase transformerless grid-connected photovoltaic (PV) systems, mainly the low-power single-phase systems, requires high efficiency, small size, lightweight, and low-cost grid-connected inverters. However, problems such as leakage current, the DC current injection and safety issues are incorporated with transformerless grid-connected PV inverters. Besides, the new standards such as low-voltage ride-through (LVRT) capability and staying connected to the grid during the fault occurrence should be considered for the next generation of transformerless PV inverters. In this paper, a study is going underway on the LVRT capability and the Common-Mode Voltage (CMV) in a number of most common transformerless grid-connected PV inverters. In fact, by a comprehensive study on all possible switching combinations and the current paths during the freewheeling period of the selected inverters, the proposed control strategy for performance improvement of the PV inverters under the normal and the LVRT conditions is presented. As a matter of fact, a reconfigurable PWM method is proposed, which makes it possible to switch between two PWM methods and hence provide improved performance of the inverters in the LVRT condition. Finally, the results of simulations in the normal and the LVRT operations to verify the theoretical concepts are indicated.*

***Keyword:*** Single-phase transformerless grid-connected photovoltaic systems, Leakage current, LVRT capability, Common-mode voltage.

## 1. INTRODUCTION

Energy from renewable sources is becoming a common interest of research due to the rapid increase of energy demand and the exhaustion of global resources. Among renewable power sources, photovoltaic (PV) energy source is known as one of the great alternatives all over the world due to the inexhaustible and pollution-free nature of solar power [1-3]. PV systems can be classified into the transformerless and with the transformer. The transformerless configuration for PV systems is developed to offer the advantages of high efficiency, high power density, and low cost [4, 5]. Unfortunately, there are some issues because a galvanic isolation between the grid and the PV array does not exist in the transformerless systems. Besides, due to the presence of parasitic capacitor between the PV panel and the ground, the leakage current will be appeared. The common-mode leakage current increases the system losses, reduces the grid-connected current quality, induces the severe conducted, radiated electromagnetic interference (EMI), and causes to intensify personnel safety problems. Hence, the leakage current minimization is one of the most important considerations in transformerless PV inverters. In order to eliminate the leakage current in transformerless PV systems, many research works on transformerless PV inverters have been done. Also, many solutions have recently been presented [6-10]. The solutions can be classified into modulation based solutions and structure based solutions. In Ref. [6], an improved modulation to keep the CMV constant for the leakage current reduction is presented. In Ref. [7], the reason why the typical single-phase cascaded H-Bridge inverter fails to reduce the leakage current is explained and new modulation strategy to reduce the leakage current is presented. In Ref. [8], the authors proposed space vector modulation (SVM) to eliminate leakage current for neutral point clamped inverters. The methods mentioned are in the case of the modulation based solution. On the other hand, another method for eliminating the leakage current is the topology based solution. Hence, many topologies such as H5 in Ref. [9], oH5 in Ref. [10], H6 family [11-14], and HERIC in Ref. [15] are presented to prevent the leakage current flows by DC-decoupling and AC-decoupling to disconnect the PV

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***Research Paper***

and the grid. In [16-18], the papers propose to eliminate the leakage current via galvanic isolation and CMV clamping techniques. Until a few years ago, the highlights were issues with transformerless PV systems. But, today, PV systems are largely and widely penetrated into the utility grid. Therefore, this high penetration level of PV systems may also introduce negative impacts on the grid. Thus, many standards and requirements (such as low voltage ride through, anti-islanding protection, …) have been released to regulate PV systems integration with the distribution grid [19-24]. According to the new standards, the future generation PV systems should be able to provide a full range of services similar to what conventional power plants do at present. As a matter of fact, it is expected that the future PV inverters will be more active and smart with the functionalities of LVRT capability and grid support. For example, when a grid fault (voltage drop, …) is detected, the PV system enters into the LVRT operation. It is required by the grid codes that the system should withstand the voltage drop for a specified short period, as it is presented in some grid codes [19-22], at the same time, the PV system should inject reactive power to support the grid voltage recovery. If those above aspects are not well considered, the maintenance costs and energy losses may increase. Thus, it is necessary to explore the performance of the single-phase transformerless grid-connected PV inverters under different conditions. In Ref [22], the authors focused on the control of some transformerless PV systems under grid faults. Then control strategies and reactive power injection possibilities for some single-phase PV systems are discussed. However, under LVRT condition some of the selected inverters cannot provide reactive power. Also, the grid current of the inverters is severely distorted at voltage zero-crossing points. In Ref [24], during LVRT operation, the PWM is switched from unipolar modulation to bipolar modulation. Therefore, switching losses due to higher voltage variation and the higher current ripple reduced efficiency. In this paper, several transformerless PV inverters such as H-Bridge (bipolar and unipolar modulation), H5, H6D1, H6D2, HERIC and H8 [25] are studied in terms of CMV, leakage current elimination, current path during freewheeling period, and LVRT capability with reactive power injection. Then, the proposed control strategy for performance improvement of these inverters in LVRT and normal operations is presented. In fact, the control system provides LVRT capability for all of the mentioned inverters by a unit of reconfigurable PWM, which makes it possible to switch between two PWM methods. The first PWM is for the normal condition and another is for LVRT condition. Furthermore, by the suitable PWM, the CMV remains constant therefore the leakage current will be reduced or eliminated.

This paper is organized as follows: in section 2, a general overview of all switching combinations of mentioned inverters and the reactive power injection possibilities for single-phase transformerless grid-connected PV inverters are discussed. The proposed control strategy is presented in next section (section 3). In section 4, the simulation results of the mentioned inverters performance under the LVRT condition and the normal condition are presented. Summarizes the conclusions drawn from the investigation in section 5.

## 2. SINGLE-PHASE TRANSFORMERLESS GRID-CONNECTED PV INVERTERS

Single-phase transformerless grid-connected PV inverters that in this paper discussed are presented in Fig. 1. This section organized into two parts. The first part has an overall study over the switching combinations of these inverters and emphasizes on CMV in the switching combinations. Part two studies the current path during the freewheeling period and reactive power injection possibilities for every single inverter. The definition of CMV and differential-mode voltage (DMV) can be helpful to better understand the discussion.

$$V_{CMV} = (V_{An} + V_{Bn})/2 \quad (1)$$

$$V_{DMV} = V_{An} - V_{Bn} \quad (2)$$

Where, $V_{An}$ and $V_{Bn}$ are the pulse voltage between the bridge midpoint and the DC bus negative terminal, respectively. With no filter, leakage current only depends on the variations of the inverter CMV and can be expressed as follows:

$$I_{Leak} = C\frac{dV_{CMV}}{dt} \quad (3)$$

According to Eq. (3), in order to avoid leakage currents, the CMV must be kept constant.

### 2.1. Overview of Switching Combinations of Transformerless PV Inverters

Fig. 1 shows the single-phase grid-connected PV systems based on the different topology of transformerless inverters. Fig. 1(a) to Fig. 1(f) shows the H-Bridge, H5, H6D1, H6D2, HERIC and H8 inverters based PV system, respectively. Table 1 presents the switching combinations of the H-Bridge inverter in the unipolar modulation. According to this table, eight switching combinations are available for this inverter in the unipolar modulation, six for the zero output voltage, one for the positive output voltage and one other for the negative output voltage. As indicated in Table 1, the switching combinations which provide zero output voltage have the CMV different from the other switching combinations.

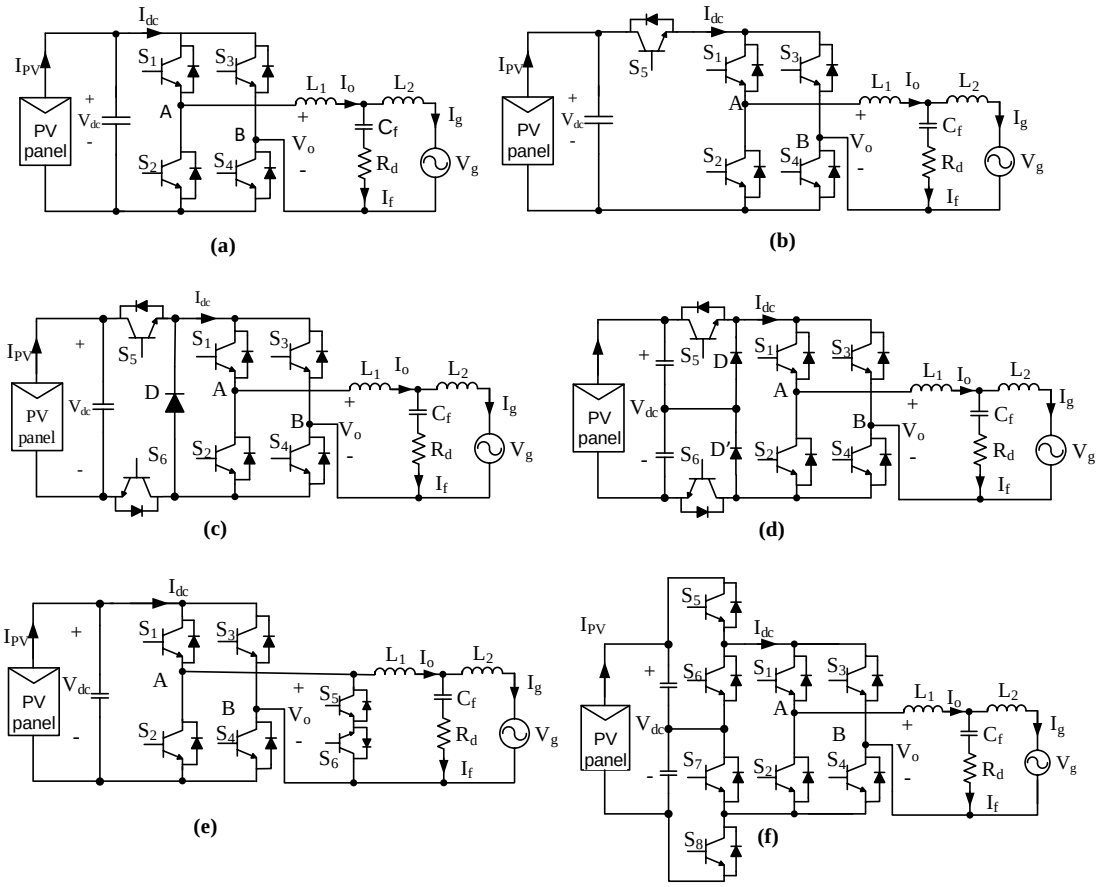


**Fig. 1. The single-phase transformerless grid-connected PV inverters with an LCL filter:(a) H-Bridge, (b) H5, (c)H6D1, (d) H6D2, (e) HERIC, (f) H8.**

**Table 1. Switching combinations for H-Bridge inverter with unipolar modulation.**

| No. | ON switches | Device in current path | | $V_{An}$ | $V_{Bn}$ | $V_{CMV}$ | $V_o$ |
|---|---|---|---|---|---|---|---|
| 1 | $S_1, S_4$ | $S_1, S_4$ | | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 2 | $S_2, S_3$ | $S_2, S_3$ | | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| 3 | $S_1, S_3$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| 4 | $S_2, S_4$ | $I_o > 0$ | $D_2, S_4$ | 0 | 0 | 0 | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 5 | $S_1$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| | | $I_o < 0$ | $D_1, D_4$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 6 | $S_3$ | $I_o > 0$ | $D_3, D_2$ | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| | | $I_o < 0$ | $S_3, D_1$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| 7 | $S_2$ | $I_o > 0$ | $D_2, D_3$ | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| | | $I_o < 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 8 | $S_4$ | $I_o > 0$ | $S_4, D_2$ | 0 | 0 | 0 | 0 |
| | | $I_o < 0$ | $D_4, D_1$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |

In order to have constant CMV, this is a key feature for transformerless PV inverters; the zero voltage level should not be used. Therefore, the H-Bridge inverter with bipolar modulation is used resulting in a two-level inverter. Table 2 indicates switching combinations of the bipolar modulation. According to this table, the CMV is constant in these two combinations. Therefore, there will be no leakage current according to Eq. (3). Fig. 1(b) shows the structure of the H5 inverter. As can be seen, this structure is based on H-Bridge family. The purpose is to add a switch to the H-Bridge structure to prevent the exchange of reactive power between the DC-link capacitor and the inductors of the filter and separating the grid-connected inverter from the DC source at the zero voltage levels, which has a great effect on limiting the leakage current. All of the possible switching combinations for the H5 inverter is presented in Table 3.

**Table 2. Switching combinations for H-Bridge inverter with bipolar modulation.**

| No. | ON switches | $V_{An}$ | $V_{Bn}$ | $V_{CMV}$ | $V_o$ |
|---|---|---|---|---|---|
| 1 | $S_1, S_4$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 2 | $S_2, S_3$ | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |

In five of the switching combinations (No. 1, 2, 3 and 7, 8), the value of the CMV is equal to $V_{dc}/2$ and others are 0 or $V_{dc}$ .

**Table 3. Switching combinations for the H5 inverter.**

| No. | ON switches | Device in current path | | $V_{An}$ | $V_{Bn}$ | $V_{CMV}$ | $V_o$ |
|---|---|---|---|---|---|---|---|
| 1 | $S_1, S_4, S_5$ | $S_1, S_4, S_5$ | | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 2 | $S_2, S_3, S_5$ | $S_2, S_3, S_5$ | | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| 3 | $S_1, S_3$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 4 | $S_2, S_4$ | $I_o > 0$ | $D_2, S_4$ | 0 | 0 | 0 | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 5 | $S_2$ | $I_o > 0$ | $D_3, D_5, D_2$ | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| | | $I_o < 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 6 | $S_4$ | $I_o > 0$ | $S_4, D_2$ | 0 | 0 | 0 | 0 |
| | | $I_o < 0$ | $D_1, D_5, D_4$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 7 | $S_1$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_1, D_5, D_4$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 8 | $S_3$ | $I_o > 0$ | $D_3, D_5, D_2$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $-V_{dc}$ |
| | | $I_o < 0$ | $S_3, D_1$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |

**Table 4. Switching combinations for the H6D1 inverter.**

| No. | ON switches | Device in current path | | $V_{An}$ | $V_{Bn}$ | $V_{CMV}$ | $V_o$ |
|---|---|---|---|---|---|---|---|
| 1 | $S_1, S_3$ | $I_o > 0$ | $S_1, D_3$ | $2V_{dc}/3$ | $2V_{dc}/3$ | $2V_{dc}/3$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $2V_{dc}/3$ | $2V_{dc}/3$ | $2V_{dc}/3$ | 0 |
| 2 | $S_1, S_3, S_6$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 3 | $S_1, S_3, S_5$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 4 | $S_1, S_3, S_5, S_6$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| 5 | $S_2, S_4$ | $I_o > 0$ | $D_2, S_4$ | $V_{dc}/3$ | $V_{dc}/3$ | $V_{dc}/3$ | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | $V_{dc}/3$ | $V_{dc}/3$ | $V_{dc}/3$ | 0 |
| 6 | $S_2, S_4, S_5$ | $I_o > 0$ | $D_2, S_4$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 7 | $S_2, S_4, S_6$ | $I_o > 0$ | $D_2, S_4$ | 0 | 0 | 0 | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 8 | $S_2, S_4, S_5, S_6$ | $I_o > 0$ | $D_2, S_4$ | 0 | 0 | 0 | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 9 | $S_1, S_4$ | $I_o > 0$ | $S_1, S_4, D$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_1, D_5, D_6, D_4$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 10 | $S_1, S_4, S_5, S_6$ | $S_1, S_4, S_5, S_6$ | | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 11 | $S_2, S_3$ | $I_o > 0$ | $D_2, D_3, D_5, D_6$ | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| | | $I_o < 0$ | $S_2, S_3, D$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 12 | $S_2, S_3, S_5, S_6$ | $S_2, S_3, S_5, S_6$ | | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |

Fig. 1(c) shows the H6D1 inverter structure. Adding a diode to the H6 inverter structure will increase the efficiency and provide the proper conditions in modulation to generate a constant CMV (Table 4). As a result, there is a decrease in the leakage current. By using the switches $S_5$ and $S_6$ in the zero voltage states, the PV module can be separated from the grid. This would prevent any exchange of reactive power between the DC-link capacitor and filter inductors and would also decrease the leakage current.

Fig. 1(d) shows the improved grid-connected inverter topology, which can meet the condition of eliminating common-mode leakage current. This topology has the ability to provide three-level and 5-level output voltage.

**Table 5. Switching combinations for the H6D2 inverter.**

| No. | ON switches | Device in current path | | $V_{An}$ | $V_{Bn}$ | $V_{CMV}$ | $V_o$ |
|---|---|---|---|---|---|---|---|
| 1 | $S_1, S_3$ | $I_o > 0$ | $S_1, D_3$ | $3V_{dc}/4$ | $3V_{dc}/4$ | $3V_{dc}/4$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $3V_{dc}/4$ | $3V_{dc}/4$ | $3V_{dc}/4$ | 0 |
| 2 | $S_1, S_3, S_6$ | $I_o > 0$ | $S_1, D_3$ | $3V_{dc}/4$ | $3V_{dc}/4$ | $3V_{dc}/4$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $3V_{dc}/4$ | $3V_{dc}/4$ | $3V_{dc}/4$ | 0 |
| 3 | $S_1, S_3, S_5$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| 4 | $S_1, S_3, S_5, S_6$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| 5 | $S_2, S_4$ | $I_o > 0$ | $D_2, S_4$ | $V_{dc}/4$ | $V_{dc}/4$ | $V_{dc}/4$ | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | $V_{dc}/4$ | $V_{dc}/4$ | $V_{dc}/4$ | 0 |
| 6 | $S_2, S_4, S_5$ | $I_o > 0$ | $D_2, S_4$ | $V_{dc}/4$ | $V_{dc}/4$ | $V_{dc}/4$ | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | $V_{dc}/4$ | $V_{dc}/4$ | $V_{dc}/4$ | 0 |
| 7 | $S_2, S_4, S_6$ | $I_o > 0$ | $D_2, S_4$ | 0 | 0 | 0 | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 8 | $S_2, S_4, S_5, S_6$ | $I_o > 0$ | $D_2, S_4$ | 0 | 0 | 0 | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 9 | $S_1, S_4$ | $I_o > 0$ | $S_1, S_4, D, D'$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_1, D_4, D_5, D$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 10 | $S_1, S_4, S_5$ | $I_o > 0$ | $S_1, S_4, S_5, D$ | $V_{dc}$ | $V_{dc}/2$ | $3V_{dc}/4$ | $V_{dc}/2$ |
| | | $I_o < 0$ | $D_1, D_5, D_6, D$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 11 | $S_1, S_4, S_6$ | $I_o > 0$ | $S_1, S_4, S_6, D$ | $V_{dc}/2$ | 0 | $V_{dc}/4$ | $V_{dc}/2$ |
| | | $I_o < 0$ | $D_1, D_5, D_6, D$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 12 | $S_1, S_4, S_5, S_6$ | $S_1, S_4, S_5, S_6$ | | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 13 | $S_2, S_3$ | $I_o > 0$ | $D_2, D_3, D_5, D$ | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| | | $I_o < 0$ | $S_2, S_3, D, D'$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 14 | $S_2, S_3, S_5$ | $I_o > 0$ | $D_2, D_3, D_5, D$ | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| | | $I_o < 0$ | $S_2, S_3, S_5, D$ | $V_{dc}/2$ | $V_{dc}$ | $3V_{dc}/4$ | $-V_{dc}/2$ |
| 15 | $S_2, S_3, S_6$ | $I_o > 0$ | $D_2, D_3, D_5, D$ | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| | | $I_o < 0$ | $S_2, S_3, S_6, D$ | 0 | $V_{dc}/2$ | $V_{dc}/4$ | $-V_{dc}/2$ |
| 16 | $S_2, S_3, S_5, S_6$ | $S_2, S_3, S_5, S_6$ | | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |

Two additional diodes $D$ and $D'$ are added to the H6 inverter, and half of the DC bus voltage is applied across the DC bus IGBTs and free-wheeling diodes. Therefore, it causes the midpoint to be balanced. This change in the structure of the H6 inverter has had a more suitable performance in satisfying key factors for the transformerless grid-connected inverters. All the possible

switching combinations of the H6D2 inverter are presented in Table 5. Compared to other inverters, this inverter has the most number of the switching combinations. In Fig. 1(e), a new modification to the H-Bridge inverter is indicated, called Highly Efficient Reliable Inverter Concept (HERIC) which is being commercialized by the Sunways company. A bypass branch has been added to the H-Bridge in the AC side with two IGBTs with freewheeling diodes. The AC bypass provides the same two vital functions as the fifth switch in case of the H5 topology. First, prevents the reactive power exchange between filter inductors and DC-link capacitor during the zero voltage state. According to the mentioned fact and taking into account that the IGBTs ($S_5$ and $S_6$) operate in fundamental frequency, therefore, efficiency is increased. Second, isolates the PV from the grid during the zero voltage states, thus eliminating the leakage current.

**Table 6. Switching combinations for the HERIC inverter.**

| No. | ON switches | Device in current path | | $V_{An}$ | $V_{Bn}$ | $V_{CMV}$ | $V_o$ |
|---|---|---|---|---|---|---|---|
| 1 | $S_5, S_6$ | $I_o > 0$ | $D_5, S_6$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $S_5, D_6$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 2 | $S_6$ | $I_o > 0$ | $D_5, S_6$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_1, D_4$ | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 3 | $S_5$ | $I_o > 0$ | $D_6, S_5$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_2, D_3$ | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| 4 | $S_1, S_4, S_6$ | $S_1, S_4$ | | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 5 | $S_1, S_4$ | $S_1, S_4$ | | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 6 | $S_2, S_3, S_5$ | $S_2, S_3$ | | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |
| 7 | $S_2, S_3$ | $S_2, S_3$ | | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |

**Table 7. Switching combinations for the H8 inverter (5-Level).**

| No. | ON switches | Device in current path | | $V_{An}$ | $V_{Bn}$ | $V_{CMV}$ | $V_o$ |
|---|---|---|---|---|---|---|---|
| 1 | $S_1, S_4, S_6, S_7$ | $I_o > 0$ | $S_1, S_4, D_6, D_7$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_1, D_4, S_6, S_7$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 2 | $S_2, S_3, S_6, S_7$ | $I_o > 0$ | $D_2, D_3, S_6, S_7$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $S_2, S_3, D_6, D_7$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 3 | $S_1, S_3, S_6, S_7$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 4 | $S_1, S_3, S_5, S_7$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| 5 | $S_1, S_3, S_5, S_8$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| | | $I_o < 0$ | $D_1, S_3$ | $V_{dc}$ | $V_{dc}$ | $V_{dc}$ | 0 |
| 6 | $S_1, S_3, S_6, S_8$ | $I_o > 0$ | $S_1, D_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o > 0$ | $D_1, S_3$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 7 | $S_2, S_4, S_6, S_7$ | $I_o > 0$ | $D_2, S_4$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 8 | $S_2, S_4, S_5, S_7$ | $I_o > 0$ | $D_2, S_4$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | $V_{dc}/2$ | $V_{dc}/2$ | $V_{dc}/2$ | 0 |
| 9 | $S_2, S_4, S_5, S_8$ | $I_o > 0$ | $D_2, S_4$ | 0 | 0 | 0 | 0 |
| | | $I_o > 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 10 | $S_2, S_4, S_6, S_8$ | $I_o > 0$ | $D_2, S_4$ | 0 | 0 | 0 | 0 |
| | | $I_o < 0$ | $S_2, D_4$ | 0 | 0 | 0 | 0 |
| 11 | $S_1, S_4, S_5, S_7$ | $I_o > 0$ | $S_1, S_4, S_5, D_7$ | $V_{dc}$ | $V_{dc}/2$ | $3V_{dc}/4$ | $V_{dc}/2$ |
| | | $I_o < 0$ | $D_1, D_4, D_5, S_7$ | $V_{dc}$ | $V_{dc}/2$ | $3V_{dc}/4$ | $V_{dc}/2$ |
| 12 | $S_1, S_4, S_6, S_8$ | $I_o > 0$ | $S_1, S_4, D_6, S_8$ | $V_{dc}/2$ | 0 | $V_{dc}/4$ | $V_{dc}/2$ |
| | | $I_o < 0$ | $D_1, D_4, S_6, D_8$ | $V_{dc}/2$ | 0 | $V_{dc}/4$ | $V_{dc}/2$ |
| 13 | $S_2, S_3, S_5, S_7$ | $I_o > 0$ | $S_2, S_3, S_5, D_7$ | $V_{dc}/2$ | $V_{dc}$ | $3V_{dc}/4$ | $-V_{dc}/2$ |
| | | $I_o < 0$ | $D_2, D_3, D_5, S_7$ | $V_{dc}/2$ | $V_{dc}$ | $3V_{dc}/4$ | $-V_{dc}/2$ |
| 14 | $S_2, S_3, S_6, S_8$ | $I_o > 0$ | $S_2, S_3, D_6, S_8$ | 0 | $V_{dc}/2$ | $V_{dc}/4$ | $-V_{dc}/2$ |
| | | $I_o < 0$ | $D_2, D_3, S_6, D_8$ | 0 | $V_{dc}/2$ | $V_{dc}/4$ | $-V_{dc}/2$ |
| 15 | $S_1, S_4, S_5, S_8$ | $S_1, S_4, S_5, S_8$ | | $V_{dc}$ | 0 | $V_{dc}/2$ | $V_{dc}$ |
| 16 | $S_2, S_3, S_5, S_8$ | $S_2, S_3, S_5, S_8$ | | 0 | $V_{dc}$ | $V_{dc}/2$ | $-V_{dc}$ |

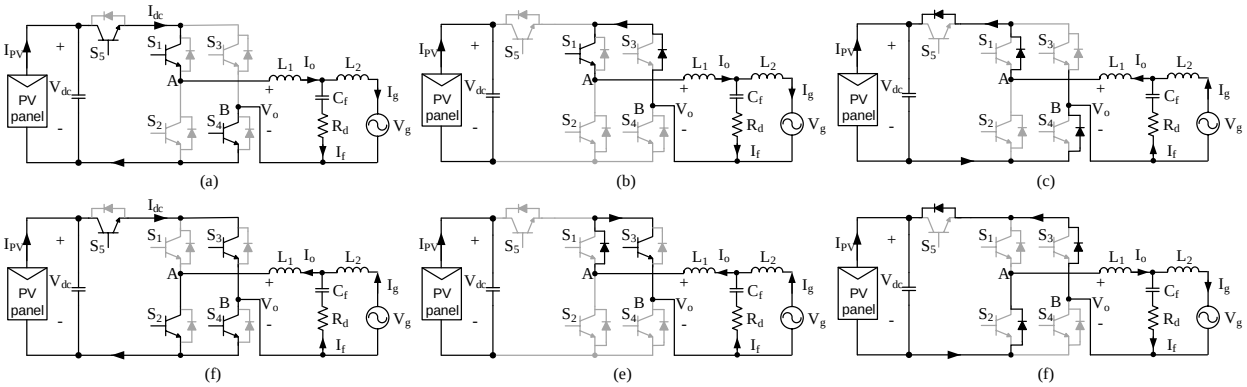


**Fig. 2. Operation modes of H5 inverter with conventional modulation. (a)** $S_5$ , $S_1$ , $S_4$ : $V_o = +V_{dc}$ , **(b)** $S_1$ : $V_o$ **=0 freewheeling mode during positive half cycle in positive power region (** $I_o$ **and** $V_g$ **>0), (c)** $S_1$ : $V_o = +V_{dc}$ **mode in negative power region (** $V_g$ **>0 and** $I_o$ **<0), (d)** $S_5$ , $S_3$ , $S_2$ : $V_o = -V_{dc}$ , **(e)** $S_3$ : $V_o$ **=0 freewheeling mode during negative half cycle in positive power region (** $I_o$ **and** $V_g$ **<0), (f)** $S_3$ : $V_o = -V_{dc}$ **mode in negative power region (** $V_g$ **<0 and** $I_o$ **>0).**

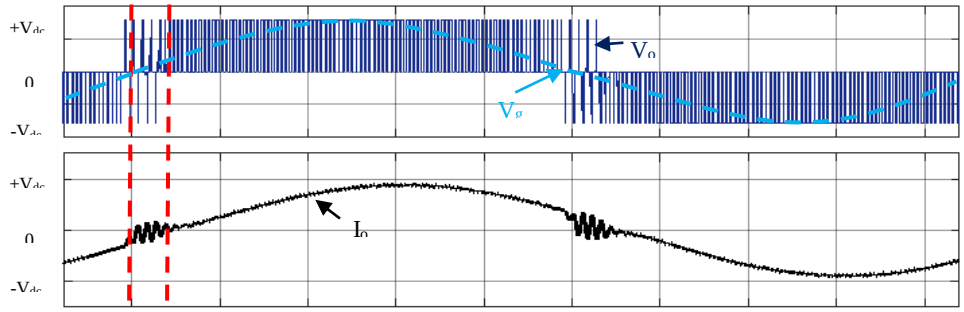


**Fig. 3. Waveforms of the conventional modulation for the H5 inverter under non-unity power factor.**

Table 6 presents the possible switching combinations of the HERIC inverter. In all the possible switching combinations for this inverter, the CMV is constant and equal to $V_{dc}/2$. That means the leakage current is close to zero.

In Fig. 1(f) the H8 inverter is indicated [25]. This topology uses 8 power electronic switches (IGBTs in this study) denoted by $S_1 \sim S_8$. The switches $S_1 \sim S_4$ operate in fundamental frequency (low-frequency switches) while the other switches operate with switching frequency (high-frequency switches). The interesting fact is that the high-frequency switches operate at lower voltage and the low-frequency switches operate at the higher voltage which results in high efficiency. The switching combinations of the multilevel inverter are shown in Table 7. There are 10 different switching combinations that produce the output voltage of zero. For the voltage levels $V_{dc}/2$ and $-V_{dc}/2$ both available combinations should be used in order to balance the voltage of capacitors.

### 2.2. Reactive power injection capability of single-phase transformerless PV inverter

The reactive power capability of single-phase transformerless PV inverters is studied in this part. According to the grid requirements and grid codes [19-23], the design of next-generation transformerless PV systems should consider not only the quality of the grid current but also the reactive power injection capability under grid faults (unity and non-unity power factor operation).

In non-unity power factor operation, during the negative power region, the sign of the grid voltage $V_g$ and the sign of the grid current $I_o$ are opposite. In the case of unipolar modulation, the output voltage of inverters is three-level ( $+V_{dc}$ , $0$ , $-V_{dc}$ ). In the negative power region, generating unipolar PWM is depended on the polarities of both $V_g$ and $I_o$. For example, in the H5 inverter with conventional modulation, as shown in Fig. 2(c), when $V_g$ is positive and $I_o$ is negative, the current passes through anti-parallel diodes of $S_1$ , $S_5$ , and $S_4$. Therefore, in this case, the output voltage is $+V_{dc}$ while the level of the output voltage should be zero. As a result, as indicated in Fig. 3, a distortion occurs in the negative power region. In the modulation of transformerless grid-connected PV inverters, it has been tried to use the switching combinations which have the same value of the

CMV. This means the CMV remain constant; which according to (3), the leakage current will be negligible or almost zero. But as seen in the presented tables for switching combinations of the inverters, some of these switching combinations are dependent on the grid current [26, 27].

For example, in Table 1, which presents the possible switching combinations for the H-Bridge inverter with unipolar modulation, in switching combinations number 5 to 8, if $V_g$ and $I_o$ do not have the same sign, in the zero output voltage states, the real value of the output voltage would not be zero. This means that in the zero output voltage states, the current path would be different. Moreover, the CMV would also vary. This, however, does not happen in the case of bipolar modulation and the CMV would remain constant, thus the leakage current is zero (Table 2). In H5 (Table 3, Fig. 2 and Fig. 3) and HERIC inverters the same condition exists. With the difference that the CMV in HERIC inverter is constant for all of the switching combinations (Table 6). Also, the conventional modulation of mentioned inverters (H5 and HERIC) is depicted in Figs. 2 and 4. Tables 4 and 5 show the switching combinations for two inverters, H6D1 and H6D2. There are much more switching combinations in comparison with the H-Bridge inverter. However, as the tables indicate, the CMV, as well as the output voltage in most of the switching combinations, depends on grid current ( $I_o$ ) direction. Furthermore, Operation modes of the H6D1 inverter with the conventional modulation are illustrated in Fig. 5. The highlighted combinations within the switching combinations that provide the constant CMV provide zero output voltage level. In order to have constant CMV, only the highlighted switching combinations should be used. This means that the output voltage levels of $\pm V_{dc}/2$ in the H6D2 inverter are not available. If in some time interval of the positive half cycle of the output voltage, $I_o < 0$, as indicated in Table 5, while keeping constant CMV (using only the highlighted switching combinations) the zero voltage level cannot be obtained because there is no path for the current to flow. This means that it has no reactive power injection capability. Therefore, taking into consideration the constant CMV, these inverters are also two-level inverters unless the condition $I_o > 0$ could be always guaranteed.

The switching combinations of the inverter shown in Fig. 1(f) are indicated in Table 7. Based on this table, the inverter could be a 5-level inverter. However, considering the constant CMV, the output voltage levels of $\pm V_{dc}/2$ will not be achieved. Therefore, the inverter is a three-level inverter including the positive, zero and negative voltage levels. Considering Table 7, there are six combinations of the zero output voltage which provide constant CMV (No. 1-3 and 6-8). However, in this paper, the aim is that the H-Bridge ( $S_1 \sim S_4$ ) to operate in fundamental frequency and therefore only two of the switching combinations are used for the zero output voltage (No. 1 for the positive half cycle and No. 2 for the negative half cycle).

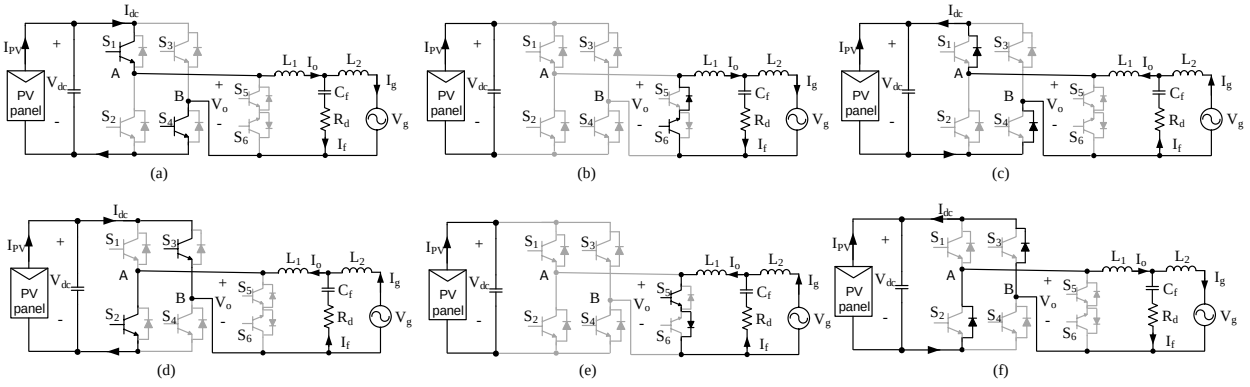


**Fig. 4. Operation modes of HERIC inverter with conventional modulation. (a) $S_1$, $S_4$ : $V_o = +V_{dc}$, (b) $S_6$ : $V_o$ =0 freewheeling mode during positive half cycle in positive power region ( $I_o$ and $V_g$ >0), (c) $S_6$ : $V_o = +V_{dc}$ mode in negative power region ( $V_g$ >0 and $I_o$ <0), (d) $S_3$, $S_2$ : $V_o = -V_{dc}$, (e) $S_5$ : $V_o$ =0 freewheeling mode during negative half cycle in positive power region ( $I_o$ and $V_g$ <0), (f) $S_5$ : $V_o = -V_{dc}$ mode in negative power region ( $V_g$ <0 and $I_o$ >0).**

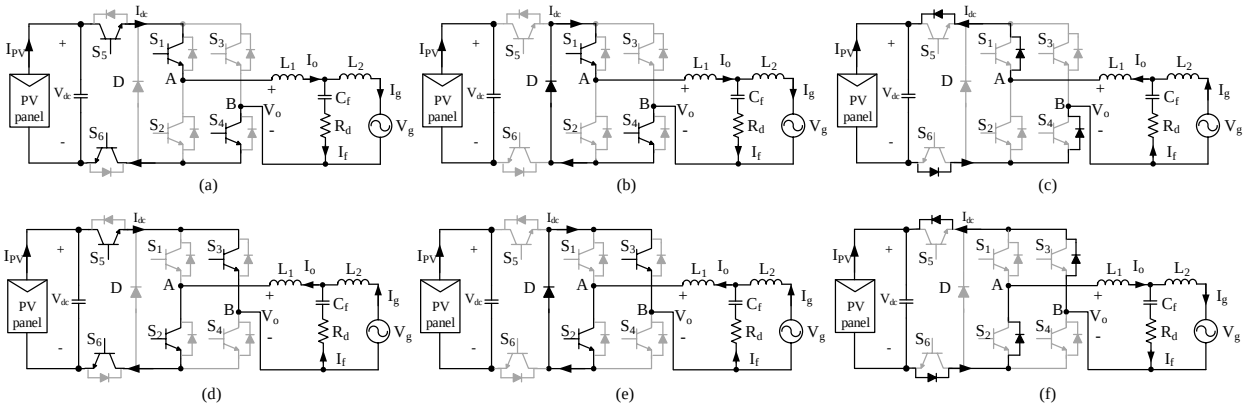


**Fig. 5. Operation modes of H6D1 inverter with conventional modulation. (a)** $S_5$ , $S_6$ , $S_1$ , $S_4$ : $V_o = +V_{dc}$ , **(b)** $S_1$ , $S_4$ : $V_o$ **=0 freewheeling mode during positive half cycle in positive power region (** $I_o$ **and** $V_g$ **>0), (c)** $S_1$ , $S_4$ : $V_o = +V_{dc}$ **mode in negative power region (** $V_g$ **>0 and** $I_o$ **<0), (d)** $S_5$ , $S_6$ , $S_3$ , $S_2$ : $V_o = -V_{dc}$ , **(e)** $S_3$ , $S_2$ : $V_o$ **=0 freewheeling mode during negative half cycle in positive power region (** $I_o$ **and** $V_g$ **<0), (f)** $S_3$ , $S_2$ : $V_o = -V_{dc}$ **mode in negative power region (** $V_g$ **<0 and** $I_o$ **>0).**

As the voltage rating of the switches $S_1 \sim S_4$ is double of that of the switches $S_5 \sim S_8$, the operation of the switches $S_1 \sim S_4$ in fundamental frequency helps to reduce their stresses. As a result, for the switches $S_1 \sim S_4$ low-cost slow switches could be selected lowering the overall cost of the inverter. As a summary, for the inverter shown in Fig. 1(f) only the switching combinations No. 1, 2, 15 and 16 (Table 7) are used in order to have constant CMV and also fundamental frequency operation of the switches $S_1 \sim S_4$. One of the reasons for the development and improvement of the transformerless grid-connected inverters is the CMV and leakage current issue while the new standards emphasize on the LVRT capability and reactive power injection. Based on the switching table shown in the previous section (Tables 1-7) and the analysis above, the discussed inverters have a good performance in unity power factor, but not in a non-unity power factor except the H8 inverter which has better performance in both conditions. In fact, the inverters operate optimally at unity power factor because the sign of $I_o$ and $V_g$ is always the same. But, during negative power region (non-unity power factor), the zero-voltage state could not be realized because there is no current path for the current to flow. Based on the analysis, the generated reactive power in mentioned PV inverters is underlined current path must be provided so that zero-voltage state is attained during negative power region.

## 3. CONTROL SYSTEM

Nowadays ideas should be put forward to improve the new structures according to standards, as having LVRT capability with reactive power injection; or to think of modulations that could make use of these capabilities. In this section, a simple control is being proposed which can provide LVRT capability in the grid voltage drop (the grid voltage sag) and also keep constant CMV into both LVRT and normal operations.

### 3.1. Control Loop

In the grid-connected PV inverters, delivering a specific power to the grid is the main objective. The overall control system is shown in Fig. 6. The Second-Order Generalized Integrator Quadrature Signal Generator (SOGI-QSG) based phase locked loop (PLL) [9], [25], [28], [29] is used in order to synchronize the control system with the grid voltage and generate orthogonal signals, $v_\alpha$ and $v_\beta$ . Further, applying the Park transformation ($\alpha\beta \rightarrow dq$) leads to the $v_q$ signal is given the amplitude of the output voltage and the $v_d$ signal is made equal to zero in the steady state by the action of the phase-locking loop.

In fact, the SOGI is able to generate both in-phase $v_\alpha$ and quadrature $v_\beta$ components that are filtered and contain only the fundamental component. It consists of feedback loops involving two integrators, as indicated in Fig. 7. The transfer function $G_d(s)$ from $V_g$ to $v_\alpha$ can be written as follows:

$$G_d(s) = k\omega s / s^2 + k\omega s + \omega^2 \quad (4)$$

In Eq. (4), $\omega = \theta$ is the resonant frequency of the SOGI-QSG, and the transfer function $G_q(s)$ from $V_g$ to $v_\beta$ can be obtained as follows:

$$G_q(s) = k\omega^2 / s^2 + k\omega s + \omega^2 \quad (5)$$

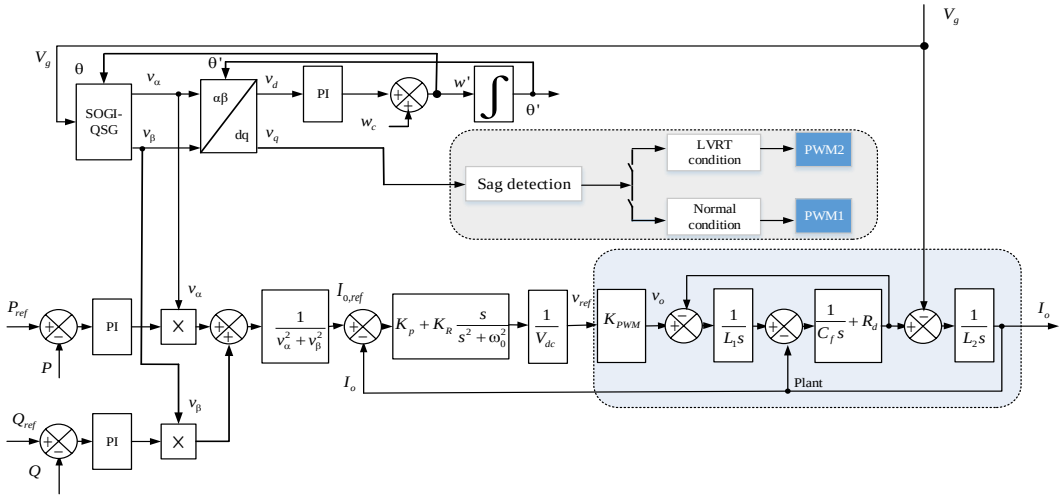


**Fig. 6. System model and control system including the SOGI-QSG, PI power controllers and PR current controller, and sag detection unit.**

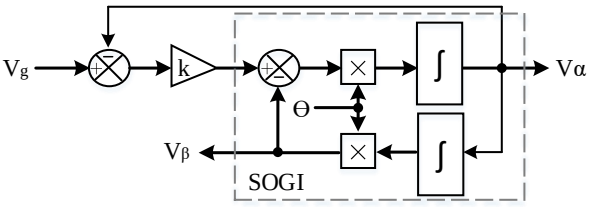


**Fig. 7. SOGI-based quadrature-signal generator (SOGI-QSG).**

Both $G_d(s)$ and $G_q(s)$ are resonant filters for $0 \le k < 2$ and are able to select the component of $V_g$ at the resonant frequency $\omega$. When the frequency moves away from $\omega$, $|G_d|$ and $|G_q|$ decrease, depending on the gain k. as a result, only the fundamental frequency component can pass the SOGI-QSG.

A smaller gain k leads to better selectivity and offers better attenuation to other frequency components but it takes longer to settle down. Another important characteristic of SOGI-QSG is that $v_\beta$ is always 90° delayed, at any frequency, from $v_\alpha$ because:

$$G_d(s) = \frac{s}{\omega} G_q(s) \tag{6}$$

Which means the SOGI-QSG always generates two perpendicular components $v_\alpha$ and $v_\beta$, at the frequency of $\omega$.

The SOGI-QSG can be plugged into the typical single-phase PLL shown in Fig. 6. The components $v_\alpha$ and $v_\beta$ are created, which are further transferred into DC components $v_d$ and $v_q$ using the park transformation. A PI controller is used to drive $v_d$ to zero. The output the PI controller is added with the nominal frequency $\omega_c$ to form the estimated frequency $\theta$, which is then integrated to obtain the estimated phase angle $\theta'$. Note that the estimated frequency $\theta$ is fed back to SOGI-QSG so that it is able to select the component at right frequency. When the phase is locked, $v_d$ =0. As a result, the frequency, the phase and the amplitude of signal $V_g$ are all available.

As shown in Fig. 6, the control objective is to deliver a specified active and reactive power ( $P_{ref}$ , $Q_{ref}$ ) to the grid. $P_{ref}$ is achieved from the MPPT algorithm and $Q_{ref}$ is usually set to zero in normal operating condition. Based on the single-phase PQ theory [22], [25], [30], [31], the injected grid current reference can be produced by regulating the active and reactive power to add inner current control loop to shape the grid current in LVRT operation mode with the purpose of reactive power injection. The active and reactive power controllers are the proportional-integral (PI) type. Obtaining the reference value of the grid current ( $I_{o,ref}$ ) requires mathematical processes for output controllers. Therefore, the grid current reference $I_{o,ref}$ can be achieved as follows:

$$I_{o,ref} = \frac{1}{v_\alpha^{\,2} + v_\beta^{\,2}} \begin{bmatrix} v_\alpha & v_\beta \end{bmatrix} \begin{bmatrix} G_P(s)(P - P_{ref}) \\ G_Q(s)(Q - Q_{ref}) \end{bmatrix} \tag{7}$$

where $v_\alpha$ , $v_\beta$ are the orthogonal components of the grid voltage, respectively, $P$ , $Q$ are the active power and reactive power, $P_{ref}$ and $Q_{ref}$ are the power references

and $G_P(s)$, $G_Q(s)$ are PI-based controllers for the active power and reactive power, respectively.

For the current control loop, the Proportional-Resonant (PR) current controller is used. The PR controller with harmonic compensators presents an acceptable performance in terms of accurate tracking and fast dynamic response. The transfer function of this current controller can be obtained as follows:

$$G_I(s) = k_p + k_R \frac{s}{s^2 + \omega_o^2} + \sum_{h=3,5,7} \frac{k_{Rh} s}{s^2 + (h\omega_o)^2} \quad (8)$$

where $k_p$ is the proportional gain, $k_R$ is the fundamental resonant control gain, $k_{Rh}$ is the control gain for h-order resonant controller and $\omega_o$ is the grid fundamental frequency.

The output of the current controller divided by the DC-link voltage is the reference voltage ( $v_{ref}$ ) for inverter modulation. Then the reference voltage ( $v_{ref}$ ) is compared with triangular carrier waves to generate the gate signals of the inverter.

The control system described above is a conventional control system for single-phase grid-connected PV inverters. The point is that when using the same PWM method for both normal and LVRT conditions, in most of the inverters, the output voltage and current quality deteriorate in around the zero-cross point of the voltage. Considering the switching tables of the inverter structures given in the previous section and bringing into mind that the CMV should be constant (only highlighted switching combinations should be used), the reason behind this phenomenon is that in some of the switching combinations, the value of the output voltage depends on the output current direction and its correspondence with the output voltage polarity. If such a switching combination is used in the modulation method of the normal operating condition (where output power factor is unity) there will not be a deficiency. However, if the same PWM method is used in the LVRT condition (where the output power factor is non-unity), the output voltage will have non-intended value around the zero-cross point. Therefore, this will clearly deteriorate the quality of the output voltage and current. In order to solve this problem, the reconfigurable PWM method is proposed in this paper. This method is based on switching between two PWM methods (denoted by PWM1 and PWM2 in Fig. 6) for the two normal and LVRT conditions.

Using conventional PWM (PWM1) and keeping constant CMV, as examples, the operation modes of the inverters H5, HERIC, and H6D1 are indicated in Figs. 2, 4, and 5. Considering Fig. 2(b) and 2(c), in both of the modes the switch $S_1$ is turned ON, however, in the mode Fig. 2(b) in which $I_o$ >0, the output voltage is zero while in mode Fig. 2(c) in which $I_o$ <0, the output voltage is equal to $+V_{dc}$ . The same discussion could be presented for the other inverters as shown in Figs. 4(b), 4(c) and Figs. 5(b), 5(c).

In order to improve the operation of the inverters in the LVRT condition and adding the capability of reactive power injection without distorting the output current waveform, the PWM2 is used as indicated in Figs. 8, 9, and 10 for the inverters H5, HERIC, and H6D1, respectively.

For example, as shown in Fig. 9 for the HERIC inverter, the switches $S_5$ and $S_6$ are turned ON simultaneously to provide zero output voltage level.

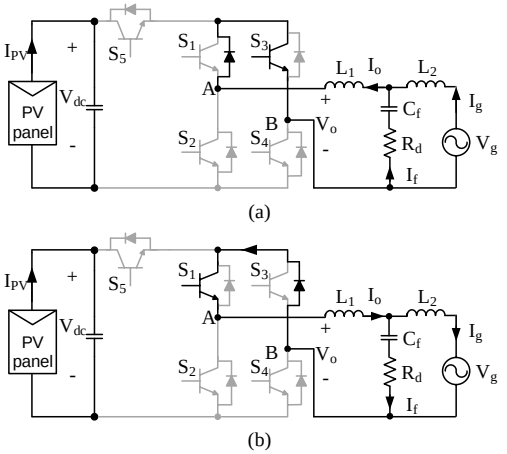


**Fig. 8. Zero voltage level of H5 inverter with proposed PWM in negative power reign: $S_1$ , $S_3$ =ON, (a) $V_g > 0$ , $I_o < 0$ , (b) $V_g < 0$ , $I_o > 0$ .**

In this case, the output voltage value does not depend on the current direction and therefore, it will not take non-intended values improving the output waveforms quality while keeping constant CMV. Also, according to Tables 1 to 7, for other inverters can select appropriate switching combination such that it does not depend on the direction of the output current to provide the zero voltage state.

### 3.2. Reactive Power Injection Strategy

When the grid faults are detected by the sag detection unit, the PV system enters the LVRT operation from the normal operation. According to the requirements in the grid codes, the system should be connected to the grid for a specified period of time to support the grid and help to compensate for the voltage drop.

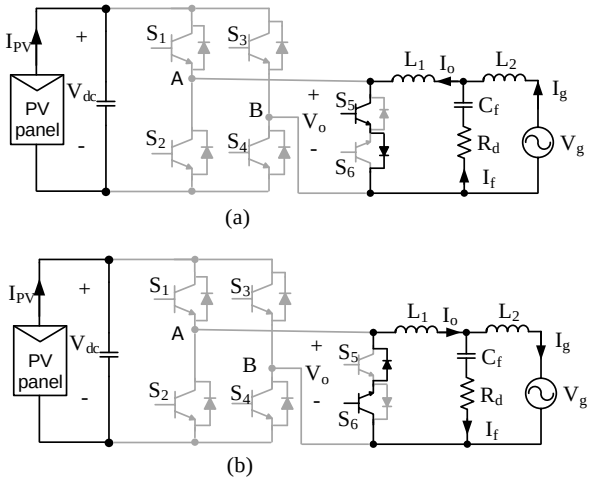


**Fig. 9. Zero voltage level of HERIC inverter with proposed PWM in negative power reign: $S_5$ , $S_6$ =ON, (a) $V_g > 0$ , $I_o < 0$ , (b) $V_g < 0$ , $I_o > 0$ .**

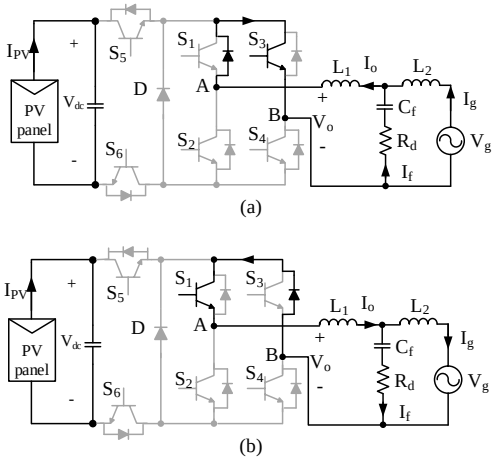


**Fig. 10. Zero voltage level of H6D1 inverter with proposed PWM in negative power reign: $S_1$ , $S_3$ , $S_6$ =ON, (a) $V_g > 0$ , $I_o < 0$ , (b) $V_g < 0$ , $I_o > 0$ .**

For single-phase PV systems, considering the protection of PV inverters against overcurrent, some strategies are proposed in [22, 28]. In this paper, the constant average active power strategy has been used for injection of reactive power at the time of the occurrence of a fault. This Control strategy is to remain the active power constant and to take the maximum available energy of PV panel. The following equations describe the injected reactive power proportional to the voltage sag depth.

$$\begin{cases} I_d = \dfrac{1}{V_g} I_N \\ I_q = k(1 - V_g) I_N \end{cases} \tag{9}$$

where $I_d$ , $I_N$ , and $I_q$ are the active current, the nominal current, and the reactive current, respectively. In this reactive power injection strategy, due to over-current may be the inverter shutdown. The following limitation should be considered to prevent inverter shutdown in the design of the inverter.

## 4. SIMULATION AND ANALYSIS OF PERFORMANCE TRANSFORMERLESS PV INVERTERS

As mentioned earlier, all inverters have a good performance in unity power factor, but not in a non-unity power factor except the H8 inverter. This means that they do not have the capability to inject reactive power. Taking into account the tables presented, by selecting appropriate switching combinations, it is possible to create new current paths for the zero level, so that reactive power injection is realized while keeping constant CMV. In order to analyze the theoretical concepts, simulation results are obtained by MATLAB/Simulink. The inverter specifications for a 1kW, 220V, 50Hz system are presented in Table 8.

**Table 8. Parameters of Inverters.**

| Simulation parameters | Value |
|---|---|
| Input Voltage | 320 V |
| Grid Voltage/Frequency | 220 V/50 Hz |
| Rated Power | 1 kW |
| DC-Link Capacitor | 1200 µF |
| LCL-Filter | L1 =3.6 mH, L2 =0.7 mH, Cf =2.3 µF, Rd =5 Ω |
| Switching Frequency | 10 kHz |
| Stray Capacitor | 150 nF |

The proposed control method of Fig. 6 is implemented on three widely adopted PV inverters, i.e., H5, H6D1, and HERIC. The PI controllers are set at $K_{pp} = 1$ , $K_{pq} = 10$ , $K_{ip} = 50$ and $K_{iq} = 10$ , the parameters of the PR current controller $K_p = 20$ , $K_R = 2000$ and $K_{R3,5,7} = 3000$ are considered. During normal operation, the system operates in unity power factor ( $Q^* = 0$ ) and the reference of active power is set at $P^* = 1kW$ .

As shown in Fig. 11 to Fig. 13, in time interval 1.2s<t<1.4s a voltage sag happens. In this interval, the LVRT operation is started. The value of the voltage sag is 0.25 p.u., and thus according to the constant average active power strategy [22, 28], the average active power remains constant at $P^* = 1kW$ , and the required injection of reactive power $Q^*$ should be 375 Var with regard to over-current protection in this control strategy.

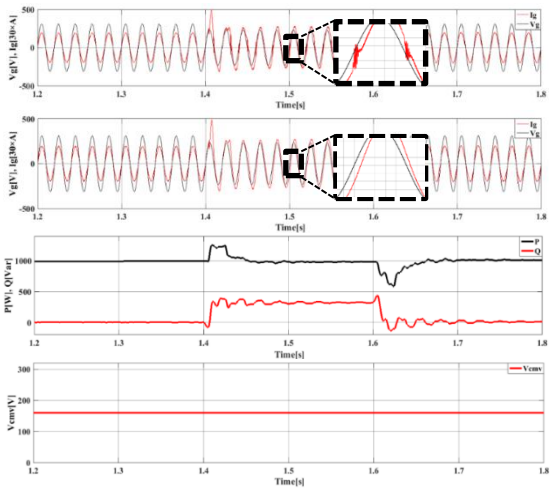

**Fig. 11. Performance of the H5 inverter with conventional modulation and proposed method in normal and LVRT operation (voltage sag 0.25pu): grid voltage Vg [V], grid current Ig [30×A], active power P [W], reactive power Q [Var], and CMV Vcmv [V].**

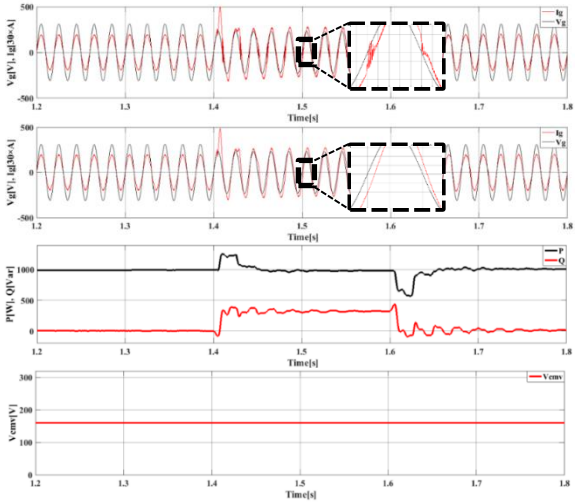

**Fig. 12. Performance of the H6D1 inverter with conventional modulation and proposed method in normal and LVRT operation (voltage sag 0.25pu): grid voltage Vg [V], grid current Ig [30×A], active power P [W], reactive power Q [Var], and CMV Vcmv [V].**

This would result in a decay in the quality of the output current waveform. In addition, due to current flow in another path, this would cause variable CMV in that time period. This is a cause for the leakage current occurrence. But using the proposed reconfigurable PWM method, the quality of the output current waveform around the zero voltage state is improved as illustrated in Figs. 11 to 13. It is worth noting that this improvement is achieved by simply switching between two PWM methods in a same structure of the inverter. In the LVRT condition, as described in the previous section, those switching combinations which are independent of the output current direction are used to produce zero output voltage. The CMV is also kept constant, resulting in a limitation in the leakage current. Therefore, the LVRT capability with the reactive power injection is obtained by this proposed control system. Furthermore, the proposed method can be used for not only these inverters but also all the single-phase grid-connected transformerless PV inverters.

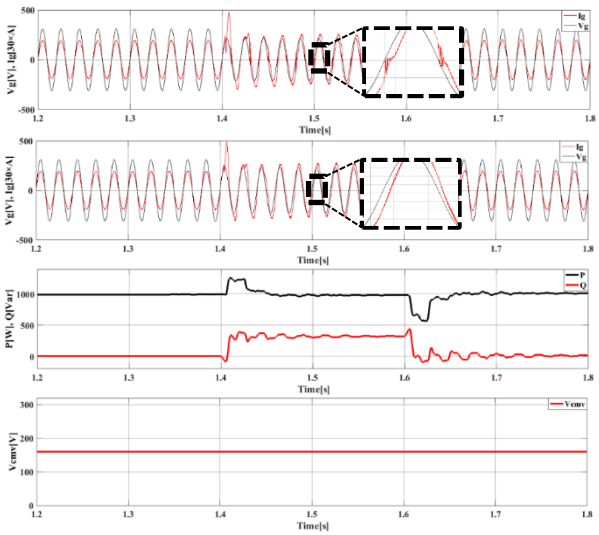


**Fig. 13. Performance of the HERIC inverter with conventional modulation and proposed method in normal and LVRT operation (voltage sag 0.25pu): grid voltage Vg [V], grid current Ig [30×A], active power P [W], reactive power Q [Var], and CMV Vcmv [V].**

**Table 9. Overall comparison of the mentioned PV inverters.**

| **Inverters** | | **H-Bridge (bipolar)** | **H-Bridge (unipolar)** | **H5** | **H6D1** | **H6D2** | **HERIC** | **H8** |
|---|---|---|---|---|---|---|---|---|
| **Number of power switches** | | 4 | 4 | 5 | 6 | 6 | 6 | 8 |
| **LVRT operation in conventional modulation** | **CMV** | Constant | Variable | Constant except at ZVL | Constant except at ZVL | Constant except at ZVL | Constant except at ZVL | Constant |
| | **Device of switching frequency/ grid frequency** | 4/0 | 2/2 | 3/2 | 2/4 | 2/4 | 4/2 | 4/4 |
| | **Efficiency** | 96.5% | 97.5% | 96.1% | 96.2% | 96% | 96.3% | 96.74% |
| | **THD** | 1.45% | 8.69% | 10.54% | 9.92% | 9.98% | 11.34% | 1.54% |
| **LVRT operation in proposed method** | **CMV** | Constant | Variable | Constant | Constant | Constant except at ZVL | Constant | Constant |
| | **Device of switching frequency/ grid frequency** | 4/0 | 4/0 | 5/0 | 6/ 0 | 6/ 0 | 6/ 0 | 4/ 4 |
| | **Efficiency** | 96.5% | 96.9% | 95.7% | 95.9% | 95.5% | 95.9% | 96.74% |
| | **THD** | 2.45% | 1.81% | 5.89% | 5.95% | 5.9% | 6.12% | 1.54% |
| **Normal operation** | **CMV** | Constant | Variable | Constant | Constant | Constant | Constant | Constant |
| | **Device of switching frequency/ grid frequency** | 4/0 | 2/2 | 3/2 | 2/ 4 | 2/ 4 | 4/ 2 | 4/ 4 |
| | **Efficiency** | 97.1% | 97.9% | 96.8% | 97.1% | 96.5% | 96.61% | 96.9% |

* ZVL: Zero Voltage Level

Overall comparison of the mentioned PV inverters in normal and LVRT operations is presented in Table 9.

## 5. CONCLUSIONS

Transformerless inverters offer the better efficiency, compared to those inverters that have the galvanic isolation. On the other hand, in case the transformer is eliminated, the generated common-mode behavior of the inverter topology mainly influences the leakage current through the parasitic capacitance of the PV systems. Moreover, recently an important part of requirements for PV systems is the so-called LVRT capability. Considering the structure of commercially available inverters such as H-Bridge, H5, H6D1, H6D2, HERIC, and H8, offering a solution that can provide the aforementioned requirements is an economical, cost-effective, and high-efficiency solution. This paper has introduced a control system and given a flexible solution for the PV inverters, used to generate the suitable zero-voltage state for providing LVRT capability with reactive power injection. The proposed method is based on a reconfigurable PWM method, in which, it is switched

between two PWM methods in the two operation conditions (normal and LVRT). As can be seen in the simulation results of the previous section, by using the possible and appropriate switching combinations, the constant CMV and high efficiency can be achieved. This point makes it an attractive solution for transformerless PV applications.

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