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A DC-DC Converter with High Voltage Conversion Ratio Recommended for Renewable Energy Application

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Abstract— *In this article, a novel topology of DC-DC converter based on voltage multiplier cell and coupled inductor with higher efficiency and low blocking voltage across semiconductor is proposed for renewable energy application. The recommended topology obtains a high voltage gain using voltage multiplier cell and one coupled inductor. Only one power switch is utilized in this structure, which reduces the converter's cost. The other benefits of this converter are low number of components, high efficiency due to the zero-voltage switching and the zero-current switching of diodes, and low blocking voltage of the power switch and diodes. Besides, the voltage multiplier cell acts as a passive clamp circuit and reduces the voltage stress across the power switch. Thus, a low rated power switch can be used in the presented topology. Due to the zero-current switching in Off-state, the reverse recovery problem of diodes is reduced. To illustrate the performance and superiority of the presented topology, operation modes, steady-state and efficiency analysis, and the comparison study with other similar converters are presented. Finally, a 160 W experimental prototype with 50 kHz switching frequency and 17 V input voltage are built to confirm the theoretical investigation and effectiveness of the proposed converter.*

Keywords— Voltage multiplier cell, Coupled inductor, Zero-voltage switching, Zero-current switching, High voltage gain

1. INTRODUCTION

Today, due to the quick increase in energy dissipation, renewable energy systems like photovoltaic, fuel cells, and wind energy are remarked [1, 2]. This matter has encouraged power engineering researchers, organizations, and governments to expand renewable energy studies [3, 4]. Generated voltage by the fuel cell and PV is DC and has a low level. A high gain DC-DC converter is utilized as an interface tool between the renewable resource and the load to convert voltage from a low level to a high level. This type of DC-DC converter must have a high voltage conversion ratio, small volume, and high efficiency. DC-DC power converters could enhance the voltage level to provide the load or transmission line requirements' needs [5, 6]. Due to these matters, the expansion of high voltage gain converters has emerged as one of the most influential and notable clarifications for utilizing renewable energy [7]. Various kinds of DC-DC converters are presented that can obtain high voltage conversion ratios. Usually, the high step-up DC-DC structures can be categorized in two groups: isolated or non-isolated classes used in renewable energy applications [8, 9]. The traditional high step-up DC-Dc converters generate a high voltage conversion ratio with an extensive duty cycle. Working with a high duty cycle causes conduction losses and electromagnetic interface (EMI) problems. Furthermore, the voltage gain is limited in application due to the power losses of semiconductors, and equivalent series resistance of the capacitors and magnetic devices. The voltage conversion ratio could be enhanced using switched capacitors and or switched inductor units [10, 11]. Furthermore, electromagnetic interface (EMI) concerns limit voltage boosting because of the high duty cycle levels. On the other hand, at high step-up voltage ratios, the associated current stress may produce a failure and deteriorate element lifetime [12, 13]. We can overcome these problems using other types of traditional DC-DC converters such as forward, push-pull, and fly-back converters by adjusting the transformer's turn's ratio. Nonetheless, high voltage stress is produced across the power switches by the transformer leakage inductance's energy [14, 15]. Different high gain converters based on the coupled inductors with low core loss can be utilized. In these topologies, the switches may operate in hard switching conditions with high switching losses. In these topologies, the high voltage gain is generated through regulating the power switch's duty cycle and the coupled inductor's turns ratio. The power switch may face short-term transient voltage, and the coupled inductor's leakage inductance reduces the voltage gain and produces high power losses [16, 17]. Isolated converters are proposed with a high voltage conversion ratio. However, because of isolated configuration, the cost and volume of these converters are high. The above-mentioned obstacles can be reduced by using non-isolated DC-DC converters. These structures present numerous benefits, like low cost and volume. The proposed non-isolated topology in [18], is proper for microgrid inverters. Nevertheless, the high input current ripple of this structure reduces the input PV panel lifetime. In [19], a high step-up structure is suggested based on voltage multiplier cell (VMC) and coupled inductor. This converter also has high input current ripple. On the other hand, the number of used components is high, which leads to achieve low efficiency. In [20–25], DC-DC converters with high voltage gain advantage are proposed. However, significant problems such as high input current ripple, high voltage stress throughout the semiconductor components, diodes reverse recovery problem, high components count, and low efficiency still exist in the high step-up DC-DC structures. In [26] a high gain transformer less converter based on the switched inductor and capacitor and active network is recommended. This structure has two switches, which cause high conduction losses.

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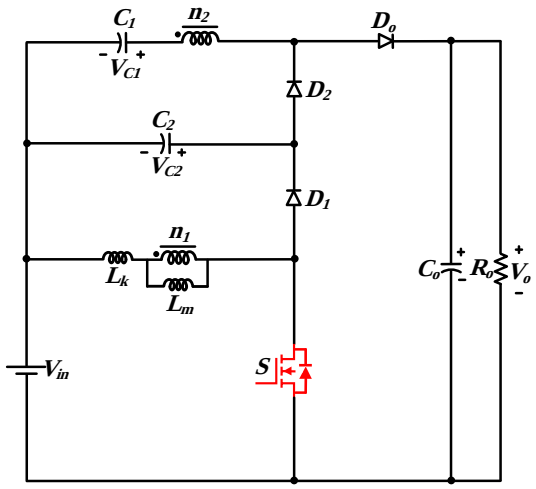


Fig. 1. Configuration of the suggested coupled inductor-based topology.

This paper proposes a new VMC and coupled inductor-based topology of high step-up DC-DC converter suggested for renewable energy usages such as fuel cell and PV power systems. The benefits of this converter are: 1) Only one power switch is used in this structure, which reduces the converter's cost, 2) low number of components, 3) high efficiency due to the ZCS and ZVS of diodes, and 4) low voltage stress across the power switch and diodes. Besides, due to the operation of the VMC as a clamp circuit, the blocking voltage of the power switch is decreased and a low rated power switch can be used in the presented topology. On the other hand, ZCS of diodes reduces the reverse recovery problem. The superiority of the suggested topology is confirmed by operation modes, steady-state and efficiency analysis, and comparison study with other similar converters. Finally, a 200 W experimental prototype with 50 kHz switching frequency is implemented to confirm the effectiveness of the presented topology.

2. Configuration of the Suggested DC-DC Converter and Operation Modes

The structure of the suggested high step-up DC-DC topology is shown in Fig. 1. As can be seen, this converter includes input DC source (V_{in}), one power switch (S), three diodes (D_1, D_2, and output diode (D_o)), one coupled inductor with n_1 (primary winding) and n_2 (secondary winding), and three capacitors (C_1, C_2, and C_o). The VMC consists of the diodes D_1 and D_2 and the capacitor C_2. Diode D_2 and the capacitor C_2 operates as passive clamp and reduces the blocking voltage of the power switch. Also, the coupled inductor is modeled as an ideal transformer, with turn ratio equal to $N=(n_2/n_1)$, magnetizing (L_m) and leakage (L_k) inductances. The stored energy in L_k is recycled and given to the output load.

The following presumptions are considered for modes analysis and steady-state investigations:

- All diodes and power switch are ideal
- The voltage ripple of the capacitors is neglected
- The leakage inductor (L_k) of the used coupled inductor is ignored.

There are three intervals in each switching period (T_s). One interval occurs in on-state and two intervals occurs in off-state of the power switch S. The time waveforms of the suggested topology during one switching period T_s are depicted in Fig. 2.

First time interval [$t_0 < t < t_1$]: This time interval is beginning when the power switch S is turned on. Diode D_2 is also turned on at ZVS condition. Diodes D_1 and D_o are reverse biased and the output voltage is divided between these two diodes. The magnetizing inductances L_m is charged by input voltage V_{in} and

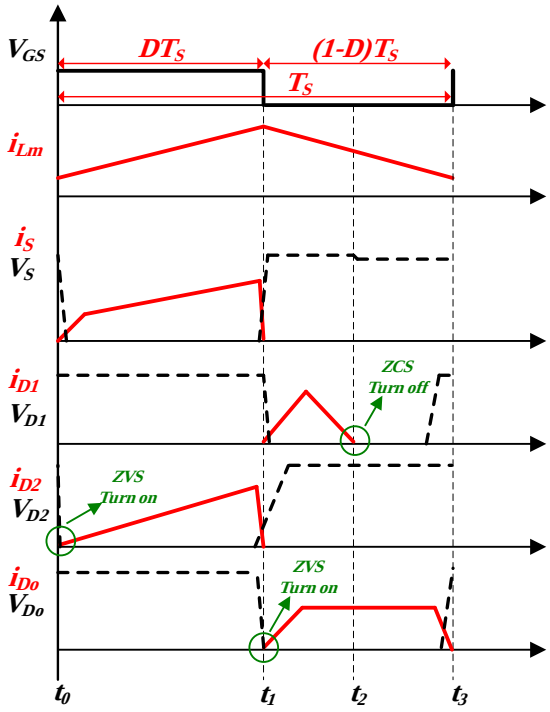


Fig. 2. Time waveform of the suggested converter.

its current is linearly raised. The capacitor C_1 and C_2 is charged and discharged, respectively. Also, R_o is supplied by output capacitor C_o. The equivalent configuration of the first-time interval is shown in Fig. 3(a). The following equations are obtained for this interval:

$$-V_{in}+V_{L_m}+V_{L_k}=0 \tag{1}$$

$$-V_{C_2}-NV_{L_m}+V_{C_1}=0 \tag{2}$$

$$i_S=i_{L_k}=i_{in} \tag{3}$$

Second time interval [$t_1 < t < t_2$]: the second time interval is beginning at $t=t_1$ when the power switch S is turned off and its current reached to zero. Because the voltage across the magnetizing inductances L_m is negative, its current is decreased. Diodes D_1 and D_o are turned on and diode D_2 is turned off. It should be noticed that, the diode D_o is turned on with zero voltage. Thus, the output voltage is divided between the switch S and D_2. In other words, the capacitor C_2 and the diode D_2 acts as a clamp circuit and reduces the voltage stress across the power switch. The stored energy of the secondary side of the coupled inductor and capacitor C_1 is transferred to the load through diode D_o. This interval ends when diode D_1 is turned off at ZCS condition. Due to the ZCS turn off, the reverse recovery problem of diode D_1 is eliminated. The equivalent configuration of the second-time interval is shown in Fig. 3(b) and its equations are calculated as follows:

$$V_{L_m}=-V_{C_2}-V_{L_k} \tag{4}$$

$$V_o=V_{in}+V_{C_1}+NV_{L_m} \tag{5}$$

$$i_{in}+i_{C_2}=i_{L_k}+i_{C_1} \tag{6}$$

$$i_{C_2}=i_{D_1} \tag{7}$$

$$i_{C_1}=-i_{D_o} \tag{8}$$

Third time interval [$t_2 < t < t_3$]: During third time-interval, the power switch S and the diode D_2 are still turned off. Diode D_o is the only semiconductor component that is tuned on. The input voltage energy is transferred to the load. Because the power switch

S and the diodes D_1 and D_2 are turned off, the output voltage is divided between these three elements. Thus, in this operation time, the voltage stress across the power switch S is lower than the second time interval. The equivalent configuration of the third mode is illustrated in Fig. 3(c). Equation (9) is achieved in third interval:

$$i_{in} = i_{C_1} = -i_{D_o} = -\left(i_{C_o} + i_o\right) \tag{9}$$

In Fig. 3, P_{si}, P_{sj}, Q_{si} and Q_{sj} are defined between bus i-th and bus j-th as below:

The suggested structure voltage gain (M=V_o/V_{in}) and the voltage stress across the used semiconductors are calculated by neglecting the power losses and the coupled inductor's leakage inductance L_k. In other words, for steady-State analysis, the ideal value of the used components is considered.

By using the volt-second low on the L_m, the following equation can be reached:

$$\langle V_{Lm} \rangle_{T_s} = 0 \quad \Rightarrow \quad DV_{in} - (1-D)\, V_{C_2} = 0 \tag{10}$$

Therefore, the voltage of C_2 is founded as (11):

$$V_{C_2} = \frac{D}{1-D} V_{in} \tag{11}$$

Using equations (1), (2), and (11), the voltage of the capacitor C_1 is calculated as (13):

$$NV_{in} = V_{C_1} - V_{C_2} \Rightarrow V_{C_1} = NV_{in} + V_{C_2} = NV_{in} + \frac{D}{1-D} V_{in} \tag{12}$$

$$V_{C_1} = \frac{N(1-D)+D}{(1-D)} V_{in} \tag{13}$$

Also, by using equations (5), the output voltage V_o can be written versus input voltage as (14):

$$V_o = V_{in} \frac{N(1-D)+D}{(1-D)} V_{in} + \frac{D}{1-D} V_{in} \tag{14}$$

Finally, the voltage gain of the suggested high step-up DC-DC topology is obtained versus duty cycle (D) and coupled inductor turns ratio (N):

$$M = \frac{V_o}{V_{in}} = \frac{1+N}{(1-D)} \tag{15}$$

The maximum voltage stress across the power switch S can be calculated in the second time interval:

$$V_S = V_{in} + V_{C_2} = V_{in} + \frac{D}{1-D} V_{in} = \frac{1}{1-D} V_{in} \Rightarrow V_S = \frac{1}{1+N} V_o \tag{16}$$

After calculating of V_S, the maximum blocking voltage the diode D_2 is also obtained:

$$-V_S - V_{D_2} + V_o = 0 \Rightarrow V_{D_2} = \left(1 - \frac{1}{1+N}\right) V_o \tag{17}$$

$$V_{D_2} = \frac{N}{1+N} V_o \tag{18}$$

The voltage stress across the diode D_1 can be obtained in the third operation time, when this diode is turned off. Additionally, Diode D_1 voltage stress is equal to V_S:

$$V_{D_1} = V_S = \frac{1}{1+N} V_o \tag{19}$$

Besides, the voltage stress across the diode D_1 can be calculated in the first-time interval:

$$-V_{D_1} - V_{D_o} + V_o = 0 \quad \Rightarrow \quad V_{D_o} = \left(1 - \frac{1}{1+N}\right) V_o \tag{20}$$

$$V_{D_o} = \frac{N}{1+N} V_o \tag{21}$$

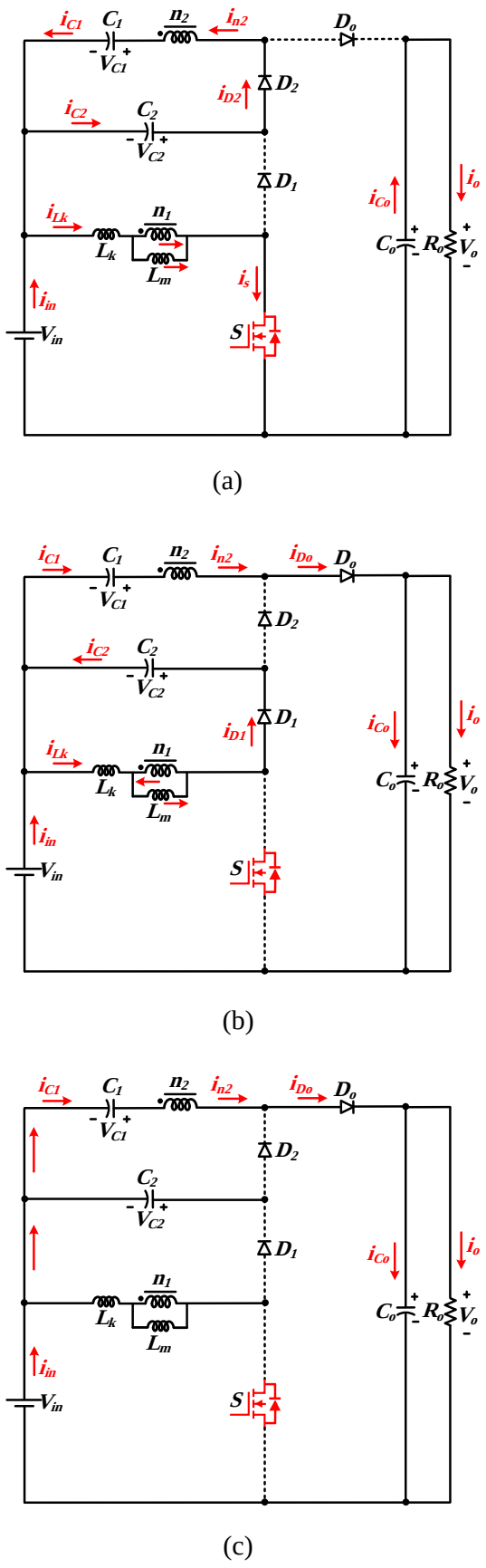
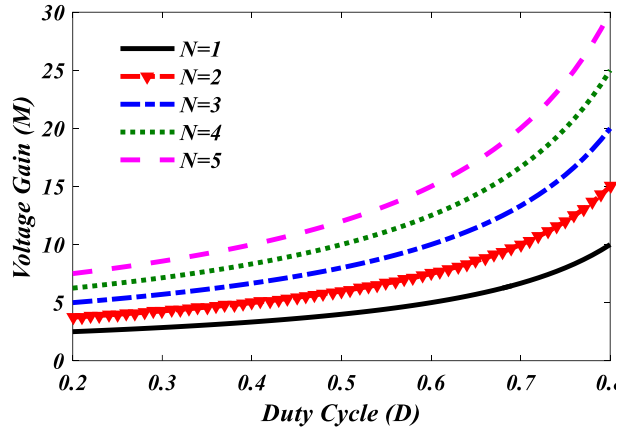
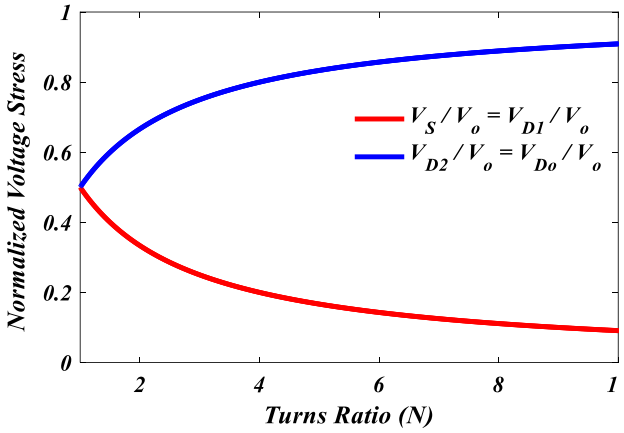


Fig. 3. The operation modes equivalent circuit of the proposed structure, (a) mode 1, (b) mode 2, (c) mode 3.



(a)



(b)

Fig. 4. The voltage conversion ratio (M) and voltage stress of the suggested topology (a) voltage gain, (b) semiconductors blocking voltage.

The voltage conversion ratio (M) and blocking voltage of the semiconductors versus D and N are depicted in Figures 4 (a) and (b), respectively.

According to the configuration of the suggested topology, the diodes average currents are equal to the output current:

$$I_{D_1}^{avg} = I_{D_2}^{avg} = I_{D_o}^{avg} = I_o \tag{22}$$

Average current of L_m is equal to the input average current. By using the voltage gain relation, the input average current can be expressed versus output current as (23):

$$I_{L_m}^{avg} = I_{in}^{avg} = \frac{1+N}{1-D} I_o \tag{23}$$

The power switch's average current is calculated as (24):

$$I_S^{avg} = I_{L_m}^{avg} - I_{D_1}^{avg} = \left(\frac{1+N}{1-D} - 1\right) I_o = \frac{N+D}{1-D} I_o \tag{24}$$

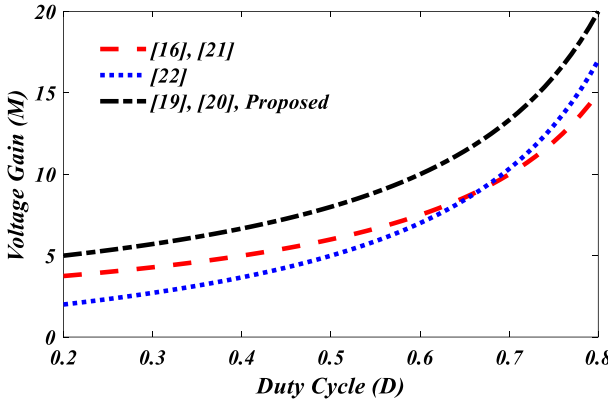
The current stress of the switch S and diodes are obtained as (25)–(28):

$$i_S = \frac{N+D}{D\,(1-D)} I_o \tag{25}$$

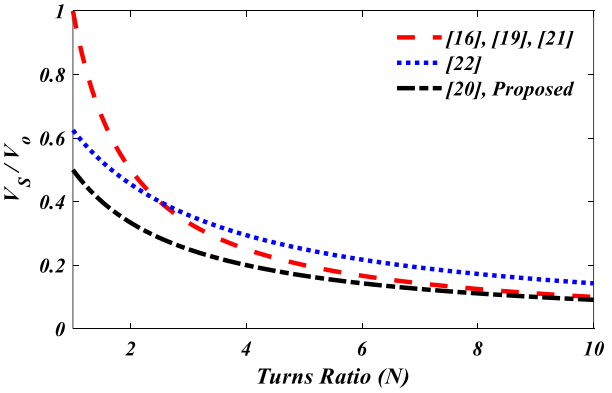
$$i_{D_1} = \frac{N}{1-D} I_o \tag{26}$$

$$i_{D_2} = \frac{1}{D} I_o \tag{27}$$

$$i_{D_o} = \frac{1}{1-D} I_o \tag{28}$$



(a)



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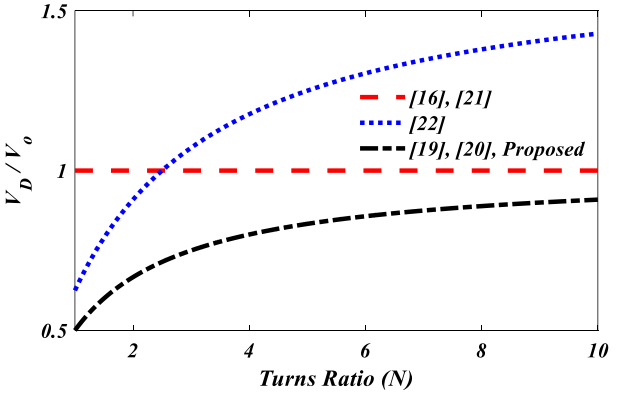


(c)

Fig. 5. Comparison of the recommended topology and introduced converters in Table 2, (a) M, (b) V_S / V_o, and (c) V_D / V_o.

The suggested DC-DC converter's efficiency is analyzed based on the following considerations:

1) R_{DS-ON}: Turn-on resistance of switch S
2) $R_{(n1,\ n2)}$: Equivalent series resistance (ESR) of the coupled inductor primary and secondary windings
3) $R_{(D1,\ D2,\ Do)}$: Diodes ESR
4) $V_{F\ (D1,\ D2,\ Do)}$: Forward voltage of diodes.
5) $R_{(C1,\ C2,\ Co)}$: ESR of capacitors

Using equation (29) the suggested converter's efficiency can be obtained:

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% = \frac{P_{in} - P_{Loss}}{P_{in}} \times 100\% \tag{29}$$

Table 1. The calculated RMS currents of the proposed converter's elements

RMS currents of the used components	
$I_{C_1}^{rms}=\sqrt{\frac{1}{D(1-D)}}\,I_o$	$I_{C_2}^{rms}=\sqrt{\frac{1}{D(1-D)}}\,NI_o$
$I_{C_o}^{rms}=\sqrt{\frac{D}{(1-D)}}\,I_o$	$I_S^{rms}=\frac{N+D}{\sqrt{D}(1-D)}\,I_o$
$I_{D_1}^{rms}=\frac{N}{\sqrt{1-D}}\,I_o$	$I_{D_2}^{rms}=\frac{1}{\sqrt{D}}\,I_o$
$I_{D_o}^{rms}=\frac{1}{\sqrt{1-D}}\,I_o$	$I_{n_1}^{rms}=\frac{N+D}{\sqrt{D}(1-D)}\,I_o$
$I_{n_2}^{rms}=\sqrt{\frac{1}{D(1-D)}}\,I_o$	

$$P_{Loss}=P_{S\_conduction}+P_{S\_switching}+P_{D\_conduction}+P_{D\_forward}+P_{capacitors}+P_{CL} \quad (30)$$

In (30), $P_{S\_conduction}$ is the switch S conduction power loss:

$$P_{S\_conduction}=R_{DS,on}\left(I_{S\_rms}\right)^2 \quad (31)$$

$P_{S\_switching}$ is the switching loss of the power switch S and is defined as follows:

$$P_{S\_switching}=\frac{1}{2}(t_r+t_f)f_sV_SI_{S\_avg} \quad (32)$$

$P_{D\_conduction}$ is the sum of diodes conduction losses and is expressed as (33):

$$P_{D\_conduction}=R_{D_1}\left(I_{D_1\_rms}\right)^2+R_{D_2}\left(I_{D_2\_rms}\right)^2+R_{D_o}\left(I_{D_o\_rms}\right)^2 \quad (33)$$

$P_{D\_forward}$ is the sum of diodes forwarded voltage losses and is equal to (34):

$$P_{D\_forward}=V_{F_{D1}}I_{D_1\_avg}+V_{F_{D2}}I_{D_2\_avg}+V_{F_{Do}}I_{D_o\_avg} \quad (34)$$

$P_{capacitors}$ is the sum of power capacitors losses and can be expressed as follows:

$$P_{capacitors}=r_{C_1}\left(I_{C_1-rms}\right)^2+r_{C_2}\left(I_{C_2-rms}\right)^2+r_{C_o}\left(I_{C_o-rms}\right)^2 \quad (35)$$

P_{CL} is the sum of coupled inductor's primary and secondary side conduction losses, which is calculated as (36):

$$P_{CL}=r_{n_1}\left(I_{n_1-rms}\right)^2+r_{n_2}\left(I_{n_2-rms}\right)^2 \quad (36)$$

It should be noticed that, for efficiency analysis, calculation of Root Mean Square (RMS) currents is necessary. These currents are calculated and summarized in Table 1.

3. Design Considerations

3.1. Magnetizing Inductance and the Coupled Inductor Turns Ratio (*N*)

The input magnetizing inductances L_m can be calculated by (37):

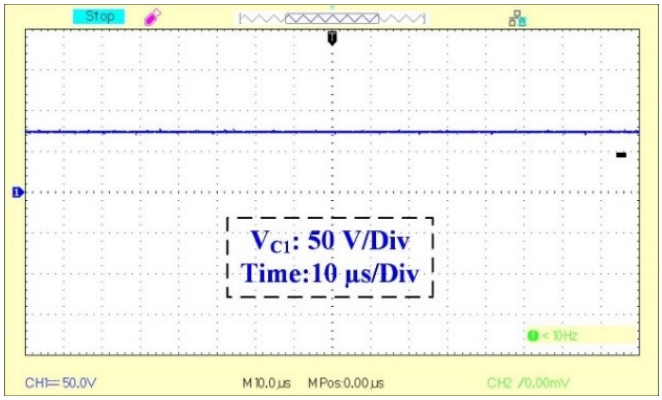
$$V_{L_m}=L_m\frac{di_{L_m}}{dt} \quad \Rightarrow \quad L_m=\frac{V_{L_m}D}{\Delta i_{L_m}f_s} \quad (37)$$

In (36), Δi_{L_m} defines the current ripple of the L_m. For CCM operation of the recommended topology, the value of $\Delta i_{L_{in}}$ is assumed as (37):

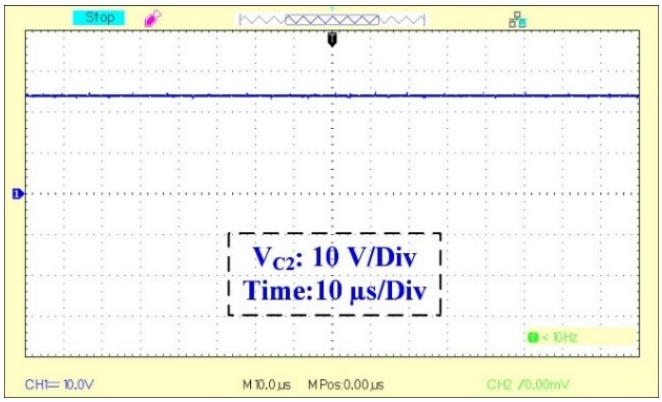
$$\Delta i_{L_{in}}\geq 20\%I_{L_{in}} \quad (38)$$

Finally, the value of L_m can be expressed versus duty cycle, switching frequency, coupled inductor turns ratio and the output resistor as follows:

$$L_m\geq\frac{V_{L_m}D}{20\%I_{L_m}f_s}=\frac{V_{in}D}{20\%\left(\frac{1+N}{1-D}\right)I_of_s}=\frac{V_{in}D\left(1-D\right)}{20\%\left(1+N\right)I_of_s}=\frac{D\left(1-D\right)^2V_o}{20\%\left(1+N\right)^2I_of_s}=\frac{D\left(1-D\right)^2R_o}{20\%\left(1+N\right)^2f_s} \quad (39)$$



(a)



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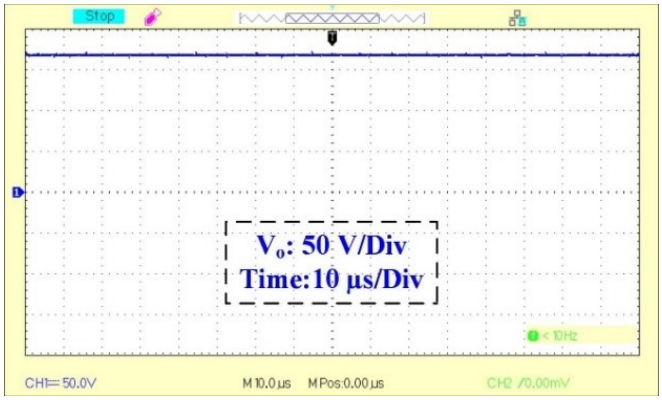


(c)

Fig. 6. Experimental measurement of the proposed converter, (a) V_{C1}, (b) V_{C2}, and (c) V_o

Besides, using (15), N can be achieved versus V_o, V_{in}, and D:

$$N = M\left(1-D\right) - 1 = \frac{V_o}{V_{in}}\left(1-D\right) - 1 \tag{40}$$

3.2. Capacitors

The current and the voltage relation of a capacitor is expressed as (40):

$$i_C = C\frac{dV_C}{dt} \quad \Rightarrow \quad C = \frac{i_C D}{\Delta V_C f_s} \tag{41}$$

In order to obtain low voltage ripple on the capacitors, the following assumption is considered:

$$\Delta V_C \geq 2\%\ V_C \tag{42}$$

The values of the C_1, C_2, and C_o are calculated versus N, D, f_s, and R_o as (42) - (44), respectively:

$$\begin{aligned} C_1 \geq \frac{i_{C_1} D}{2\% V_{C_1} f_s} &= \frac{\left(1-D\right) I_o}{2\%\left(N\left(1-D\right)+D\right) V_{in} f_s} \\ &= \frac{\left(1+N\right) I_o}{2\%\left(N\left(1-D\right)+D\right) V_o f_s} \\ &= \frac{\left(1+N\right)}{2\%\left(N\left(1-D\right)+D\right) R_o f_s} \end{aligned} \tag{43}$$

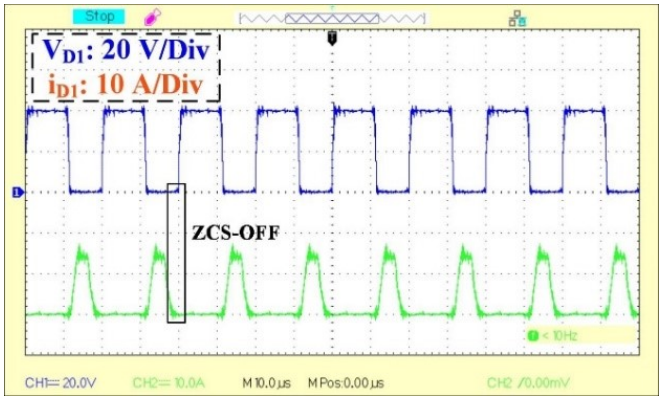
$$\begin{aligned} C_2 \geq \frac{i_{C_2} D}{2\% V_{C_2} f_s} &= \frac{N I_o}{2\% V_{in} f_s} \\ &= \frac{N\left(1+N\right) I_o}{2\%\left(1-D\right) V_o f_s} \\ &= \frac{N\left(1+N\right)}{2\%\left(1-D\right) R_o f_s} \end{aligned} \tag{44}$$

$$C_o \geq \frac{i_{C_o} D}{2\% V_{C_o} f_s} = \frac{D^2 I_o}{2\%\left(1-D\right) V_o f_s} = \frac{D^2}{2\%\left(1-D\right) R_o f_s} \tag{45}$$

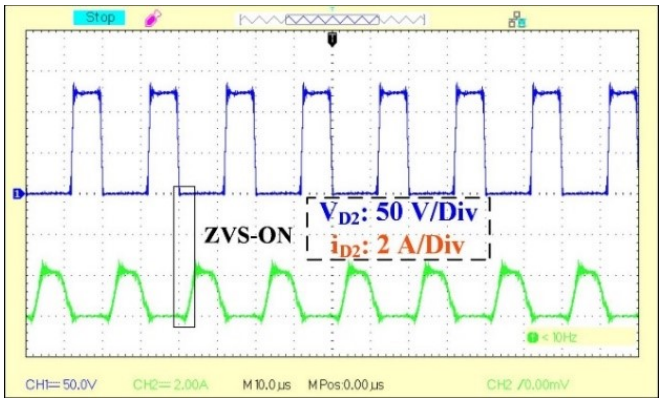
4. Comparison Study

A comprehensive comparison between the recommended DC-Dc structure and other similar coupled inductor-based topologies is presented to confirm the performance of the recommended topology in terms of voltage conversion ratio (M), normalized maximum blocking voltage of switches (V_S / V_o) and diodes (V_D / V_o), components count, efficiency, and soft-switching. This comparison is summarized in Table 2. The values of this table are calculated for *N=3* and *D=0.6*.

Figure 5(a) shows the voltage gain comparison between the introduced converters. According to this figure and Table 2, the proposed converter and converters in [19] and [20] have equal voltage gain. Besides, the voltage gains of the converters in [16], [21], and [22] are lower than the proposed converter. However, the presented converter in [19] has higher voltage stress across the power switch, and it needs a high rated switch. The converter in [20] has two magnetic core. Therefore, the volume and the cost of this converter are higher than the suggested topology. On the other hand, the used semiconductors in [20] suffer from hard switching problem. Figure 5(b) illustrates the normalized maximum voltage stress across the power switches. As shown in this figure, the proposed converter and [20] have lower voltage stress on switches than the other introduced converters. Therefore, a low rated power switch can be used in the suggested structure, which reduces the cost and increases the efficiency of the proposed topology. The comparison of the voltage stress across the didoes is depicted in figure 5(c). Converters in [16] and [21] have constant voltage stress versus coupled inductor turns ratio. The proposed converter in [22] has a high value of voltage stress throughout diodes for turns ratio number higher than two (*N>2*). The proposed converter and [19] and [20] have lower V_D / V_o



(a)



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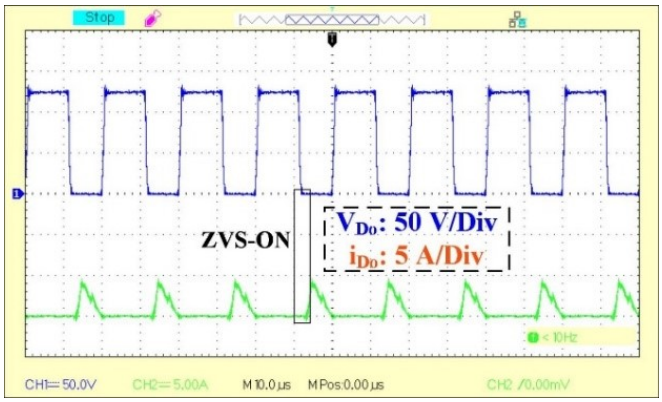
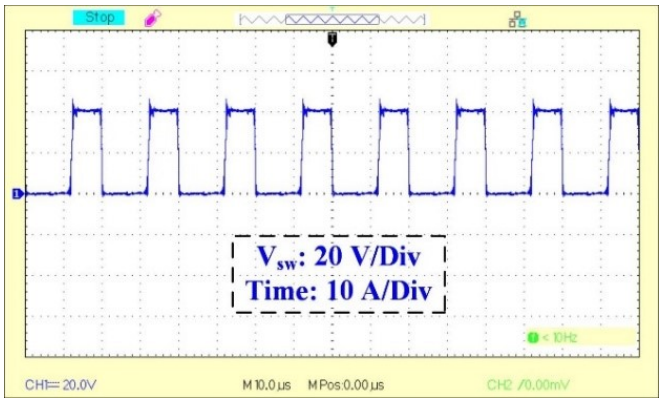


(c)



(d)

Fig. 7. Experimental measurement of the proposed topology, (a) V_{D1}-I_{D1}, (b) V_{D2}-I_{D2}, (c) V_{Do}-I_{Do}, and (d) V_{sw}

Table 2. Comparison between the suggested DC-DC topology and other similar converters

Converter	Number of components					M	V_S / V_o	V_D / V_o	Eff [%] at 200 W	Soft Switching
	CI*	I*	S*	D*	C*					
[16]	1	1	1	2	2	$\frac{N}{1-D}=7.5$	$\frac{1}{N}=0.33$	1	95.9	Yes
[19]	1	0	1	3	3	$\frac{1+N}{1-D}=10$	$\frac{1}{N}=0.33$	$\frac{N}{1+N}=0.75$	94	Yes
[20]	1	1	1	3	3	$\frac{1+N}{1-D}=10$	$\frac{1}{1+N}=0.25$	$\frac{N}{1+N}=0.75$	-	No
[21]	1	1	2	2	3	$\frac{N}{1-D}=7.5$	$\frac{1}{N}=0.33$	1	95.4	Yes
[22]	1	1	1	4	3	$\frac{1+ND}{1-D}=7$	$\frac{1}{1+ND}=0.35$	$\frac{N}{1+ND}=1.07$	93.8	No
[27]	1	0	1	3	3	$\frac{2+N}{1-D}=8.33$	$\frac{1}{2+N}=0.2$	$\frac{N+1}{N+2}=0.8$	96.3	No
[28]	1	0	1	3	2	$\frac{2+N}{1-D}=8.33$	$\frac{1}{2+N}=0.2$	$\frac{N+1}{N+2}=0.8$	96	No
[29]	1	0	2	1	2	$\frac{1+N}{1-D}=10$	$\frac{1}{1+N}=0.25$	1	92.8	Yes
[30]	1	0	2	1	2	$\frac{1+N}{1-D}=10$	$\frac{1}{1+N}=0.25$	1	-	Yes
[31]	1	0	1	3	3	$\frac{1+N}{1-D}=10$	$\frac{1}{1+N}=0.25$	$\frac{1}{N}=0.33$	-	No
[32]	1	1	1	5	4	$\frac{N+2}{(1-D)^2}=13.89$	$\frac{N+1}{N+2}=0.8$	1	93.8	No
[33]	1	0	1	3	3	$\frac{2+N}{1-D}=8.33$	$\frac{1}{2+N}=0.2$	$\frac{N+1}{N+2}=0.8$	96	No
Proposed	1	0	1	3	3	$\frac{1+N}{(1-D)}=10$	$\frac{1}{1+N}=0.25$	$\frac{N}{1+N}=0.75$	95.6	Yes

* CL=coupled inductor, *I=inductor, *S=switch, *D=diodes, *C=capacitors, $D=0.6$, and $N=3$.

between the introduced converters. Due to the low components count and didoes soft turn on and off, the suggested converter has higher efficiency, which its value is equal to 95.6 % at 160 W output power. In Table 2, the proposed converter and the converter in [16] and [21] have the highest efficiency. Also, the efficiency of [16] is higher than the proposed converter. These converters have high efficiency because of low number of components and existing of soft switching. However, the proposed converter has a higher voltage gain than the converters in [16] and [21]. Where, the voltage gain of [16] and [21] for N=3 and D=0.6 is obtained 7.5 and the voltage gain of the suggested converter is obtained equal to 10. Also, the proposed converter has lower voltage stress across power switch and diodes than [16] and [21]. This leads to use low rated semiconductor and as a result, the cost of the proposed converter is lower than the other converters of Table 2. {R1-3} As seen in this table, the proposed converters in [27] and [28] has high voltage gain with high efficiency. But there is not soft switching condition throughout this topology and the peak voltage across the diode od this converter is high compared to proposed converter. Although the presented converters in [29], [30] and [31] have similar voltage gain and voltage stress through the switch, but the overall efficiency of this structure is low and cannot be used in renewable energy applications. Besides, the mentioned converter in [31] has not soft-switching conditions such as ZVS and ZCS throughout the semiconductor elements. The recommended converter in [33] has higher voltage gain in compared to the proposed converter, however, this converter has a lot of elements, which leads to decrease the efficiency of the proposed converter and also it has not soft-switching condition.
The experimental prototype of the recommended converter has been indicated in Fig. 9.

5. Experimental Results

The experimental results of the suggested high step-up converter are provided in this section of the paper. The obtained experimental measurements indicate the correctness of the theoretical investigations, mathematical calculation and also the performance of the recommended structure. The specification of the used components has been shown in Table 3. The recommended DC-DC topology is built with N=3, V_{in}=17, f_s=50 kHz, and D=0.6 in 160 W output power level.

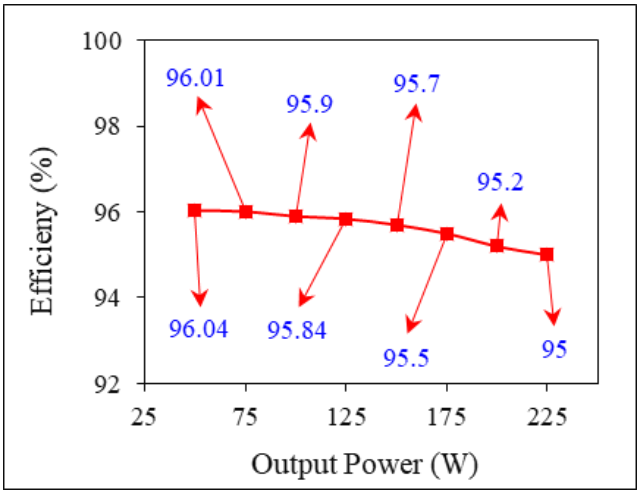


Fig. 8. The measured efficiency curve versus output power

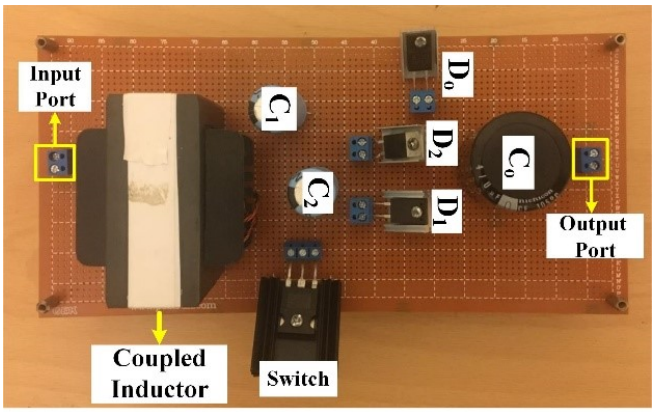


Fig. 9. Experimental prototype of the suggested converter

Table 3. List of the circuit components of the prototype

Element	Specification
Switch	IRFP260N (R_{DS-ON}=0.04)
Diodes	MUR2060 (RDiodes=0.01, V_F=0.9)
L_m	Ferrite core EE50, 200 H, N2/N1=3/1, R_{n1}=0.001, R_{n2}=0.002
C_1,C_2 and C_3	200 V/220 F (R_C=0.01)
C_o	400 V/470 F (R_C=0.02)
L_{k1} and L_{k2}	2 H

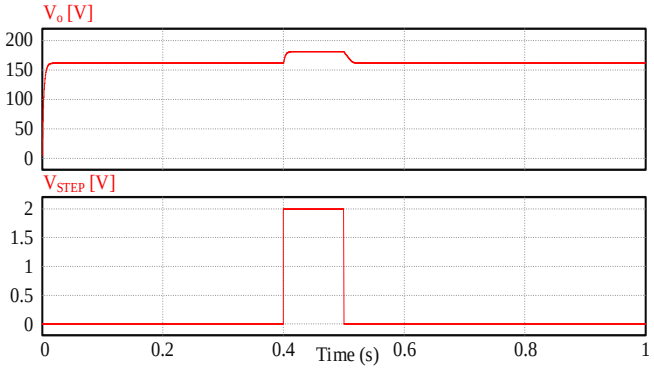


Fig. 10. Dynamics response of the proposed converter

The specific experimental waveforms of the recommended structure have been illustrated in Figures 6 – 7. The capacitor C_1 voltage waveform is depicted in Fig. 6(a). From this figure, the voltage across the capacitor C_1 is equal to 74. The voltage measurement of the capacitor C_2 has been demonstrated in Fig. 6(b), which equal to 24 V. The measurement voltage of the capacitors in experimental result confirm the obtained equations in (11) and (13). The output voltage waveform has been indicated in Fig. 6(c). Regarding this figure, the output voltage V_o is increased to 168 V with poor voltage ripple. The voltage and the current waveform of the diode D_1 have been depicted in Fig. 7(a). From this figure, the V_{D1} and i_{D1} are 40 V and 15 A, respectively. Also, ZCS of D_1 can be seen from this figure. Figure 7(b) indicates the voltage and current waveform of the diode D_2, which are 125 V and 2.6 A, respectively. The voltage and current waveform of the diode D_o have been illustrated in Fig. 7(c). The measured V_{Do} and i_{Do} are 125 V and 4 A, respectively. Related to Figures 7 (b) and 7 (c), these diodes are turned on with zero voltage (ZVS). These conditions enhance in the overall efficiency of the suggested topology. Figure 7(c), demonstrates the voltage measurement of the switch. It can be found that the maximum voltage across the switch is 41 V. This value is very smaller than the V_o. Therefore, the recommended high step-up topology can be achieved high output voltage with low blocking voltage of the switch and diodes. The suggested converter's measured efficiency is illustrated in Fig. 8 versus output power P_o. This curve is obtained for N=3, f_s=50 kHz and D=0.6. The maximum value of the efficiency is obtained 96.04 % at P_o= 50 W. At nominal P_o= 225 W, efficiency is about 95%. Also. the overall efficiency for P_o=25 W $\sim$ 225 W is more than 95%.

The transient response of the proposed converter for step-change about 2V in input voltage is illustrated in Fig. 10. Based on this figure, it is clear that the proposed converter has a good dynamic response for the step-change in the input voltage. Nowadays, the renewable energies such as PV systems, uninterruptible power supplies, wind turbines and fuel cells one of the matter purposes of all governments. However, renewable sources have a low output voltage level. Hence, DC-DC converters with high voltage gain and high efficiency should be used for increasing the voltage level. Related to the theoretical analysis, comparison survey and the laboratory result, it is clear that the semiconductor elements that used in the proposed topology have presented at a low peak voltage, which results in lower cost and increased efficiency of the converter. Considering the presented analysis, the benefits of this converter can be categorized as: 1) only one power switch is used in its structure, which reduces the converter's cost, 2) low number of components, 3) high efficiency due to the ZCS and ZVS of diodes, 4) low blocking voltage of power switch and diodes, 5) using a low rated power switch; because the VMC acts as a passive clamp circuit and reduces the voltage stress across the power switch, 6) negligible reverse recovery problem of diodes due to the ZCS. Besides, it has been shown that the recommended structure efficiency is flexible and higher than 95% that show the suggested converter has ability to operate in high power rating for industry application. Therefore, the proposed converter can be an appropriate candidate in low power and high-power applications such as PV systems, fuel cells.

6. Conclusion

This paper suggested a non-isolated coupled inductor and VMC based topology. The performance and superiority of the proposed topology is verified by operation modes survey, steady-state analysis, efficiency measurement, and comparison study with other similar converters. Considering the presented analysis, the benefits of this converter can be categorized as: A) only one power switch is used in its structure, which reduces the converter's cost, B) low number of components, B) high efficiency due to the ZCS and ZVS of diodes, 4) low blocking voltage of power switch and diodes, 5) using a low rated power switch; because the VMC acts as a passive clamp circuit and reduces the voltage stress across the power switch, 6) negligible reverse recovery problem of diodes due to the ZCS. The main contribution of the proposed converter and the critical factors of the proposed converters and other converters were discussed in detail in the literature. In order to verify the mathematical analysis, a 160 W experimental prototype with 50 kHz switching frequency and 17 V input voltage are built. It was shown that the suggested structure's efficiency is higher than 95 %. Therefore, related to technical survey, steady-state calculation and the experimental result, the recommended high step-up converter could be a proper topology for renewable energy systems

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