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A Modified Switched Capacitor Multilevel Inverter with Symmetric and Asymmetric Extendable Configurations

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Abstract— *Switched capacitor multilevel inverters with low input DC voltage sources and voltage boost capability are very attractive to producing a high voltage levels in the output. The paper introduces a modified switched capacitor multilevel inverter with voltage boost capability. The suggested topology can be extended into symmetric and asymmetric configurations. Nearest-level modulation method is employed to generate high-quality output waveforms. The presented multilevel inverter is compared with the similar configurations by considering various criteria. Finally, to confirm the operation of the suggested topology, a laboratory scale of the suggested inverter is implemented and the results are given.*

Keywords— Multilevel inverter, Switched-capacitor, Symmetric and asymmetric configurations, The nearest level modulation.

1. INTRODUCTION

Multilevel inverters, firstly introduced about four decades ago [1], have become highly reliable power electronic converters for a variety of power systems applications [2–4]. Inverters Multilevel topologies are employed in many applications for power electronics and power systems owing to their remarkable features such as harmonic reduction, voltage stress reduction on switches, *dv/dt* reduction, improved quality and high-efficiency [5]. Their applications include renewable energy resources, FACTs devices, traction drives, electric vehicles, etc. [6–9].

Many advances have been made in the last two decades regarding multilevel inverters. These advances have further emphasized reducing the count of switching elements and, more importantly, the count of DC sources [10, 11]. Conventional multilevel inverters are categorized in to three class: cascaded H-Bridge inverter or CHB [12], flying capacitor inverter or FC and neutral point clamp inverter or NPC. Each of these inverters has drawbacks that limit their applications. FC inverter needs an intricate control method to keep the capacitor voltage at the required level. This topology also has problems with balance and stability with changing types of load. NPC inverter has limited applications due to switch requirements at high voltage generation levels. In addition, FCs and NPCs only can generate three to five-level because of intricate techniques in balancing the capacitor voltage. CHB inverter is superior to FC and NPC due to features such as modularity, high reliability and better error management however, it needs a many isolated DC voltage sources to produce staircase output voltage [13–15].

Recently, many topologies have been introduced for decrease the number of devices in various authorities. As the number of semiconductor devices decreases, the gate driver circuits, size, volume and overall price of the system decrease. DC sources have more weight, volume and price than the other components used in the multilevel inverters [16, 17]. Therefore, research on developing multilevel inverters to reduce isolated DC sources has attracted the attention of researchers. Capacitors are a suitable candidate to replace with DC sources, which introduced switched-capacitor (SC) multilevel inverters [18, 19]. SC inverters are applied in renewable energy resources because their generated voltage is low, so in high-voltage applications, it is required to increase the voltage level. Unlike traditional topologies lacking voltage boost capability, many of the recently suggested SC multilevel inverter topologies have voltage boost capability. Multilevel inverters with voltage boost capability are introduced in [20–22]. In [23], a seven-level topology of inverter with voltage boost capability in grid-connected mode is presented, which uses a single DC input source, two capacitors, and ten switches are employed to step up the input voltage. In [24], a five-level switched capacitor inverter topology with the ability to step up the voltage up to 2 times the input voltage is proposed. The suggested topology uses 8 switches, and one capacitor with a single DC voltage source to produce five-level output voltage. The disadvantage of this inverter is its high number of switching devices to generate five levels in the output. A seven-level switched capacitor multilevel inverter with a boost factor of 1.5, and capacitor voltage balancing ability is presented in [25], which uses a single DC source. The drawback of this topology is its low boost factor, similar to the structure presented in [26]. The proposed topology in [26] has merits such as maximum voltage stress of the switches is less than the input voltage, and it has a voltage boosting capability, which makes it suitable for high voltage applications. Another switched capacitor configuration has been presented in [27], which produces nine levels at the output while using 12 power switches with boost factor of 2.

In this paper, a modified topology of multilevel inverter based on switched-capacitor is proposed. The suggested topology with using the boost ability produce seven-level output voltage waveform with only one input DC source. In the introduced inverter, the number of levels in the output voltage can be increased with

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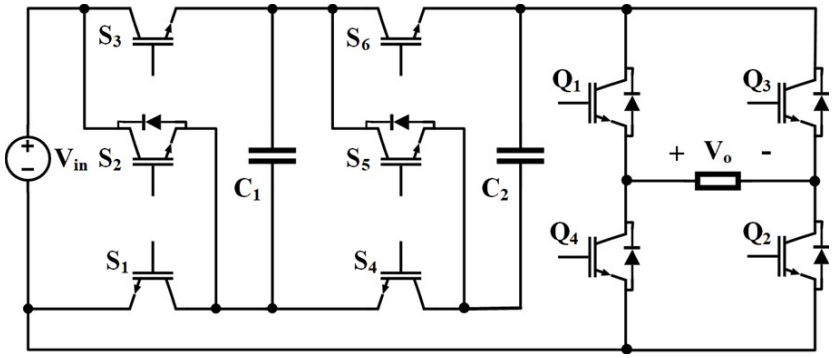


Fig. 1. Configuration of proposed 7-level switched-capacitor inverter

expanding SC units with symmetric and asymmetric input sources. The nearest level modulation method is applied to generate pulses for the switches. The rest of the paper is organized as follows: the proposed 7-level SC inverter topology and its operation modes are described in section 2. In section 3, the extension of the proposed configuration is discussed. In section 4, calculations of capacitors size and power loss are analyzed. To confirm the operation of the introduced topology, experimental test results are presented in section 5. Finally, the paper concluded in section 6.

2. Proposed 7-Level Switched-Capacitor Multilevel Inverter

2.1. Configuration

Configuration of proposed seven-level switched capacitor inverter is given in Fig. 1. It includes ten switches named S_1 to S_6 and Q_1 to Q_4, and two capacitors C_1 and C_2. Capacitors are charged and discharged to generate required voltage levels. A single voltage source, V_{in}, is used as input DC source.

2.2. Operation Principle

To generate 3 positive voltage levels in the inverter output, three operation modes are recognized using the operation of switches S_1 to S_6. The operation of H-bridge converter with switches Q_1 to Q_4 provides negative voltage levels beside the positive levels. In the following, proposed inverter operation modes are described.

Mode 1: When switches S_1, S_3, S_4 and S_6 are turned on while switches S_2 and S_5 are off, both capacitors C_1 and C_2 are charged to V_{in} utilizing the voltage source. As illustrated in Fig. 2(a), the output voltage equals the input voltage, i.e., V_O=V_{in}.

Mode 2: When switches S_1, S_3 and S_5 are turned on while switches S_2, S_4 and S_6 are off, the capacitor C_2 is still charging by the input voltage source. As shown in Fig. 2(b), the series connection of capacitor C_1 and the input voltage source through the switch S_5 doubles the output voltage more than the input voltage, i.e., V_O=$2V_{in}$.

Mode 3: When switches S_2 and S_5 are turned on while the other switches are off, both capacitors C_1 and C_2 are connected in series with the input voltage source to step up the output voltage three times the input voltage, i.e., V_O=$3V_{in}$.

As illustrated in Table. 1, the inverter circuit operates in seven modes related to seven voltage levels, i.e., *0*, $\pm V_{in}$, $\pm 2V_{in}$, and $\pm 3V_{in}$.

2.3. Modulation Algorithm

Various modulation techniques for multilevel inverters are presented in [28, 29]. To produce the required voltage levels, a suitable algorithm for switching of inverter should be used. The inverter output voltage must have all voltage levels with at least total harmonic distortion (THD). To achieve identical voltage steps,

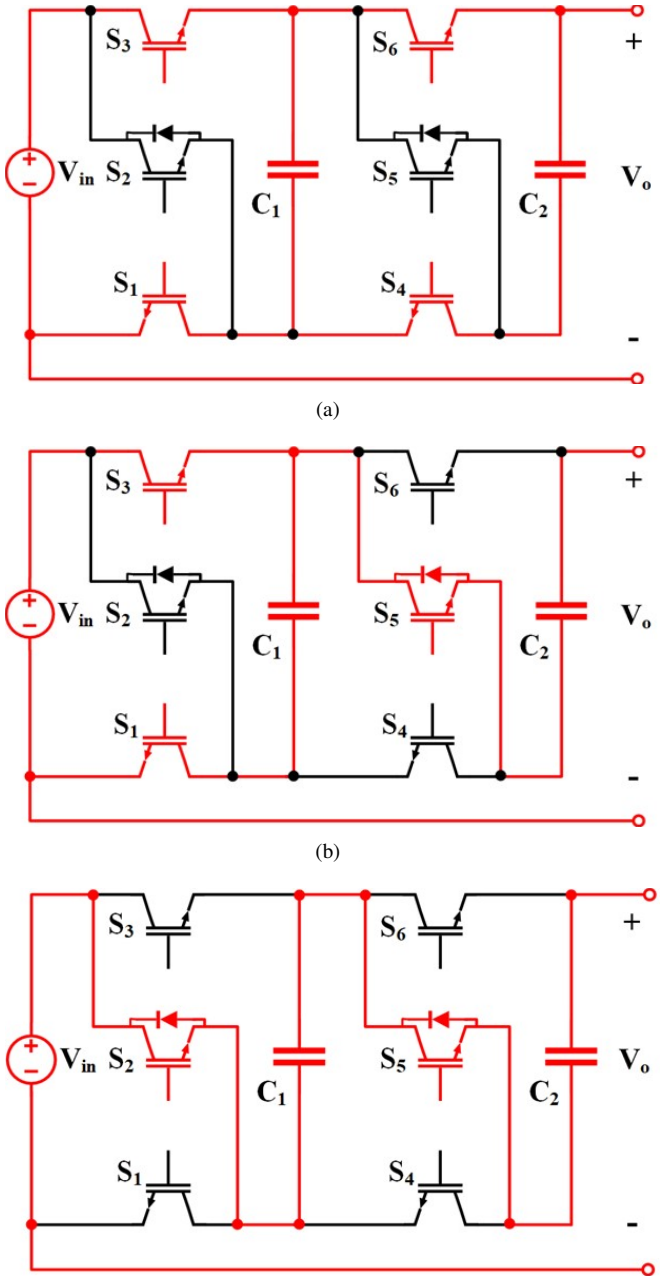


Fig. 2. Operating modes of the suggested switched-capacitor unit; (a) Mode 1, (b) Mode 2, (c) Mode 3

Table 1. Relation of on-state switches and output voltages

On-state switches	Output voltage	Capacitor state
S_2, S_5, Q_1, Q_2	$3V_{in}$	C_1, C_2 ↓
S_1, S_3, S_5, Q_1, Q_2	$2V_{in}$	C_1 ↓
S_1, S_3, S_4, S_6, Q_1, Q_2	V_{in}	C_1, C_2 ↑
Q_1, Q_3 or Q_2, Q_4	0	-
S_1, S_3, S_4, S_6, Q_3, Q_4	$-V_{in}$	C_1, C_2 ↑
S_1, S_3, S_5, Q_3, Q_4	$-2V_{in}$	C_1 ↓
S_2, S_5, Q_3, Q_4	$-3V_{in}$	C_1, C_2 ↓

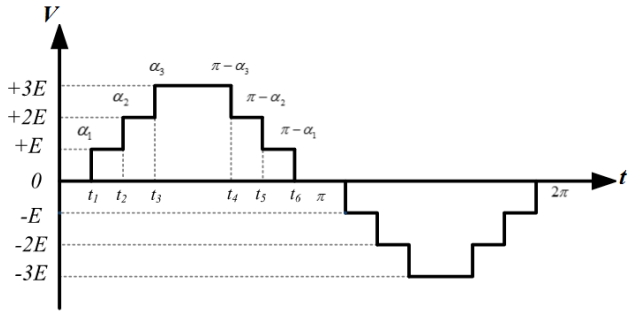


Fig. 3. Staircase modulation

fundamental and harmonic components are determined as given in (1) [30].

$$H_n = \begin{cases} 0 & n = 2k \\ \frac{4E}{n\pi} \sum_{j=1}^{s} \cos(n\alpha_j) & n = 2k+1 \end{cases} \quad (1)$$

Where E is the magnitude of the step waveforms, S is the number of voltage levels and α_j is the optimized switching angles of harmonics. The angles α_j are described by the coming equation:

$$\alpha_j = \sin^{-1}\left(\frac{j-.5}{S}\right) \qquad j = 1, 2, ..., S \quad (2)$$

THD of the output voltage is calculated as follows:

$$THD = \frac{\sqrt{\sum_{3,5}^{\infty} V_n^2}}{V_1} = \sqrt{\left(\frac{V_o}{V_1}\right)^2 - 1} \quad (3)$$

where

$$V_o = \frac{2\sqrt{2}E}{\pi} \sqrt{\sum_{n=1,3,5,...}^{\infty} \left(\sum_{j=1}^{S} \frac{\cos(n\alpha_j)}{n}\right)^2} \quad (4)$$

$$V_1 = \frac{2\sqrt{2}E}{\pi} \sum_{j=1}^{S} \cos\alpha_j \quad (5)$$

In (3)–(5), V_n and V_O are the RMS values of the h^{th} order component of the output voltage and V_O is the RMS value of the output voltage, respectively.

3. Circuit Elements Design

Determination of the capacitor size is essential to certify a lower ripple in the capacitor voltage. A large ripple in the capacitor voltage causes asymmetry in the output voltage levels. The maximum voltage ripple of the capacitor is X% of the charged capacitor voltage.

According to Fig. 2 and Fig. 3, capacitors C_1 and C_2 are parallel with the input voltage source and are charged in the time intervals [t_1, t_2] and [t_1, t_3]. The times t_1 to t_6 in Fig. 3 are determined as follow:

$$\begin{cases} t_i = {}^{\alpha_i}/_{18000} \ , & (i = 1, 2, 3) \\ t_j = {}^{\pi - \alpha_j}/_{18000} \ , & (j = 4, 5, 6) \end{cases} \quad (6)$$

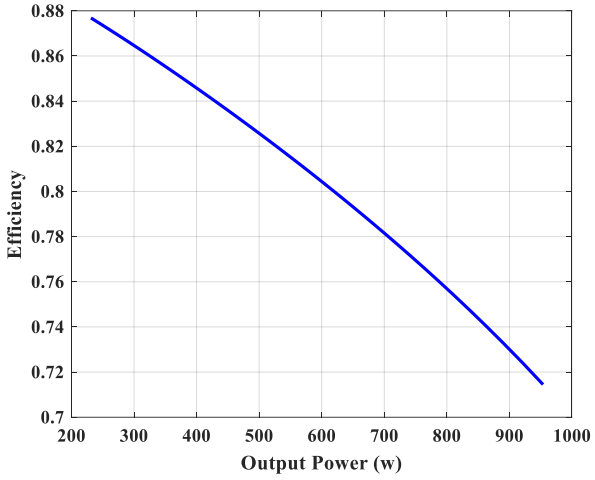


Fig. 4. Efficiency of proposed seven-level inverter

As illustrated in Fig. 3, the capacitor C_1 is discharged during time interval [t_2, t_5]. The discharge time of the capacitor C_2 is from t_3 to t_4, as shown in Fig. 3. Considering discharge time intervals of the capacitors, the capacitor's voltage ripples are approximated as follow:

$$\Delta V_{C_1} \simeq \left(\frac{1}{C_1}\int_{t_2}^{T/4} i_{C_1}(t)\,dt\right) \quad (7)$$

$$\Delta V_{C_2} \simeq \left(\frac{1}{C_2}\int_{t_3}^{T/4} i_{C_2}(t)\,dt\right) \quad (8)$$

Where ΔV_{C_1} and ΔV_{C_2} are the voltage ripple of capacitors C_1 and C_2 from t_2 to t_5, and from t_3 to t_4, respectively. Because the maximum voltage ripple is X% of charged capacitor, the capacitors size are determined as follow:

$$C_1 \geq \frac{1}{2V_{in}X\%}\int_{t_2}^{t_5} i_{C_1}(t)\,dt \quad (9)$$

$$C_2 \geq \frac{1}{2V_{in}X\%}\int_{t_3}^{t_4} i_{C_2}(t)\,dt \quad (10)$$

4. Power Loss Analysis

The power loss analysis and efficiency of the proposed inverter are studied in this section. In general, the main losses of switched-capacitor inverters, are related to capacitor losses, so in the proposed converter, analysis of switching power loss is the same as the analysis in [31], while the capacitor power losses consist of ripple loss, P_{rip}, and conduction loss, P_{cond} are different. When capacitor C_i connection changes from parallel to series, the ripple equals to difference of the input voltage, V_{in}, and the capacitor voltage, V_{ci}. The voltage ripple of capacitor C_i, ΔV_{rip} is given in (11).

$$\Delta V_{rip} = \frac{1}{C_i}\int_{t_-}^{t_+} i_{C_i} d(t) \quad (11)$$

where i_{Ci} is the capacitor C_i transient current, discharging time during is indicated using t_- to t_+, so in mode 2, t_2 to t_5 time interval represents the discharge time of the capacitor C_1. For capacitor C_2 in mode 3, t_- and t_+ are t_3 and t_4, respectively. The power loss of voltage ripple is equal to (12).

$$P_{rip} = \sum_{i=1}^{k} C_i \Delta V_{rip}^2 f_s \quad (12)$$

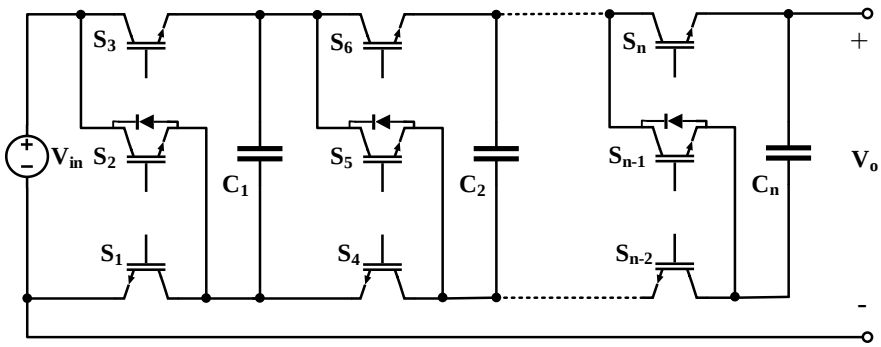


Fig. 5. Extended topology of proposed multilevel inverter; *N*-level topology

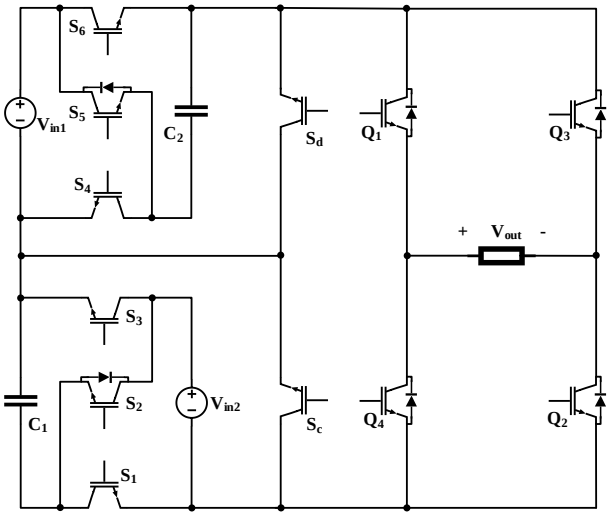


Fig. 6. Extended topology of the suggested multilevel inverter; 17-level configuration

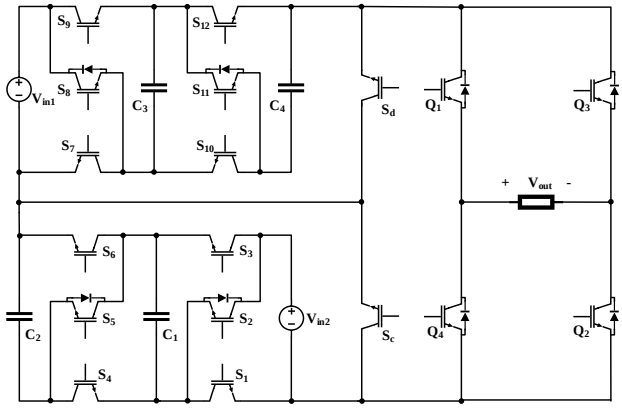


Fig. 7. Extended configuration of proposed multilevel inverter, 31-level configuration

Table 2. Switches state of specified output voltage level for 17-level configuration

On-state switches	Voltage level	Capacitor state
S_2, S_5	8E	C_1, $C_2 \downarrow$
S_2, S_4, S_6	7E	$C_2 \uparrow$, $C_1 \downarrow$
S_2, S_d	6E	$C_1 \downarrow$
S_1, S_3 , S_5	5E	$C_1 \uparrow$, $C_2 \downarrow$
S_1, S_3 , S_4, S_6	4E	C_1, $C_2 \uparrow$
S_1, S_3, S_d	3E	$C_1 \uparrow$
S_5, S_c	2E	$C_2 \downarrow$
S_4, S_6, S_c	E	$C_2 \uparrow$

where k denotes the count of switching capacitors, and f_s presents frequency of the output voltage. It's resultant that the ripple loss is directly related to the capacitor size. Also, the conduction loss is determined using (13).

$$P_{cond} = 2f_s \sum_{i=1}^{k} \int_{t_-}^{t_+} r_c i_{c_i}^2 dt \tag{13}$$

where r_c is equivalent series resistance (ESR) of the capacitor. A larger capacitor current increases the conduction loss. Finally, the total power loss of SCs is achieved as given in (14).

$$P_{sc} = P_{rip} + P_{cond} \tag{14}$$

From (12) and (13), it can be calculated that both ripple and conduction losses are related to frequency of the output voltage and the count of capacitors. Also, it's resultant that the larger size of capacitors improves the efficiency and lifetime of the capacitor. Yet, the larger size of capacitors increases the overall cost. So, a trade-off between efficiency and cost should be considered.

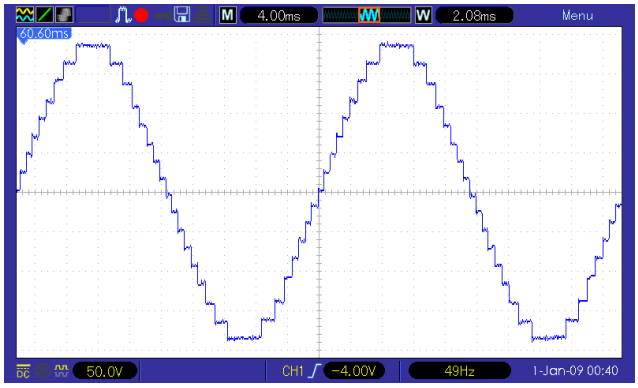
The efficiency of the proposed basic seven-level inverter at the power range of 200W to 900W is depicted in Fig. 4. This figure shows that the proposed inverter efficiency decreases with increasing in the output power due to the increase in power losses of the passive elements.

5. Extended Configuration of Proposed Multilevel Inverter

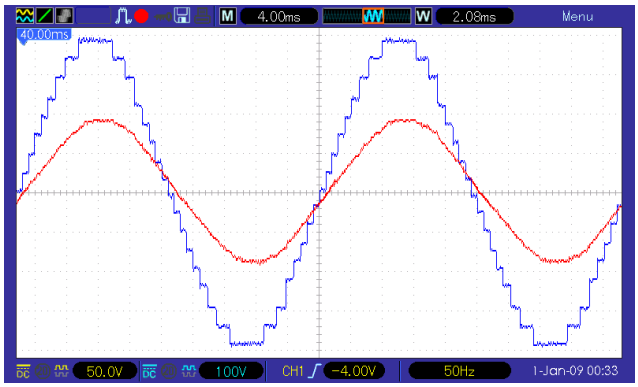
To achieve output voltage with a high number of levels, the proposed 7-level configuration can be expanded as given in Fig. 5. The introduced topology can be extended in series and parallel with connecting N_C number of capacitors C_1 to C_n utilizing switches S_1 to S_n. The required number of capacitors and switches for the generation of *N*-level voltage in the output are obtained as given in (15) and (16).

$$N_{sw} = (\frac{N-3}{2}) \times 3 \tag{15}$$

Fig. 8. Hardware setup



(a)



(b)

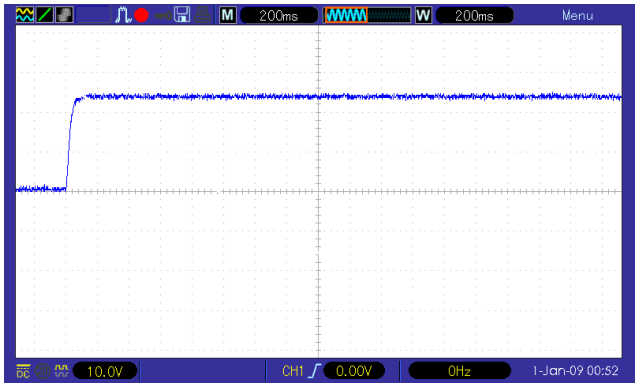
Fig. 9. Experimental test results; voltage and current waveforms of 17-Level inverters with (a) *R* Load, (b) Load *R-L*

$$N_C = (\frac{N-3}{2}) \tag{16}$$

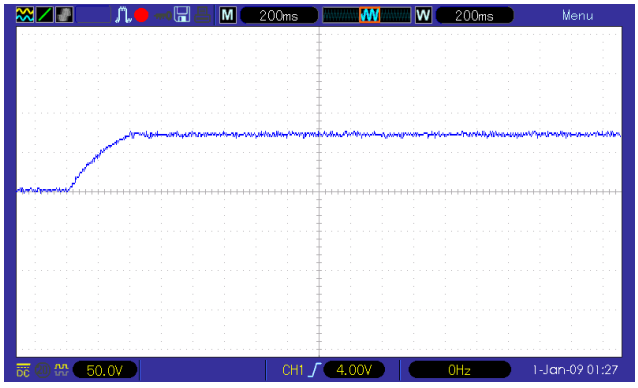
Similar to traditional cascaded multilevel inverters, the suggested multilevel converter can be implemented in symmetric and asymmetric topologies. In asymmetric configuration, as shown in Fig. 6, i.e., $V_{in_1} = E$and $V_{in_2} = 3E$. When two SC-based units operate together, 17 levels are generated in the output voltage. In another asymmetric configuration, as shown in Fig. 7, i.e., $V_{in_1} = E$ and $V_{in_2} = 4E$, so when two SC-based units operate together, 31 levels are generated in the output voltage.

5.1. 17-Level Topology of Proposed Inverter

As shown in Fig. 6, the 17-level configuration of proposed inverter consists of two SC-based units. Two unequal voltage



(a)



(b)

Fig. 10. Experimental test results; voltage waveforms of (a) Capacitor C_1, (b) Capacitor C_2

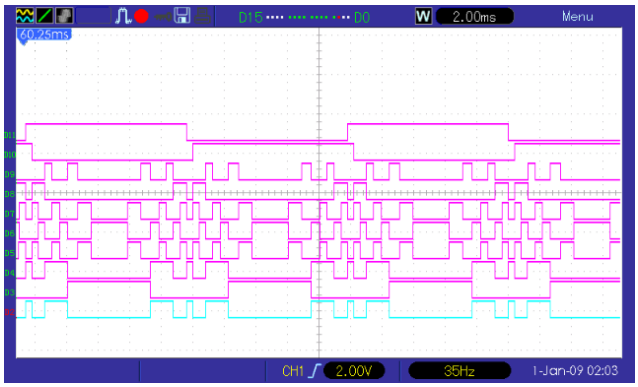


Fig. 11. Experimental test results; generated gate pulses for 17-Level inverter switches

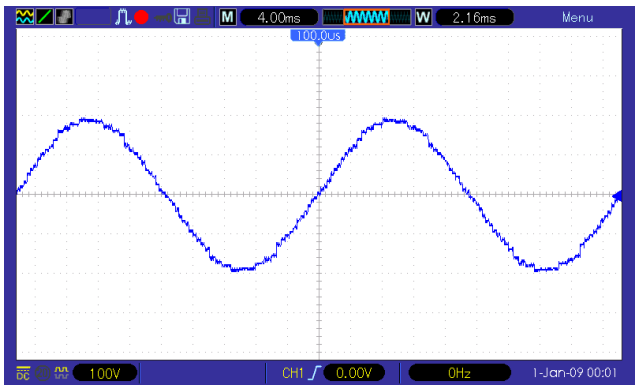
sources V_{in1}=E, V_{in2}=3E), two capacitors, and 12 switches are employed in this topology. In each of the switching states, by turning on or turning off the switches S_c and S_d, each of the SC-based units are connected in series and generate output voltage levels separately. Table 2 describes the switching states of the proposed configuration for positive half cycle. With operation of the H-Bridge unit, AC voltage is produced in the inverter output.

5.2. 31-Level Configuration of Proposed Inverter

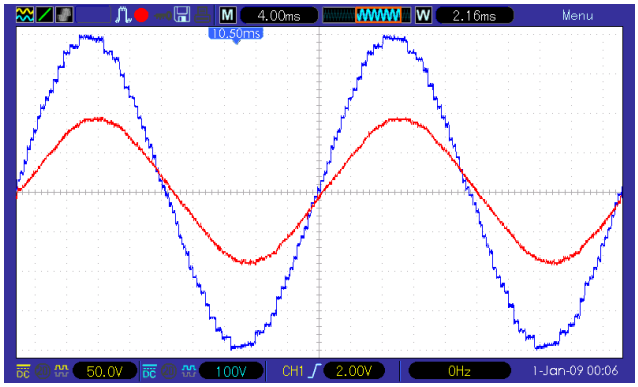
The suggested 7-level configuration can be expanded to get a higher number of voltage levels with unequal input voltage sources. Fig. 7 shows the 31-level extended configuration. The 31-level configuration consists of two SC-based units with unequal

Table 3. Switches state and output voltage level of 31-level inverter

On-state switches	Output voltage	Capacitor state
S_2, S_5, S_8, S_{11}	15E	$C_1 \downarrow$, $C_2 \downarrow$, $C_3 \downarrow$, $C_4 \downarrow$
S_2, S_5, S_7, S_9, S_{11}	14E	$C_1 \downarrow$, $C_2 \downarrow$, $C_3 \uparrow$, $C_4 \downarrow$
S_2, S_5, S_7, S_9, S_{10}, S_{12}	13E	$C_1 \downarrow$, $C_2 \downarrow$, $C_3 \uparrow$, $C_4 \uparrow$
S_2, S_5, S_d	12E	$C_1 \downarrow$, $C_2 \downarrow$
S_1, S_3, S_5, S_8, S_{11}	11E	$C_1 \uparrow$, $C_2 \downarrow$, $C_3 \downarrow$, $C_4 \downarrow$
S_1, S_3, S_5, S_7, S_9, S_{11}	10E	$C_1 \uparrow$, $C_2 \downarrow$, $C_3 \uparrow$, $C_4 \downarrow$
S_1, S_3, S_5, S_7, S_9, S_{10}, S_{12}	9E	$C_1 \uparrow$, $C_2 \downarrow$, $C_3 \uparrow$, $C_4 \uparrow$
S_1, S_3, S_5, S_d	8E	$C_1 \uparrow$, $C_2 \downarrow$
S_1, S_3, S_4, S_6, S_8, S_{11}	7E	$C_1 \uparrow$, $C_2 \uparrow$, $C_3 \downarrow$, $C_4 \downarrow$
S_1, S_3, S_4, S_6, S_7, S_9 , S_{11}	6E	$C_1 \uparrow$, $C_2 \uparrow$, $C_3 \uparrow$, $C_4 \downarrow$
S_1, S_3, S_4, S_6, S_7, S_9, S_{10}, S_{12}	5E	$C_1 \uparrow$, $C_2 \uparrow$, $C_3 \uparrow$, $C_4 \uparrow$
S_1, S_3, S_4, S_6, S_d	4E	$C_1 \downarrow$, $C_2 \downarrow$
S_8, S_{11}, S_c	3E	$C_3 \downarrow$, $C_4 \downarrow$
S_7, S_9, S_{11}, S_c	2E	$C_3 \uparrow$, $C_4 \downarrow$
S_7, S_9, S_{10}, S_{12}, S_c	E	$C_3 \uparrow$, $C_4 \uparrow$



(a)



(b)

Fig. 12. Experimental test results; voltage and current waveforms of 31-Level inverters results (a) *R* Load, (b) *R-L* load

voltage sources that V_{in1}, V_{in2} are equals E and 4E, respectively. The proposed topology needs two unequal voltage sources, four capacitors, and 18 switches. The charging and discharging states of capacitors and switching states for different output voltage levels in the positive half cycle are given in Table 3. The output AC voltage waveform is obtained with the operating of the H-bridge converter.

6. Comparison Study

To evaluate merits of the proposed multilevel inverter, it is compared with the recently proposed SC-based single DC source multilevel inverter structures. The considered SC multilevel inverters for the comparison with the proposed multilevel inverter has the following characteristics: 1) Use a single DC input voltage source

Table 4. Comparison summary of various single DC source SC multilevel inverter topologies

	N_L	N_{sw}	N_c	N_{gd}	$TSV_{(P.U)}$	B
[24]	7	10	3	8	5.3	1.5
[19]	7	9	3	8	5.3	1.5
[20]	7	9	3	9	5.3	1.5
[32]	7	10	3	9	6	1.5
[33]	7	9	3	8	5.67	1.5
[21]	7	10	4	8	7.3	1.5
[34]	7	11	2	11	5.67	3
[35]	7	12	2	12	5.3	3
[36]	7	16	2	14	5.3	3
Proposed topology	7	10	2	10	4.33	3

Table 5. Table 5 Prototype circuit elements values

Parameter	**value**
17-level Input DC sources	V_{in1}=25, V_{in2}=75
31-level Input DC sources	V_{in1}=15, V_{in2}=60
MOSFETs	IRFP260n
Output frequency	f_o=50 Hz
Opto-coupler	TLP250
Capacitances	C_1=C_2=C_3=C_4=4700f
Load	R=100Ω, L=50mH
Microcontroller	Atmega8a

2) Capacitor voltage equality with the input voltage source To certify the features of the proposed SC multilevel inverter, the basic 7-level configuration is compared with the newly presented topologies from various aspects in Table 4. The number of output voltage levels, N_L, number of switches, N_{sw}, number of capacitors, N_c, number of gate drivers, N_{gd}, total voltage stress of switches (TSV), and output voltage boost factor (B) are the comparison items. The comparison results indicate that the introduced inverter in [21] uses four capacitors, and the proposed inverters in [19, 20] and [33, 34] use three capacitors to produce a 7-level output voltage while the proposed inverter uses only two capacitors. The number of switches applied in the proposed 7-level inverter is 10 while the given inverters in [34–36] require 11, 12, and 16 switches, respectively. It's concluded that the suggested topology, in comparison to the inverters presented in [19–21], [34–36], in addition to produce higher or equal voltage gain, imposes lower total voltage stress on the semiconductor elements.

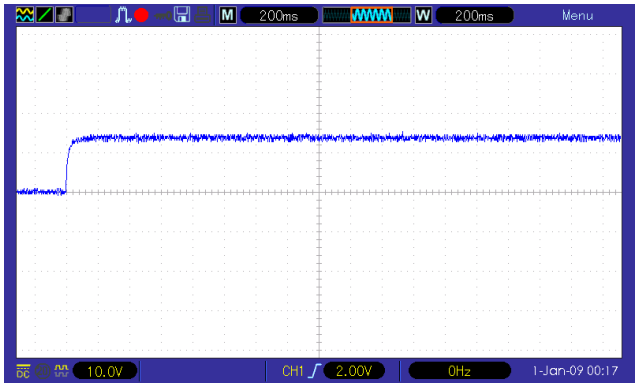
7. Experimental Test Measurements

To confirm operation of the introduced multilevel inverter, laboratory test results of 17-level and 31-level topologies, implemented in the laboratory scale, are presented in this section. To generate switching pulses, the nearest level modulation strategy utilizing Atmega8a microcontroller is applied. The values of the elements used in the implemented configurations are listed in Table 5 and also, the implemented prototype used for testing the suggested multilevel inverter in 200W is illustrated in Fig. 8.

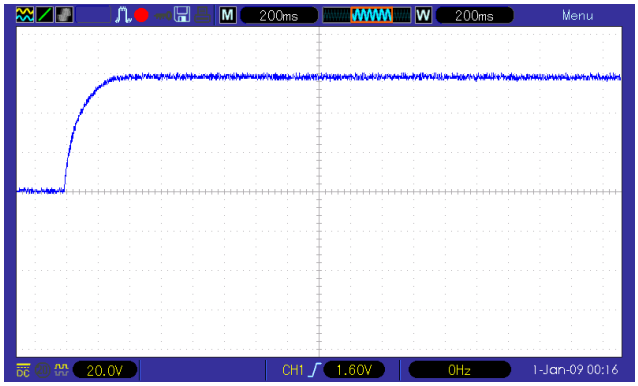
Fig. 9 shows voltage and current waveforms of 17-level structure for resistive (*R*) and resistive-inductive load (*R-L*). It is clear that the number of output voltage steps is 17, validating the 17-level operation. As shown in fig. 9(b), according to the resistive-inductive load, the current waveform is almost sinusoidal and has a phase difference with the voltage waveform.

The voltage waveforms of capacitors C_1 and C_2 are given in Fig. 10. According to this figure, the capacitors are charged to the input DC voltage. Also, the results show that the capacitor voltage ripples are in the admissible range.

The gate pulses generated from NLC control method for switches $S_1 \sim S_6$, S_c and S_d, Q_1 and Q_4 in two switching cycles are shown



(a)



(b)

Fig. 13. Experimental test results; capacitors voltage of 31-level configuration (a) C_1&C_2, (b) C_3&C_4

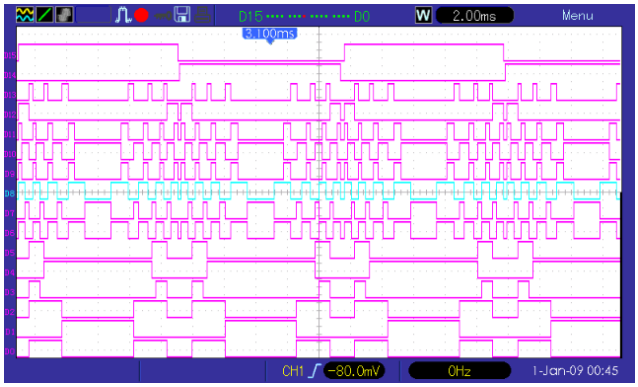


Fig. 14. Experimental test results; generated gate pulses for switches of 31-Level inverter

in Fig. 11.

As given in Fig. 4, when two units of 7-level configuration are connected in series with asymmetric input sources, the 31-level configuration is created. Fig. 12 illustrates experimental test results of the output voltage and current waveforms for *R* and *R-L* loads of the 31-level configuration. It is clear that by increasing the number of output levels to 31, the voltage and current waveforms become closer to sinusoidal waveforms.

The voltage waveforms of capacitors $C_1 \sim C_4$ are shown in Fig. 13, which indicates that the capacitors are charged to input DC voltage sources and have very low ripples.

Fig. 14 shows the waveforms of the gate pulses generated for switches of 31-Level configuration.

8. Conclusion

A novel multilevel inverter based on switched-capacitor configuration with boosting ability is introduced in this research. The presented converter can produces 7 levels in the output voltage utilizing only a single DC input voltage source with boost factor of 3. The nearest level modulation method is applied to generate pulses for the switches. The extended topologies of the introduced SC multilevel inverter in symmetric and asymmetric topologies are presented which produce 17-level and 31-level voltage waveforms. A comparison between the introduced multilevel inverter and similar structures is given to show superiorities of the proposed multilevel inverter. Eventually, a laboratory scale setup of the suggested inverter was implemented and tested to confirm its performance.

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