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A Generalized Modular Multilevel Current Source Inverter

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Abstract-*This paper proposes a novel topology of multilevel current source inverter which is suitable to apply in low/medium voltage. The proposed topology is capable of producing desirable bidirectional output current levels. Furthermore, it can employ symmetrical DC current sources as well as asymmetrical ones which is a significant advantage. Asymmetrical mode makes it possible to generate a great number of output levels by appropriate selection of DC current source magnitude, needless to make changes in the hardware of the inverter. As a result, various methods are presented to compute the magnitude of needed DC current sources. In comparison to the conventional H-Bridge inverter (CHB), the proposed inverter has lessened the number of required DC current sources, switches as well as related gate driver circuits. The reduced number of required components has leads to cost and volume advantages. In addition, the control layout has become simpler. Reduction of power loss as a result of reduced number of on-state switches is the other merit of the proposed inverter. To evaluate the efficiency of the proposed inverter, its simulation and experimental results are extracted including results of various methods of determining DC current source magnitude.*

Keywords: Multilevel current source inverters, Symmetric inverter, Asymmetric inverter, Reduced number of circuit devices, Power loss.

1. INTRODUCTION

Introduction of the multilevel inverter by Nabae et al. [1] has led to utilization of multilevel inverters instead of electronic power conversion. As a practical power electronic device, owning high quality of output waveforms along with high efficiency has made multilevel inverter suitable to be used in industrial [2]. The main merits of multilevel inverter include improvement of power quality and electromagnetic compatibility, less harmonic, lower value of dv/dt and di/dt as well as switching losses. These advantages are resultant from staircase structure of output voltage/current which is generated by various DC links. By increment of DC links number, the output waveforms include lower degree of harmonics and become almost sinusoidal [3].

Multiple international standards such as IEEE-929, IEEE-1547, and EN-61000-3-2 have explained more in detail output power quality of inverter *i.e.* Harmonic spectra and etc. along with THD of output voltage/current. The modulation strategy has an effect on the operation of multilevel inverters. As a result, by the introduction of multilevel inverters, various switching techniques have been proposed for different kind of multilevel inverters in order to improve their efficiency as well as power quality [4-6]. Among the switching methods, PWM (Pulse width modulation) and SVM (space vector modulation) are the most commonly used ones in the industrial [7].

Based on the structure of inverters, the DC sources can be connected or islanded [8]. For example, in [9], a novel voltage source multilevel converter is proposed with is composed of series connection of a number of the proposed basic multilevel units. Also, five different algorithms are proposed to determine the magnitude of DC voltage sources in this paper. Reduction of the power switches and the different magnitudes of DC voltage sources are two main advantages of this topology. Furthermore, multilevel inverters can be considered as one of the notable technologies of flexible AC transmission systems devices [10] and renewable energy

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resources [11]. The multilevel inverters can be categorized into two classes including multilevel voltage source inverters (MVSI's) and multilevel current source inverters (MCSI's). The first category is able to transfer AC current waveform from DC current power source to the load. However, the latter one owns DC voltage links and can generate AC voltage waveform. Generally, distributed generation units such as photovoltaic panels need to convert generated DC power into AC power which is performed through grid-connected inverters. MCSI is suitable to provide the connection between AC and DC side of power grid whose control is simpler than MVSI. Buffering the output current from grid voltage fluctuation, generating a predestine current to the power grid in absence of AC current feedback loops and having high power factor operation are the other advantages of grid-connected MCSI. Moreover, its output current has less dependency on the grid voltage and it can protect against short circuits, innately [12]. The application of CSC includes megawatt motor drive due to its transformer-less and four quadrant operation [13], grid integration without AC feedback due to direct output current control [14], high-voltage DC (HVDC) and flexible AC transmission system (FACTS) due to inherent short circuit protection with longer mean time between failure (MTFB) [15], and operation in weak grids due to independent control of active and reactive power. The multilevel CSI can replace two stage fuel-cell grid integration as it performs both maximum power point tracking as well as grid integration [16]. In [17], the topology of paralleled H-bridge multilevel converter has been proposed for multi-string configuration and dc-dc module-integrated configuration with centralized inverter.

The multilevel current waveform can be produced by paralleling multiple three-level H-Bridge CSIs. The requirement to a large number of circuit devices is the drawback of conventional H-Bridge inverter (CHB) similar to its peer. The other disadvantages of CHB inverter can be named as large number of isolated DC current sources and power switches in addition to gate drive circuits [18].

The dual of flying capacitor based full bridge MVSI is the other method which is a multi-cell structure based MCSI. However, existence of bulky intermediate inductors is the weak point of this structure which leads to complication of balancing control of intermediate current level [19]. In spite of proposing various techniques to yield this difficulty, utilization of cumbersome inductors is expensive and restricts the application of this MCSI kind [19]. Another MCSI is proposed in [20] based on applying a single rating inductor cell topology while it is the dual of the improved diode clamped MVSI. This structure needs giant inductors to firm alternative currents to avoid high losses and less efficiency of power conversion.

In [21], modular symmetric and asymmetric reduced count switch multilevel current source inverter is formed by H-Bridge converter and "current cell". Each current cell has two IGBTs.

Current source modular multilevel converter has been proposed recently in [22]. This topology is composed of inductor modular cells. In this topology, to control the output current, the half-bridge and full-bridge cell are inserted or bypassed in each arm of the converter. A MCSI using inductor cell connected to H-Bridge in [23]. This topology does not require multiple isolated DC current sources. However, this topology includes costly, high volume and multi rating inductor.

Unfortunately, less MCSI topologies are proposed up to now and a great effort is needed for this issue. In addition to advantages of multilevel inverters, there exist various drawbacks, too. The most important drawback is requirement to a high number of power devices including DC current source, power switches along with related gate drive circuits. Since expensiveness of DC current sources, decreasing the number of required sources leads to reducingtotal cost. In other words, a great amount of current source inverter is related to the cost of DC current sources. In addition, the number of power switches has a great effort on the total cost. Applying a large number of power devices in the construction of inverter makes the circuit more complicated and needy to control scheme which leads to expensiveness of inverter and reduction of its reliability and efficiency [23]. As a result, it is necessary to reduce circuit device number and propose a new multilevel inverter structure to reach better performance by reducing circuit components. This paper proposes a novel multilevel current source inverter which is suitable for high steps and has a lower number of circuit components. The proposed structure is suitable for low/medium power appliances while its control layout is as simple as the cascaded multilevel inverter and is capable of being applied symmetric and asymmetric inverter. Moreover, different methods have been presented to compute the value of DC current sources. A significant increment in the number of inverter output levels can be reached by suitable selection of DC sources magnitude and needless to retouch its hardware. Finally, the gained simulation and experimental results approve merits of the proposed multilevel inverter. The rest of the

paper is organized as follows: The proposed topology is explained in Section 2. In Section 3, results of the proposed inverter are compared with results of the conventional CHB. The simulation and experimental results are presented in Section 4. Lately, total achievements of the paper are concluded in Section 5.

2. Configuration, Specification and Basic Operation Principles of Proposed Topology

The required circuit devices are one of the main issues that multilevel inverters are dealt with. It is common that the number of required components and output current levels are related to each other. It means that by an increment in output current level, the number of circuit components will increase too. The switches and relevant gate drive circuits as the basic parts of converters are supplied through DC power sources. The proposed structure is constructed by paralleling multiple general modules while per module is composed of several cells as well as H-bridge inverter that are connected to the cells in a suitable manner. The combination of DC current source along with a pair of semiconductor unidirectional switch makes cells while four semiconductor unidirectional switches have formed H-bridge inverter. Unlike MVSI, the IGBT as a unidirectional switch in the structure of MCSI is needless of anti-parallel fast recovery diode. Different methods are explained in the following to specify the number of modules, cells and magnitude of DC current sources. Fig. 1(a) depicts total perspective of the general module. The proposed scheme is able to generate positive and negative output signals using various paths. Also, each current source can be provided with one DC voltage source, an IGBT (Q_c) and one inductor as shown in Fig. 1(b). The power switch is used to control current of each inductor independently. Consequently, symmetric and asymmetric DC current sources can be generated with this method.

The summation of output current values for different cells is considered as the stepwise output signal of per module. By applying H-bridge inverter, all current steps considering positive, negative and zero values can be determined for each module. This paper proposes various methods to specify the magnitude of the DC current source for the proposed inverter. All of these methods are able to generate any output current level. Since, the parameters *m* and *n* are utilized so common, it is defined here. The proposed module owns *m*-modules while n_j is the cell number of j^{th} module and *i* is the cell number of j^{th} module with n_j cells.

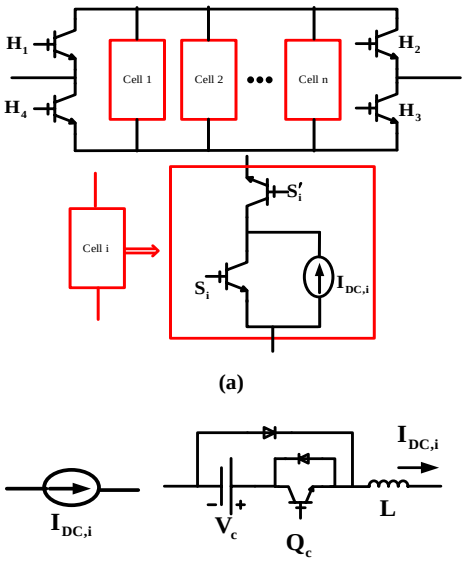


Fig. 1.(a)The basic schematic of general module (b) realization of DC current source.

A. First Method

In the first method a module (m=1) along with various cells ($n_1 \geq 1$) is taken into account. This method can be named as symmetric mode since the current magnitude of all DC sources is the same as I_{dc}. Based on the desired level of output current, n can be changed. Switch number of this method in the proposed converter is calculated as follows:

$$N_{Switch} = 2n_1 + 4 \quad (1)$$

Where $n_1$is the number of cells.

$$N_{Switch} = N_{driver} \quad (2)$$

While, N_{Switch} and N_{driver} are the number of switches and gate drivers, respectively. The output current is reached by combining the individual currents of DC sources. As a result, $I_{o,max}$ which is calculated by summation of the magnitude of DC sources is considered as the upper limit of current. The proposed method to compute $I_{o,max}$ is expressed in Eq. (3) as bellow:

$$I_{o,\max} = \sum_{i=1}^{n_1} I_i = n_1 \times I_{dc} \quad (3)$$

The following equation can determine the number of current levels (l):

$$l = 2n_1 + 1 \quad (4)$$

The semiconductor device power (SDP) is a vital index for multilevel inverters which can be calculated for all switches using the equation bellow:

$$SDP = \sum_{k=1} SDP_{Switch_k} = \sum_{k=1} V_{Switch_k} \times I_{Switch_k} \quad (5)$$

Utilizing the above-mentioned equation, the SDP value for this method is as follows:

$$SDP^{p.u.} = 6n_1 \quad (6)$$

The circuit topology of the first method for a 5-level inverter is shown in Fig. 2. The converter is composed of two DC current source along with eight switches. It can be seen that the converter has one module (m=1) while the cell number is equal to two.

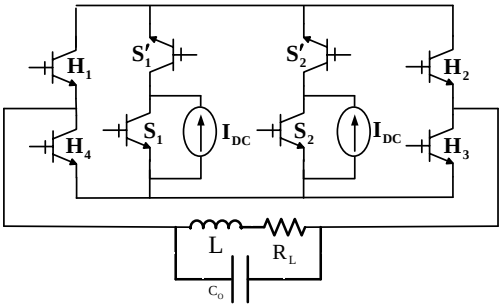


Fig. 2. Schematic of 5-level proposed MCSI according to First Method.

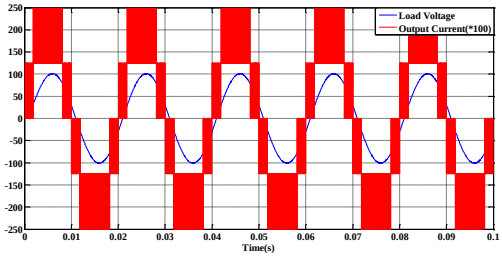
The suggested inverter is able to generate five positive negative and zero levels. The switching states proportional to each level of output current are expressed in Table 1 while 1 and 0 denote for ON and OFF states of the switch.

Table 1. Switching states of the represented module according to the first method

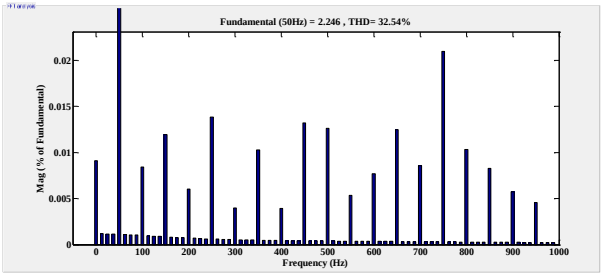
Output Current	S_1	S_2	H_1	H_2	H_3	H_4
$2I_{dc}$	0	0	0	1	0	1
I_{dc}	1	0	0	1	0	1
0	1	1	0	1	0	1
$-I_{dc}$	1	0	1	0	1	0
$-2I_{dc}$	0	0	1	0	1	0

The effective performance of the proposed symmetric inverter is proofed using simulation results for a 5-level test case as depicted in Fig. 2. As can be seen, the maximum value of staircase signal is 2.5 A. The simulation results are extracted using MATLAB/-Simulink software. The load is composed of a series resistive-inductive in parallel with a capacitor by the magnitude of 47 Ω, 8 mH and 25 µF, respectively. In addition, the load's inductor (L) and output capacitor (Co) plays as filter role. Existence of capacitor is inevitable for two reason: the harmonic components of the PWM current will flow through the filter capacitor and Due to existence of inductive load, the filter capacitor is required to avoid from the sudden current changes. The calculation of output filter capacitor is presented in [21]. The output signals related to output current and voltage for the 5-level symmetric case are shown in Fig. 3.

It can be concluded from Fig. 3 that utilizing the first method, the proposed converter is able to produce all current steps for a 5-level case study. By the way, the experimental results of output current and voltage for the 5-level test case using the symmetric structure are shown in Fig. 4.



(a)



(b)

Fig. 3. Simulation results: a) output current and voltage waveform b) harmonic content of output current; of the symmetric 5-level proposed inverter according to the first method

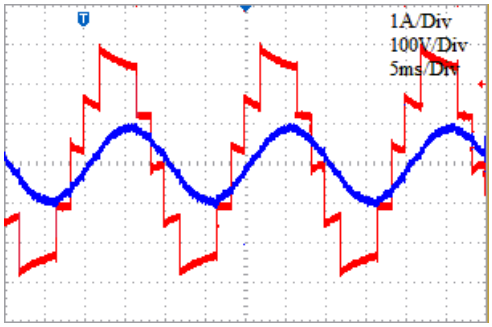


Fig. 4. Experimental results of the symmetric 5-level proposed inverter according to the first method

It is clear that these figures are so close to each other and the existed difference between simulation and experimental results are because of voltage drop on the switches.

B. Second Method

The asymmetric form of the first method is discussed in this subsection. Using this mode, the favorable number of output levels can be reached by choosing appropriate magnitude of DC source without making any change in

the hardware structure of the inverter. Applying asymmetrical DC sources is more helpful than increasing the circuit components. Here, a module (m=1) along with multiple cells are taken into account. n_1 is cells number while the magnitude of DC sources are chosen based on a geometric progression with a factor of two. The proportional value of DC sources in this mode with n_1 cells and I_{dc} as the minimum value of DC current source, is computed as bellow:

$$I_i = 2^{i-1} I_{dc} \quad (7)$$

Where i is the cell number and i=1, 2... , n_1. Equations (1) and (2) are correct for this method, too. The maximum output current ($I_{O,max}$), the number of current levels (l) and the SDP value in this method are as following, respectively:

$$I_{o,\max} = \sum_{i=1}^{n_1} I_i = (2^{n_1} - 1) I_{dc} \quad (8)$$

$$l = 2^{n_1+1} - 1 \quad (9)$$

$$SDP^{p.u.} = 6(2^{n_1} - 1) \quad (10)$$

The circuit schematic for the 7-level asymmetric inverter is shown in Fig. 5. Its prototype is composed of two DC current source along with eight switches. It can be seen that the prototype has one module (m=1) while the cell number is equal to two.

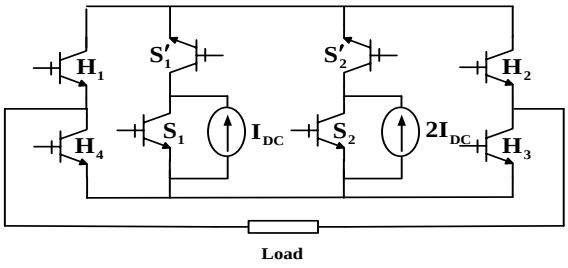


Fig. 5. The overall view of 7-level symmetric inverter according to the second method

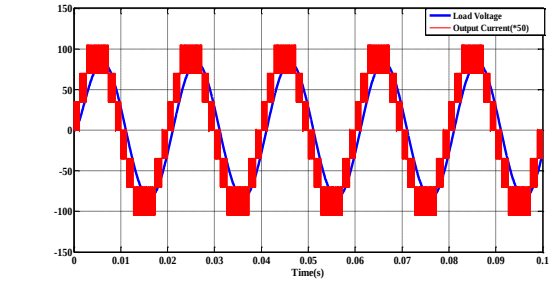
Switching states proportional to each output current value are expressed in Table 2.

Figure 6 illustrates the current and voltage signals along with the harmonic components for the 7-level test case in the proposed asymmetric inverter while Idc is 10A.The introduced method is able to generate a staircase signal with whose peak value is 2.1 A while load parameters are 47 Ω, 0.8 mH and 25 µF.

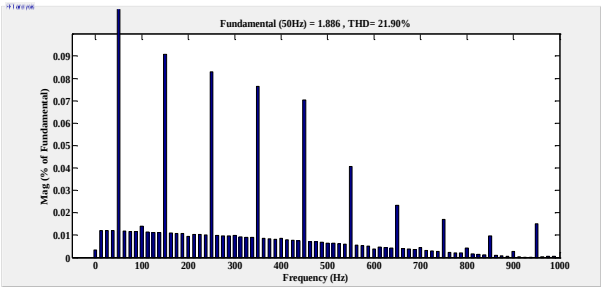
Figure 6 proves the second method is appropriate to generate all current steps for a test case 7-level asymmetric inverter through an asymmetric converter while output signals of current and voltage for this 7-level case are shown in Fig.7.

Table 2. Switching states of represented module according to the second method

Output Current	S_1	S_2	H_1	H_2	H_3	H_4
$3I_{dc}$	0	0	0	1	0	1
$2I_{dc}$	1	0	0	1	0	1
I_{dc}	0	1	0	1	0	1
0	1	1	0	1	0	1
$-I_{dc}$	0	1	1	0	1	0
$-2I_{dc}$	1	0	1	0	1	0
$-3I_{dc}$	0	0	1	0	1	0



(a)



(b)

Fig. 6. Simulation results: a) Output current and voltage waveform b) harmonic content of output current; of symmetric 7-level proposed inverter according to the second method

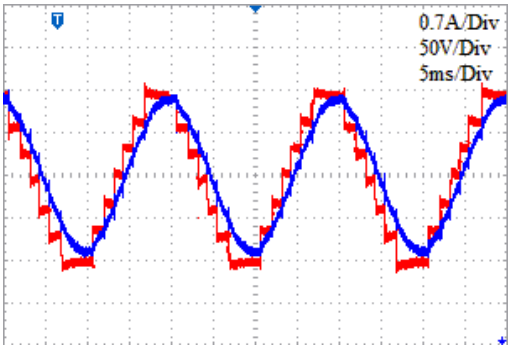


Fig. 7. Experimental Results: asymmetric 7-level proposed inverter according to the second method

It can be concluded from the figures that the simulation and experimental results are well coordinated.

C. Third Method

The number of output levels can be increased by increment of module and cell number at the same time. Unlike previous methods, module number is not unit here. Furthermore, any output current level ($m \geq 1$ & $n \geq 1$) can be reached by modifying value of m & n and this is why this method is named as the generalized mode.

Moreover, in this mode DC sources magnitude are changed to reach more output levels in comparison to the second method. To reach this goal, the magnitude of DC current sources are chosen based on geometric progression with a factor of two. The magnitude of DC source in a specific module is P-times of the last module. P is a function of module and cell number. The magnitude of DC sources proportional to each module can be computed using Eq. (11):

$$I_{ji} = 2^{i-1} I_{Basic_j} \tag{11}$$

Where $I_{Basic,j}$ is the value of smallest DC current source in j-th module and $I_{Basic,1}$ is the same as I_{dc}. P can be determined using the following equation:

$$P_j = (2\sum_{x=1}^{j-1}\sum_{i=1}^{n_j} I_{xi}) + 1 \tag{12}$$

So, the value of smallest DC current source in *j*-th module can be computed using Eq. (13):

$$I_{Basic_j} = P_j \times I_{Basic_{j-1}} \tag{13}$$

The number of desired switches for the proposed converter in this method is computed as bellow:

$$N_{switch} = \sum_{j=1}^{m} (2n_j + 4) \tag{14}$$

While the number of gate drives is by Eq. (2).

The maximum value of output current ($I_{o,max}$), the number of current levels (l) as well as theSDP in the defined method, are given in the following equations, respectively:

$$I_{o,\max} = \sum_{j=1}^{m}\sum_{i=1}^{n_j} I_{ji} \tag{15}$$

$$l = 2\frac{I_{o,\max}}{I_{dc}} + 1 \tag{16}$$

$$SDP^{p.u.} = \sum_{j=1}^{m} 6(2^{n_j} - 1)\frac{I_{Basic_j}}{I_{dc}} \tag{17}$$

The circuit schematic for the 21-level inverter is shown in Fig. 8. Its prototype is composed of three DC current source along with fourteen switches. It can be seen that the prototype has two modules (m =2) while the cell number for both modules is equal to two.

Switching states proportional to each output current value for the21-level case are expressed in Table 3.

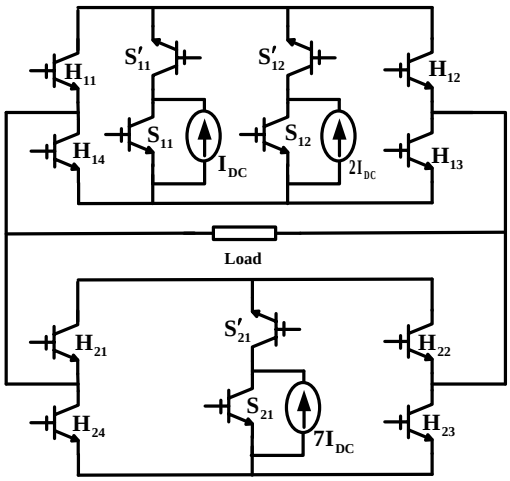


Fig. 8. The overall view of 21-level inverter according to third Method

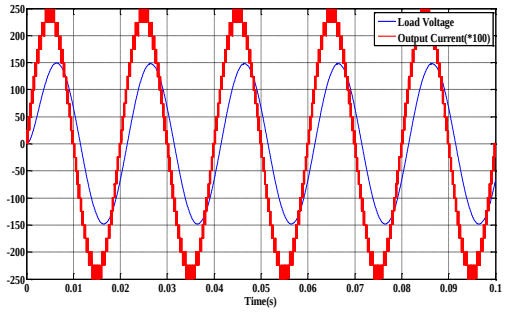
Table 3. Switching states of the represented module according to the third method

Output current level	S_{11}	S_{12}	H_{11}	H_{12}	H_{13}	H_{14}	S_{21}	H_{21}	H_{22}	H_{23}	H_{24}
$10I_{dc}$	0	0	0	1	0	1	0	0	1	0	1
$9I_{dc}$	1	0	0	1	0	1	0	0	1	0	1
$8I_{dc}$	0	1	0	1	0	1	0	0	1	0	1
$7I_{dc}$	1	1	0	1	0	1	0	0	1	0	1
$6I_{dc}$	1	0	1	0	1	0	0	0	1	0	1
$5I_{dc}$	0	1	1	0	1	0	0	0	1	0	1
$4I_{dc}$	1	1	1	0	1	0	0	0	1	0	1
$3I_{dc}$	0	0	0	1	0	1	0	0	1	1	0
$2I_{dc}$	1	0	0	1	0	1	0	0	1	1	0
I_{dc}	0	1	0	1	0	1	0	0	1	1	0
0	0	0	0	1	1	0	0	0	1	1	0
$-I_{dc}$	0	1	1	0	1	0	0	0	1	1	0
$-2I_{dc}$	1	0	1	0	1	0	0	0	1	1	0
$-3I_{dc}$	0	0	1	0	1	0	0	0	1	1	0
$-4I_{dc}$	0	0	0	1	0	1	0	1	0	1	0
$-5I_{dc}$	1	0	0	1	0	1	0	1	0	1	0
$-6I_{dc}$	0	1	0	1	0	1	0	1	0	1	0
$-7I_{dc}$	0	0	0	1	1	0	0	1	0	1	0
$-8I_{dc}$	0	1	1	0	1	0	0	1	0	1	0
$-9I_{dc}$	1	0	1	0	1	0	0	1	0	1	0
$-10I_{dc}$	0	0	1	0	1	0	0	1	0	1	0

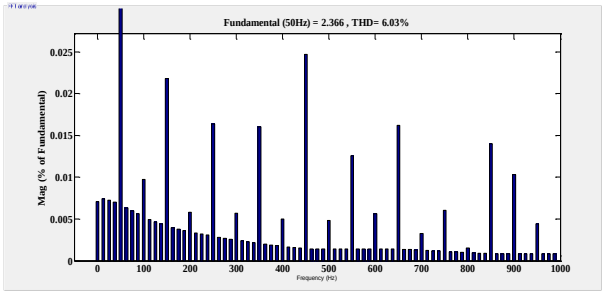
The current and voltage waveforms along with their harmonic portion in generalized mode are demonstrated in Fig. 9. The proposed inverter is able to produce a staircase whose peak value is 2.5 A while load parameters are 70Ω, 10mH and 25μF.

The abovementioned figures confirm validity and effectiveness of the proposed inverter during simulation and experimental test.

Validation results of the suggested generalized multilevel inverter in generating 21-level current steps are shown in Fig. 9. Furthermore, Fig. 10 illustrates output signals of current and voltage for the21-level case.



(a)



(b)

Fig. 9. Simulation results: a) Output Current and voltage waveform b) harmonic content of current of symmetric 21-level proposed inverter according to the second method

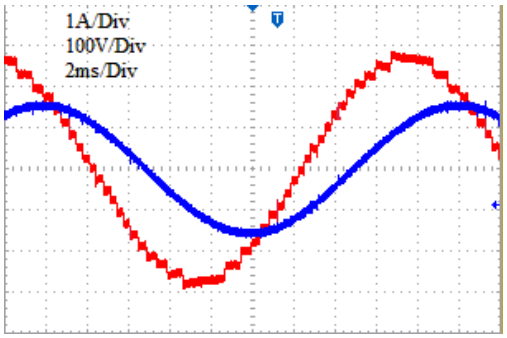


Fig. 10. Experimental results of generalized multilevel inverter for 21-level case

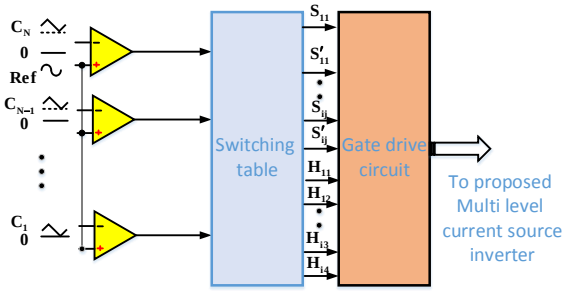


Fig.11. LSPWM scheme for proposed converter

3. Switching Strategy

One of the popular switching methods for multilevel inverters is Level Shifted Pulse Width Modulation (LS-PWM). By implementing the switching table and LS-PWM method, the proposed converter is controlled as shown in Fig.11. The *Sij* and *S'ij* are switched with carrier frequency and the *H*-Bridge switches are switched in line frequency.

4. Comparison Study

As mentioned above, great number of power devices is the main disadvantage of multilevel inverters. This drawback makes the hardware more complicated and necessitates utilizing a more complex control scheme which leads to an unreliable and more expensive inverter. As a result, the main goal of the design is to reduce the number of circuit devices. It is welcomed to suggest a new structure for the multilevel inverter which has better performance and a lowernumber of circuit devices. This section of the paper proposes a comparison between the vital parameters of the presented multilevel converter and some other traditional and recently proposed topologies. A complete comparison is done for all methods. Furthermore, conventional symmetric *H*-Bridge inverter (CHB), conventional asymmetric *H*-Bridge inverter (ACHB) and presented topologies of [14] and [21] are taken into account during comparison process to highlight merits of the proposed converter. The comparison conditions are identical for all of the inverters by using the same number of output levels and maximum level of output current. As DC current sources are expensive, it is so economical to use less number of them. In other words, a large section of inverter total cost is formed by great number of DC current sources. The performed comparisons approve that the presented MCSI has reduced the number of DC current sources in the generalized mode compared with its other modes as well as CHB and ACHB and [21] and [14]. The number of DC current sources of [14] is greater than other topologies. By the way, the number of needed switches is effective in the overall cost of the inverter. It means that the proposed inverter requires lower number of switches to generate the same level of output. In addition, the number of switches in the generalized and second modes are close to each other. It is evident that the CHB, first mode and [14] have more switches in comparison to other topologies, respectively. Since the number of required switches are reduced in the suggested inverter and necessity of one gate driver for each switch, the proportional gate drive circuits are reduced, too. So, the total expenses and installation area are reduced by reduction of components. However, the power rating of switches is an important issue due to its effect on the cost of the inverter. The ratings of power switches are selected in such a way to be suitable for low/medium power applications. In addition, the number of applied switches has more importance than their power rating.

Considering the merits of the proposed inverter along with its application and reduction in the number of switches, a little increment in the total SDP of the system in comparison to SDP of CHB and ACHB can be neglected. The SDP of [21] is close to proposed topologies. The whole value of power loss which is related to the number of ON-state switches is considered as another remarkable parameter to perform a comparison between the presented and conventional inverters. Conduction losses which are resultant from equivalent resistance and voltage drop on the switches as well as switching losses which are related to the non-ideal operation of them, are two main types of power losses. Half of the switches for the conventional MCSI and the proposed converter are ON. Lower number of ON-state switches in compared with conventional and [14] and [21] leads to lower value of conduction losses. The number of power switches versus the output level is shown in Fig. 12.

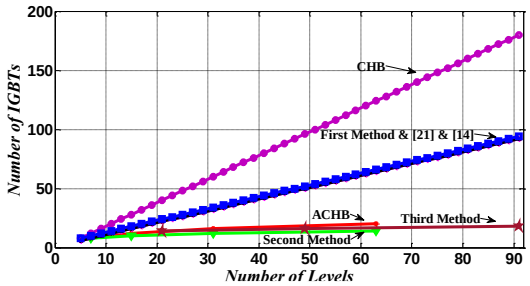


Fig. 12. The number of the power switches versus the output levels for the suggested inverter and other ones.

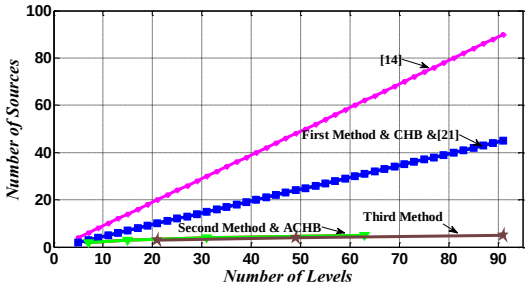


Fig. 13. The number of DC sources versus the output levels for the proposed topology and other ones.

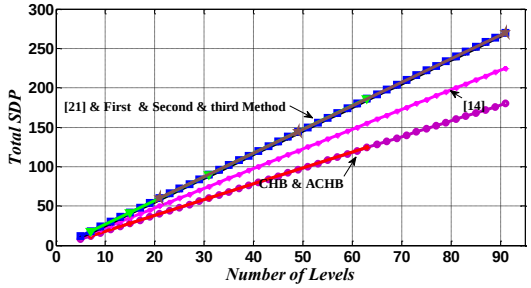


Fig. 14. Total SDP value versus output voltage levels for the proposed and other multilevel inverters

Figure 12 proves that the second method has the lowest number of switches for all of the output levels. Furthermore, switches number in generalized mode is close to the number of second method. In addition, the proposed inverter in second and third method needs fewer switches than CHB, ACHB, [14] and [21]

Obviously, cost of DC current sources forms a significant percent of the inverter cost. As a result, the number of DC current sources is too important in total cost of the inverter. The number of DC current sources versus output levels is shown in Fig. 13.

Figure 13 proves that the proposed inverter has reduced the number of DC current sources successfully in generalized and second modes. By taking into account other methods of the proposed topology, it is deduced that the number of DC current sources for the first method and [21] are the same as CHB.

The overall SDP of the above-mentioned topologies are contrasted in Fig. 14. As the proposed inverter is suitable to be applied in low/medium voltage, so the increment of SDP in comparison to the conventional MCSI can be uncared because of the achievement in reducing switch number.

5. Converter Power Loss

Generally, power loss of power electronic converters are made up of two parts:1) Conduction losses: Conduction losses are resultant of equivalent resistance and voltage drop of the semiconductor devices when they are on.2) Switching losses: Switching losses are originated as a result of the non-ideal characteristic of power switches. In this section calculation method of above-mentioned power losses for the presented multilevel inverter is explained in detail.

A. Conduction losses

The first step in computing conduction losses is to calculate it for a typical power switch along with a diode. In the next step, this method should be expanded to the whole of the system. The conduction losses proportional to switches and diodes is calculated as bellow, respectively.

$$P_{C,T}(t) = [V_T + R_T i^{\beta}(t)]i(t) \quad (18)$$

$$P_{C,D}(t) = [V_D + R_D i(t)]i(t) \quad (19)$$

Here, V_T and V_D represent the voltage across the transistor and diode when they are ON, RT and R_D displays equivalent resistance of them while β is related to transistor specifications.

The average conduction power losses of the presented

inverter is calculated as bellow [23], in which $x(t)$ and $y(t)$ is calculated via Eqs. (18) and (19) while demonstrate the number of transistors and diodes in the current direction, respectively.

$$P_C(t) = \frac{1}{\pi}\int_0^{\pi}\left[\begin{pmatrix} x(t)V_T + y(t)V_D + \\ x(t)R_T i^{\beta}(t) + y(t)R_D i(t) \end{pmatrix} i(t)\right] d\omega t \quad (20)$$

B. Switching losses

The switching losses of the proposed MCSI is calculated by expanding calculations of an identical power switch. So, the whole value of switching losses can be decomposed into two terms: 1) IGBT switching power loss. 2) Anti-parallel diodes power losses

The following expressions can be given:

$$P_{sw,T} = (E_{on,T} + E_{off,T}) f_{sw} \quad (21)$$

$$P_{sw,Anti-D} = (E_{on,Anti-D} + E_{off,Anti-D}) f_{sw}$$
$$P_{sw,Anti-D} \approx E_{on,Anti-D} f_{sw} \quad (22)$$

Here, *Psw*, *T* is switching power losses of the IGBT while Eon,Tand Eoff,Tdemonstrate energy losses of IGBT during turning ON and OFF. In addition, *fsw* symbolize the switching frequency. The Anti-D is an indicator related to the anti-parallel diodes. The switching losses are dependent on the amount switching frequency and method of modulation. Lately, the overall switching losses can be computed as following:

$$P_{sw} = \sum_1^i P_{sw,T_i} + P_{sw,Anti-D_i} \quad (23)$$

Where *i* represents the number of power switches.

The whole losses of the proposed multilevel converter can be computed using Eqs. (20) and (21) as following:

$$P_{loss} = P_{sw} + P_C \quad (24)$$

It worth to mention that the proposed inverter structure requires no diodes. As a result, the losses relevant to diodes are omitted in this topology. Fig. 15 depicts the power losses of proposed inverter versus the conventional converters while SPWM is utilized to study power losses. Moreover, BUP314 IGBTs [24] are applied in the simulation of converters.

It is clear from Fig. 15 that compared with after-mentioned inverters; the proposed structure in second mode has reduced power losses significantly due to a diminution in the number of power switches and the on-state ones.

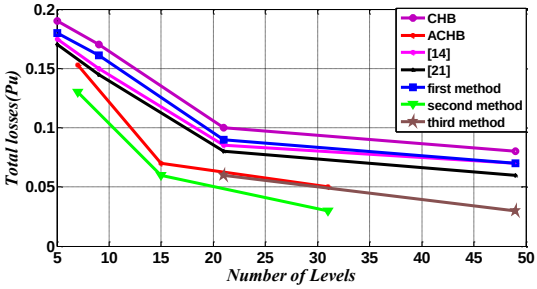


Fig. 15. Comparison of the power losses between the proposed and conventional structures

6. Conclusion

This paper proposes a new multilevel current source inverter which can be applied in low/medium power. In comparison to the conventional and recently proposed inverters, the proposed structure is capable of generating different output current levels by owning fewer circuit components such as DC current source, switches as well as related gate driver circuits. Lower number of circuit components leads to significant reduction of total cost and simplification of the control scheme. The other advantage of the proposed inverter is reduction of power loss which is resultant of adecrease in the number of switches. Furthermore, the ability to be used as an asymmetric inverter is the main advantage of this topology. In this mode, output levels can increase by suitable definition of DC sources level while there is no need to change the hardware of the inverter. As a result, various methods have been proposed to determine the magnitude of DC current sources. Multiple comparisons have been provided to prove the effectiveness of the proposed methods in selection of DC current sources magnitude. To validate simulation results, a low power prototype is proposed which tracks simulation results well and approves validity of the proposed MCSI structure. For first method five level prototype with two identical sources is constructed. For validating second method, a 7-level topology with two asymmetrical sources is implemented and for last method, 21-level converter with two module and three asymmetrical sources is constructed which results is verified the operation of converters.

REFERENCES

[1] M. R. Banaei, M. R. Jannati Oskuee and H. Khounjahan, "Reconfiguration of semi-cascaded multilevel inverter to improve systems performance parameters," *IET Power Electron.*, vol. 7, no. 5, pp. 1106-1112, 2014.

[2] M. R. Banaei, M. R. Jannati Oskuee and F. Mohajel Kazemi, "Series H-bridge with stacked multi-cell inverter to quadruplicate voltage levels," *IET Power Electron.*, vol. 6, no. 5, pp. 878-884, 2013.

[3] M. R. Banaei, F. Mohajel Kazemi, M. R. Jannati Oskuee, "New mixture of hybrid stacked multi-cell with half-

cascaded converter to increase voltage level," *IET Power Electron.*, vol. 6, no. 7, pp. 1406-1414, 2013.

[4] K. Sivakumar, D. Anandarup, R. Ramchand and C. Patel, "A hybrid multilevel inverter topology for an open-end winding induction-motor drive using two-level inverters in series with a capacitor-fed H-bridge cell," *IEEE Trans. Ind. Electrons*, vol. 57, no. 11, pp. 3707-3714, 2010.

[5] J. Rodriguez, J. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, 2002.

[6] M. Farhadi Kangarlu, E. Babaei and F. Blaabjerg, "An LCL-filtered single-phase multilevel inverter for grid integration of PV systems," *J. Oper. Autom. Power Engin.* ,vol. 4, no. 1, pp. 54-65, 2016.

[7] A. Ajami, M. R. Jannati Oskuee, A. Mokhberdoran, H. Shokri, "Selective harmonic elimination method for wide range of modulation indexes in multilevel inverters using ICA," *J. Cent. South Univ.*, vol. 21, no. 4, pp. 1329-1338, 2014.

[8] A. Ajami, M. R. Jannati Oskuee and A. Mokhberdoran, "Implementation of novel technique for selective harmonic elimination in multilevel inverters based on ICA," *Adv. Power Electron.*, vol. 2013, pp.1- 10, 2013.

[9] S. Laali, E. Babaei and M. B. B. Sharifian, "Reduction the number of power electronic devices of a cascaded multilevel inverter based on new general topology," *J. Oper. Autom. Power Eng.* ,vol. 2, no. 2, pp. 81-90, 2014.

[10] Y. Zhang and J. V. Milanovic, "Global voltage sag mitigation with FACTS based devices," *IEEE Trans. Power Deliv.*, vol. 25, no. 4, pp. 2842-2850, 2010.

[11] A. Llaria, O. Curea, J. Jiménez, and H. Camblong, "Survey on micro-grids: unplanned islanding and related inverter control techniques," *Renew. Energy*, vol. 36, no. 8, pp. 2052-2061, 2011.

[12] R. T. H. Li, H. S. Chung, and T. K. M. Chan, "An active modulation technique for single-phase grid connected CSI," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1373-1380, 2007.

[13] A. R. Beig and V. T. Ranganathan, "A novel CSI-fed induction motor drive." *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1073-1082, 2006.

[14] T. Noguchi and Suroso, "Review of novel multilevel current-source inverters with h-bridge and common-emitter based topologies," *Proc. IEEE Energy Convers. Congr. Expos.*, 2010, pp. 4006-4011.

[15] R. E. Torres-Olguin, A. Garces, M. Molinas and T. Undemand, "Integration of offshore wind farm using a hybrid HVDC transmission composed by the PWM current-source converter and line-commutated converter," *IEEE Trans. Energy Convers.*, vol. 28, no.1, pp. 125-134, 2013.

[16] V.Vekhande, N. Kothari and B. G. Fernandes, "Switching state vector selection strategies for paralleled multilevel current-fed inverter under unequal DC-link currents condition," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1998-2009, 2015.

[17] P. Cossutta, M. P. Aguirre, A. Cao, S. Raffo, and M. I. Vaua, "Single stage fuel cell to grid interface with multilevel current-source inverters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 5256-5264, 2015.

[18] S. Kwak, and H. A. Toliyat, "Multilevel converter topology using two types of current-source inverters," *IEEE Trans. Ind. Appl.*, vol. 42, no. 6, pp. 1558-1564, 2006.

[19] B. P. McGrath, and D. G. Holmes, "Natural current balancing of multi-cell current source inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1239-1246, 2008.

[20] Z. H. Bai, and Z. C. Zhang, "Conformation of multilevel current source converter topologies using the duality principle," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2260-2267, 2008.

[21] E. S. Najmi and A. Ajami, "Modular symmetric and asymmetric reduced count switch multilevel current source inverter," *IET Power Electron.*, vol. 9, no. 1, pp. 51-61, 2016.

[22] A. Nami, L. Jiaqi, F. Dijkhuizen, and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on converter cells and functionalities, " *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18-36, 2015.

[23] A. Ajami, M. R. Jannati Oskuee, M. T. Khosroshahi and A. Mokhberdoran, "Cascade multi-cell multilevel converter with reduced number of switches," *IET Power Electron.*, vol. 7, no. 3, pp. 552-558, 2014.

[24] Data sheet of IGBT 'BUP314', Available at: www.datasheetcatalog.com.